# BQ76942 High Accuracy 3-s to 10-s High Accuracy Battery Monitor and Protector for Li-Ion, Li- Polymer, and LiFePO4 Battery Packs

**Check for Samples: BQ76942**

ADVANCE INFORMATION

## 1 Features

- Battery monitoring capability for 3-series to 10-series cells
- Integrated charge pump for high-side NFET protection with optional autonomous recovery
- Extensive protection suite including voltage, temperature, current, and internal diagnostics
- Two independent ADCs
  - Support for simultaneous current and voltage sampling
  - High-accuracy coulomb counter with input offset error < 1 µV (typical)
  - High accuracy cell voltage measurement < 10 mV (typical)
- Wide-range current applications (±200-mV measurement range across sense resistor)
- Integrated secondary chemical fuse drive protection
- Autonomous or host-controlled cell balancing
- Multiple power modes (typical battery pack operating range conditions)
  - NORMAL mode: 250 µA
  - Multiple SLEEP mode options: 20 µA to 60 µA
  - Multiple DEEPSLEEP mode options: 10 µA to 14 µA
  - SHUTDOWN Mode: < 2 µA
- High voltage tolerance of 85 V on cell connect and select additional pins
- Support for temperature sensing using internal sensor and up to 9 external thermistors
- Integrated one-time-programmable (OTP) memory programmable by customers on production line
- Communication options include 400-kHz $I^2C$, SPI, and HDQ one-wire interface
- Dual programmable LDOs for external system usage
- 48-pin TQFP package (PFB)

## 2 Applications

- Cordless power tools and garden tools
- Vacuum cleaners
- E-bike, e-scooter, and LEV
- Non-military drones
- Other industrial battery pack (3s-10s)

## 3 Description

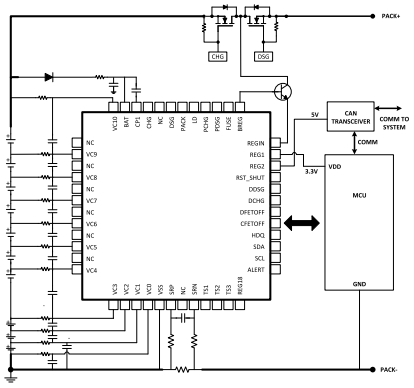
The Texas Instruments BQ76942 is a highly integrated, high accuracy battery monitor and protector for 3-series to 10-series Li-Ion, Li-Polymer, and LiFePO4 battery packs. The device includes a high accuracy monitoring system, a highly configurable protection subsystem, and support for autonomous or host controlled cell balancing. Integration includes high-side charge-pump NFET drivers, dual programmable LDOs for external system use, and a host communication peripheral supporting 400-kHz $I^2C$, SPI, and HDQ one-wire standards. The BQ76942 is available in a 48-pin TQFP package.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| BQ76942 | PFB (48-pin) | 7 mm × 7 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Simplified Schematic**



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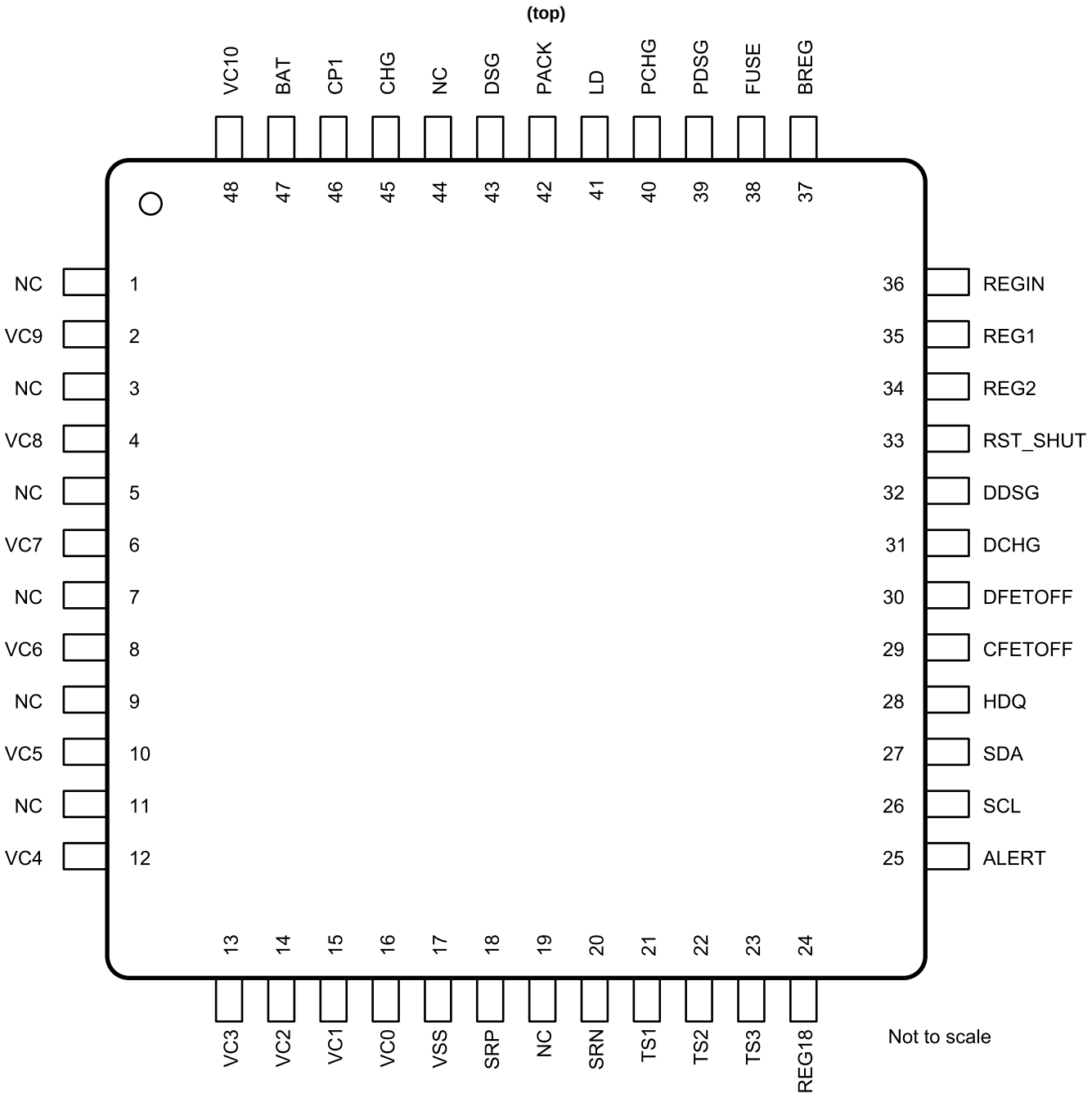
## 4 Revision History

| DATE | REVISION | NOTES |
|---|---|---|
| December 2019 | * | Initial Release |

## 5 Pin Configuration and Functions




ADVANCE INFORMATION

**BQ76942 TQFP Package (PFB) Pin Functions**

| PIN | | I/O | TYPE | DESCRIPTION |
|---|---|---|---|---|
| NO. | NAME | | | |
| 1 | NC | — | — | NC |
| 2 | VC9 | I | IA | Sense voltage input pin for the ninth cell from the bottom of the stack, balance current input for the ninth cell from the bottom of the stack, and return balance current for the tenth cell from the bottom of the stack. |
| 3 | NC | — | — | NC |

**BQ76942 TQFP Package (PFB) Pin Functions (continued)**

| PIN | | I/O | TYPE | DESCRIPTION |
|---|---|---|---|---|
| NO. | NAME | | | |
| 4 | VC8 | I | IA | Sense voltage input pin for the eighth cell from the bottom of the stack, balance current input for the eighth cell from the bottom of the stack, and return balance current for the ninth cell from the bottom of the stack. |
| 5 | NC | — | — | NC |
| 6 | VC7 | I | IA | Sense voltage input pin for the seventh cell from the bottom of the stack, balance current input for the seventh cell from the bottom of the stack and return balance current for the eighth cell from the bottom of the stack. |
| 7 | NC | — | — | NC |
| 8 | VC6 | I | IA | Sense voltage input pin for the sixth cell from the bottom of the stack, balance current input for the sixth cell from the bottom of the stack, and return balance current for the seventh cell from the bottom of the stack. |
| 9 | NC | — | — | NC |
| 10 | VC5 | I | IA | Sense voltage input pin for the fifth cell from the bottom of the stack, balance current input for the fifth cell from the bottom of the stack, and return balance current for the sixth cell from the bottom of the stack. |
| 11 | NC | — | — | NC |
| 12 | VC4 | I | IA | Sense voltage input pin for the fourth cell from the bottom of the stack, balance current input for the fourth cell from the bottom of the stack, and return balance current for the fifth cell from the bottom of the stack. |
| 13 | VC3 | I | IA | Sense voltage input pin for the third cell from the bottom of the stack, balance current input for the third cell from the bottom of the stack, and return balance current for the fourth cell from the bottom of the stack. |
| 14 | VC2 | I | IA | Sense voltage input pin for the second cell from the bottom of the stack, balance current input for the second cell from the bottom of the stack, and return balance current for the third cell from the bottom of the stack. |
| 15 | VC1 | I | IA | Sense voltage input pin for the first cell from the bottom of the stack, balance current input for the first cell from the bottom of the stack, and return balance current for the second cell from the bottom of the stack. |
| 16 | VC0 | I | IA | Sense voltage input pin for negative terminal of the first cell from the bottom of the stack, and return balance current for first cell from the bottom of the stack. |
| 17 | VSS | — | P | Device ground |
| 18 | SRP | I | IA | Analog input pin connected to the internal coulomb counter peripheral for integrating a small voltage between SRP and SRN, where SRP is the top of the sense resistor. A charging current generates a positive voltage at SRP relative to SRN. |
| 19 | NC | — | — | NC |
| 20 | SRN | I | IA | Analog input pin connected to the internal coulomb counter peripheral for integrating a small voltage between SRP and SRN, where SRN is the bottom of the sense resistor. A charging current generates a positive voltage at SRP relative to SRN. |
| 21 | TS1 | I/O | OD, I/OA | Thermistor input, or general purpose ADC input. |
| 22 | TS2 | I/O | OD, I/OA | Thermistor input and functions as wakeup from SHUTDOWN, or general purpose ADC input. |
| 23 | TS3 | I/O | OD, I/OA | Thermistor input, or general purpose ADC input. |
| 24 | REG18 | O | P | Internal 1.8 V LDO output (only for internal use). |
| 25 | ALERT | I/O | I/OD, I/OA | Multifunction pin, can be ALERT output, or HDQ I/O, or thermistor input, or general purpose ADC input, or general purpose digital output. |
| 26 | SCL | I/O | I/OD | Multifunction pin, can be SCL or SPI_SCLK. |
| 27 | SDA | I/O | I/OD | Multifunction pin, can be SDA or SPI_MISO. |
| 28 | HDQ | I/O | I/OD, I/OA | Multifunction pin, can be HDQ I/O, or SPI_MOSI, or thermistor input, or general purpose ADC input, or general purpose digital output. |
| 29 | CFETOFF | I/O | I/OD, I/OA | Multifunction pin, can be CFETOFF, or SPI_CS, or thermistor input, or general purpose ADC input, or general purpose digital output. |
| 30 | DFETOFF | I/O | I/OD, I/OA | Multifunction pin, can be DFETOFF or BOTHOFF, or thermistor input, or general purpose ADC input, or general purpose digital output. |
| 31 | DCHG | I/O | OD, I/OA | Multifunction pin, can be DCHG, or thermistor input, or general purpose ADC input, or general purpose digital output. |

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**BQ76942 TQFP Package (PFB) Pin Functions (continued)**

| PIN | | I/O | TYPE | DESCRIPTION |
|---|---|---|---|---|
| NO. | NAME | | | |
| 32 | DDSG | I/O | OD, I/OA | Multifunction pin, can be DDSG, or thermistor input, or general purpose ADC input, or general purpose digital output. |
| 33 | RST_SHUT | I | ID | Digital input pin for reset or shutdown. |
| 34 | REG2 | O | P | Second LDO (REG2) output, which can be programmed for 1.8 V, 2.5 V, 3.0 V, 3.3 V, or 5.0 V. |
| 35 | REG1 | O | P | First LDO (REG1) output, which can be programmed for 1.8 V, 2.5 V, 3.0 V, 3.3 V, or 5.0 V. |
| 36 | REGIN | I | IA | Input pin for REG1 and REG2 LDOs |
| 37 | BREG | O | OA | Base control signal for external pre-regulator transistor. |
| 38 | FUSE | I/O | I/OA | Fuse sense and drive |
| 39 | PDSG | O | OA | Predischarge PFET control |
| 40 | PCHG | O | OA | Precharge PFET control |
| 41 | LD | I/O | I/OA | Load detect pin |
| 42 | PACK | I | IA | Pack sense input pin |
| 43 | DSG | O | OA | NMOS Discharge FET drive output pin |
| 44 | NC | — | — | NC |
| 45 | CHG | O | OA | NMOS Charge FET drive output pin |
| 46 | CP1 | I/O | I/OA | Charge pump capacitor |
| 47 | BAT | I | P | Primary power supply input pin |
| 48 | VC10 | I | IA | Sense voltage input pin for the tenth cell from the bottom of the stack, balance current input for the tenth cell from the bottom of the stack, and top-of-stack measurement point. |

ADVANCE INFORMATION

# 6 Specifications

## 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).(1)

| DESCRIPTION | PINS | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage range | BAT | VSS–0.3 | VSS+85 | V |
| Input voltage range, $V_{IN}$ | PACK, PCHG, PDSG, LD | VSS–0.3 | VSS+85 | V |
| Input voltage range, $V_{IN}$ | REGIN | VSS–0.3 | the minimum of VSS+6 or $V_{BAT}$+0.3 | V |
| Input voltage range, $V_{IN}$ | BREG, FUSE(2) | VSS–0.3 | VSS+20 | V |
| Input voltage range, $V_{IN}$ | REG1, REG2, ALERT, SCL, SDA, HDQ, CFETOFF, DFETOFF, DCHG, DDSG, RST_SHUT (3) | VSS–0.3 | VSS+6 | V |
| Input voltage range, $V_{IN}$ | TS1, TS2, TS3, ALERT, CFETOFF, DFETOFF, HDQ, DCHG, DDSG (when used as thermistor or general purpose ADC input) | VSS–0.3 | $V_{REG18}$ + 0.3 | V |
| Input voltage range, $V_{IN}$ | SRP, SRN | VSS–0.3 | $V_{REG18}$ + 0.3 | V |
| Input voltage range, $V_{IN}$ | VC10 | VC9–0.3 | VSS+85 | V |
| Input voltage range, $V_{IN}$ | VC9 | VC8–0.3 | VSS+85 | V |
| Input voltage range, $V_{IN}$ | VC8 | VC7–0.3 | VSS+85 | V |
| Input voltage range, $V_{IN}$ | VC7 | VC6–0.3 | VSS+85 | V |
| Input voltage range, $V_{IN}$ | VC6 | VC5–0.3 | VSS+85 | V |
| Input voltage range, $V_{IN}$ | VC5 | VC4–0.3 | VSS+85 | V |
| Input voltage range, $V_{IN}$ | VC4 | VC3–0.3 | VSS+85 | V |
| Input voltage range, $V_{IN}$ | VC3 | VC2–0.3 | VSS+85 | V |
| Input voltage range, $V_{IN}$ | VC2 | VC1–0.3 | VSS+85 | V |
| Input voltage range, $V_{IN}$ | VC1 | VC0–0.3 | VSS+85 | V |
| Input voltage range, $V_{IN}$ | VC0 | VSS–0.3 | VSS+6 | V |
| Output voltage range, $V_O$ | CP1 | $V_{BAT}$–0.3 | the minimum of VSS+85 or $V_{BAT}$+15 | V |
| Output voltage range, $V_O$ | CHG | VSS–0.3 | VSS+85 | V |
| Output voltage range, $V_O$ | DSG | VSS–0.3 | VSS+85 | V |
| Output voltage range, $V_O$ | REG1, REG2, TS2 (for wakeup function), ALERT, CFETOFF, DFETOFF, HDQ, DCHG, DDSG, when configured to drive a digital output | VSS–0.3 | VSS+6 | V |
| Output voltage range, $V_O$ | REG18 | VSS–0.3 | VSS+2 | V |
| Maximum cell balancing current, all cells | VC0 – VC10 | | 100 | mA |
| Maximum VSS current, $I_{SS}$ | | | 75 | mA |
| Functional temperature, $T_{FUNC}$ | | –40 | 85 | °C |
| Junction temperature, $T_J$ | | –65 | 150 | °C |
| Storage temperature, $T_{STG}$ | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The current allowed to flow into the FUSE pin must be limited (such as by using external series resistance) to 2 mA or less.
(3) When the ALERT, HDQ, CFETOFF, DFETOFF, DCHG, or DDSG pins are selected for thermistor input or general purpose ADC–input, their voltage is limited to $V_{REG18}$ + 0.3 V. These pins can accept up to 6 V when configured for other uses, such as a digital input.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±1000 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## ESD Ratings (continued)

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±250 | V |

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

Typical values stated where $T_A$ = 25°C and $V_{BAT}$ = 37.0 V, min and max values stated where $T_A$ = -40°C to 85°C and $V_{BAT}$ = 4.7 V to 55 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{BAT}$ | Supply voltage | Voltage on BAT pin (normal operation) | 4.7 | | 55 | V |
| $V_{BAT}$ | Supply voltage | Voltage on BAT pin (OTP programming) | 10 | | 12 | V |
| $T_{OTP}$ | OTP programming temperature | | -40 | | 45 | °C |
| $V_{PORA}$ | Power-on reset | Rising threshold on BAT | 3 | | 4 | V |
| $V_{PORA\_HYS}$ | Power-on reset hysteresis | Device shuts down when BAT < $V_{PORA}$ - $V_{PORA\_HYS}$ | | 250 | | mV |
| $V_{WAKEONLD}$ | Wake on LD voltage | Rising edge on LD, with BAT already in valid range | 0.95 | | 4.5 | V |
| $V_{WAKEONTS2}$ | Wake on TS2 voltage | Falling edge on TS2, with BAT already in valid range. TS2 will be weakly driven with a 5 V level during shutdown. | 0.7 | | 1.1 | V |
| $V_{IN}$ | Input voltage range | PACK, PCHG, PDSG, LD | 0 | | 55 | V |
| $V_{IN}$ | Input voltage range | REG1, REG2, RST_SHUT, ALERT, SCL, SDA, HDQ, CFETOFF, DFETOFF, DCHG, DDSG, except when the pin is being used for general purpose ADC input or thermistor measurement. | 0 | | 5.5 | V |
| $V_{IN}$ | Input voltage range | TS1, TS2, TS3, CFETOFF, DFETOFF, DCHG, DDSG, ALERT, HDQ, when the pin is configured for general purpose ADC input or thermistor measurement. | 0 | | $V_{REG18}$ | V |
| $V_{IN}$ | Input voltage range | SRP, SRN, SRP-SRN (while measuring current) | –0.2 | | 0.2 | V |
| $V_{IN}$ | Input voltage range | SRP, SRN (without measuring current) | –0.2 | | $V_{REG18}$ | V |
| $V_{IN}$ | Input voltage range | $V_{VC(0)}$ | –0.2 | | 5.5 | V |
| $V_{IN}$ | Input voltage range | $V_{VC(x)}$, 1 ≤ x ≤ 4 | maximum of $V_{VC(x–1)}$ – 0.2 or VSS–0.2 | | minimum of $V_{VC(x–1)}$+5.5 or VSS+55 | V |
| $V_{IN}$ | Input voltage range | $V_{VC(x)}$, x ≥ 5 | maximum of $V_{VC(x–1)}$ – 0.2 or VSS + 2.0 | | minimum of $V_{VC(x–1)}$ + 5.5 or VSS + 55 | V |
| $V_O$ | Output voltage range | LD | | | 55 | V |
| $V_O$ | Output voltage range | CHG, DSG, CP1 | | | 70 | V |
| $T_{OPR}$ | Operating temperature | | –40 | | 85 | °C |
| $V_{CELL(ACC)}$ | Cell voltage measurement accuracy | 2 V < $V_{VC(x)}$ - $V_{VC(x-1)}$ < 5 V, $T_A$ = 25°C, 1 ≤ x ≤ 10(1) | –5 | | 5 | mV |

(1) Cell voltage accuracy is specified after completion of board offset calibration.

ADVANCE INFORMATION

## Recommended Operating Conditions (continued)

Typical values stated where $T_A$ = 25°C and $V_{BAT}$ = 37.0 V, min and max values stated where $T_A$ = -40°C to 85°C and $V_{BAT}$ = 4.7 V to 55 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CELL(ACC)}$ | Cell voltage measurement accuracy | 2 V < $V_{VC(x)}$ - $V_{VC(x-1)}$ < 5 V, $T_A$ = 0°C to 60°C, 1 ≤ x ≤ 10(1) | –10 | | 10 | mV |
| $V_{CELL(ACC)}$ | Cell voltage measurement accuracy | –0.2 V < $V_{VC(x)}$ - $V_{VC(x-1)}$ < 5.5 V, $T_A$ = -40°C to 85°C, 1 ≤ x ≤ 16(1) | –15 | | 15 | mV |
| $V_{STACK(ACC)}$ | Stack voltage (VC10 - VSS) measurement accuracy | 0 V < $V_{VC10}$ - $V_{VSS}$ < 55 V, $T_A$ = -40°C to 85°C(1) | –0.5 | | 0.5 | V |
| $V_{PACK(ACC)}$ | PACK pin voltage measurement accuracy | 0 V < $V_{PACK}$ < 55 V, $T_A$ = -40°C to 85°C(1) | –0.5 | | 0.5 | V |
| $V_{LD(ACC)}$ | LD pin voltage measurement accuracy | 0 V < $V_{LD}$ < 55 V, $T_A$ = -40°C to 85°C(1) | –0.5 | | 0.5 | V |

## 6.4 Thermal Information BQ76942

| THERMAL METRIC(1) | | BQ76942 PFB (TQFP) 48 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 66.0 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 19.6 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 29.3 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 0.8 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 29.1 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.5 Supply Current

Typical values stated where $T_A$ = 25°C and $V_{BAT}$ = 37.0 V, min and max values stated where $T_A$ = -40°C to 85°C and $V_{BAT}$ = 4.7 V to 55 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{NORMAL}$ | Normal Mode | Regular measurements and protections active, REG1 = 3.3 V with no load, REG2 = OFF, CHG = ON in 11 V overdrive mode, DSG = ON in 11 V overdrive mode, ***Settings:Configuration:Power Config[FASTADC]*** = 0, no communication | | 250 | | µA |
| $I_{SLEEP\_1}$ | SLEEP Mode | Periodic protections and monitoring, no pack current, REG1 = OFF, REG2 = OFF, CHG = OFF, DSG = ON in 11 V overdrive mode, no communication, ***Power:Sleep:Voltage Time*** = 5 s | | 60 | | µA |
| $I_{SLEEP\_2}$ | SLEEP Mode | Periodic protections and monitoring, no pack current, REG1 = OFF, REG2 = OFF, CHG = OFF, DSG = source follower mode, no communication, ***Power:Sleep:Voltage Time*** = 5 s | | 20 | | µA |
| $I_{DEEPSLEEP\_1}$ | DEEPSLEEP Mode | No monitoring or protections, REG1 = 3.3 V with no load, REG2 = OFF, LFO = ON, no communication | | 14 | | µA |
| $I_{DEEPSLEEP\_2}$ | DEEPSLEEP Mode | No monitoring or protections, REG1 = 3.3 V with no load, REG2 = OFF, LFO = OFF, no communication | | 10 | | µA |
| $I_{SHUTDOWN}$ | SHUTDOWN Mode | All blocks powered down, with the exception of the TS2 wakeup circuit, no monitoring or protections, no communication | | 1 | 2 | µA |

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## 6.6 Digital I/O

Typical values stated where $T_A$ = 25°C and $V_{BAT}$ = 37.0 V, min and max values stated where $T_A$ = -40°C to 85°C and $V_{BAT}$ = 4.7 V to 55 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input | ALERT (configured as HDQ), SCL, SDA, HDQ, CFETOFF, DFETOFF, RST_SHUT | 0.65 x $V_{REG18}$ | | 5.5 | V |
| $V_{IL}$ | Low-level input | ALERT (configured as HDQ), SCL, SDA, HDQ, CFETOFF, DFETOFF, RST_SHUT | | | 0.35 x $V_{REG18}$ | V |
| $V_{OH}$ | Output voltage high, TS2 | TS2 during SHUTDOWN mode, $V_{BAT}$ > 6 V | 4.5 | | 5.5 | V |
| $V_{OH}$ | Output voltage high, TS2 low voltage | TS2 during SHUTDOWN mode, 4.7 V ≤ $V_{BAT}$ ≤ 6 V | 3 | | 5.5 | V |
| $V_{OH}$ | Output voltage high, 5 V case | ALERT, SDA (configured as SPI_MISO), CFETOFF (configured as GPO), DFETOFF (configured as GPO), DCHG, DDSG pins driving from REG1, $V_{REG1}$ set to 5 V nominal setting, $V_{BAT}$ > 8 V, $I_{OH}$ = 5.0 mA, 10 pF load | 0.9 x $V_{REG1}$ | | $V_{REG1}$ | V |
| $V_{OL}$ | Output voltage low, 5 V case | ALERT, SCL, SDA, HDQ, DCHG, DDSG, CFETOFF (configured as GPO), DFETOFF (configured as GPO), pins driving from REG1, $V_{REG1}$ set to 5 V nominal setting, $V_{BAT}$ > 8 V, $I_{OL}$ = -5 mA, 10 pF load | | | 0.4 | V |
| $R_{OH}$ | Output weak high resistance | TS2 during SHUTDOWN mode | | 5000 | | kΩ |
| $C_{IN}$ | Input capacitance | ALERT, SCL, SDA, HDQ, CFETOFF, DFETOFF, DCHG, DDSG, REGIN, TS1, TS2, TS3 | | 5 | | pF |
| $I_{LKG}$ | Input leakage current | ALERT, SCL, SDA, HDQ, CFETOFF, DFETOFF, DCHG, DDSG, REGIN, device in SHUTDOWN mode | | | 1 | µA |

## 6.7 LD Pin

Typical values stated where $T_A$ = 25°C and $V_{BAT}$ = 37.0 V, min and max values stated where $T_A$ = -40°C to 85°C and $V_{BAT}$ = 4.7 V to 55 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{(PULLUP)}$ | Internal pullup current from BAT pin to LD pin, used for load detect functionality | $V_{BAT}$ ≥ 4.7 V, $V_{LD}$ = VSS | 35 | 100 | 155 | µA |
| $R_{PD}$ | Internal pulldown resistance on LD pin in SHUTDOWN mode | $V_{BAT}$ ≥ 4.7 V | | 80 | | kΩ |

## 6.8 Precharge (PCHG) and Predischarge (PDSG) FET Drive

Typical values stated where $T_A$ = 25°C and $V_{BAT}$ = 37.0 V, min and max values stated where $T_A$ = -40°C to 85°C and $V_{BAT}$ = 4.7 V to 55 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{(PCHG\_ON)}$ | Output voltage, PCHG on | max($V_{PACK}$, $V_{BAT}$) - $V_{PCHG}$, $V_{PACK}$ ≥ 8 V, $V_{BAT}$ ≥ 4.7 V | 7.7 | 8.7 | 9.7 | V |
| $V_{(PCHG\_ON)}$ | Output voltage, PCHG on | $V_{PACK}$ - $V_{PCHG}$, 4.7 V ≤ $V_{PACK}$ < 8 V, $V_{BAT}$ ≥ 4.7 V, $V_{PACK}$ > $V_{BAT}$ | $V_{PACK}$ – 0.5 V | | $V_{PACK}$ | V |
| $V_{(PDSG\_ON)}$ | Output voltage, PDSG on | max($V_{LD}$, $V_{BAT}$) - $V_{PDSG}$, $V_{BAT}$ ≥ 8 V | 7.7 | 8.7 | 9.7 | V |
| $V_{(PDSG\_ON)}$ | Output voltage, PDSG on | $V_{BAT}$ - $V_{PDSG}$, 4.7 V ≤ $V_{BAT}$ < 8 V, $V_{BAT}$ > $V_{LD}$ | $V_{BAT}$ – 0.5 V | | $V_{BAT}$ | V |
| $I_{(PULLDOWN)}$ | Current sink capability, PCHG and PDSG | PCHG and PDSG enabled, $V_{BAT}$ = 37.0 V | | TBD | | µA |

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## 6.9 FUSE Pin Functionality

Typical values stated where $T_A$ = 25°C and $V_{BAT}$ = 37.0 V, min and max values stated where $T_A$ = -40°C to 85°C and $V_{BAT}$ = 4.7 V to 55 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{(OH)}$ | Output voltage high (when driving fuse) | $V_{BAT}$ ≥ 8 V, $C_L$ = 1 nF, 5 kΩ load. | 6 | 7 | 9 | V |
| $V_{(OH)}$ | Output voltage high (when driving fuse) | 4.7 V ≤ $V_{BAT}$ < 8 V, $C_L$ = 1 nF, 5 kΩ load. | $V_{BAT}$ – 1.5 | | | V |
| $V_{(IH)}$ | High-level input (for fuse detection) | Current into device pin must be limited to maximum 2 mA | 2 | | 12 | V |
| $V_{(IL)}$ | Low-level input (for fuse detection) | | | | 0.7 | V |
| $t_{(RISE)}$ | Output rise time (when driving fuse) | $V_{BAT}$ ≥ 8 V, $C_L$ = 1 nF, $R_{SERIES}$ = 100 Ω, $V_{(OH)}$ = 10% to 90% of final settled voltage | | 0.5 | | µs |

## 6.10 Power-On Reset

Typical values stated where $T_A$ = 25°C and $V_{BAT}$ = 37.0 V, min and max values stated where $T_A$ = -40°C to 85°C and $V_{BAT}$ = 4.7 V to 55 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{REGPOR-}$ | Threshold when voltage is falling | $V_{REG18}$ on and falling | 1.62 | | TBD | V |
| $V_{REGPOR+}$ | Threshold when voltage is rising | $V_{REG18}$ on and rising | 1.62 | | TBD | V |
| $V_{PORhys}$ | Power-on reset hysteresis | $V_{BAT}$ ≥ 4.7V, $V_{PACK}$ = VSS | | 100 | | mV |
| $t_{RST}$ | Power-on reset time | | | 300 | | µs |

## 6.11 REG18 LDO

Typical values stated where $T_A$ = 25°C and $V_{BAT}$ = 37.0 V, min and max values stated where $T_A$ = -40°C to 85°C and $V_{BAT}$ = 4.7 V to 55 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $C_{REG18}$ | External capacitor, REG18 to VSS | | 1.8 | 2.2 | 22 | µF |
| $V_{REG18}$ | Regulator voltage | | 1.6 | 1.8 | 2 | V |
| $\Delta V_{O(TEMP)}$ | Regulator output over temperature | $\Delta V_{REG18}$ vs $V_{REG18}$ at 25°C, $I_{REG18}$ = 1 mA, $V_{BAT}$ = 37.0 V | | ±0.25 | | % |
| $\Delta V_{O(LINE)}$ | Line regulation | $\Delta V_{REG18}$ vs ($V_{REG18}$ at 25°C, $V_{BAT}$ = 37.0 V, $I_{REG18}$ = 1 mA), as $V_{BAT}$ varies across specified range | –0.6 | | 0.5 | % |
| $\Delta V_{O(LOAD)}$ | Load regulation | $\Delta V_{REG18}$ vs ($V_{REG18}$, $V_{BAT}$ = 37.0 V), $I_{REG18}$ = 0 mA to 1 mA, at 25°C | –1.5 | | 1.5 | % |
| $I_{SC}$ | Regulator short-circuit current limit | $V_{REG18}$ = 0 V | 3 | | 14 | mA |

## 6.12 REG0 Pre-regulator

Typical values stated where $T_A$ = 25°C and $V_{BAT}$ = 37.0 V, min and max values stated where $T_A$ = -40°C to 85°C and $V_{BAT}$ = 4.7 V to 55 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{BREG\_HDRM}$ | Pre-regulator control voltage headroom ( min($V_{BAT}$ - $V_{BREG}$) ) | $V_{BAT}$ ≥ 4.7 V | | 1.5 | 1.75 | V |
| $V_{REGIN\_INT}$ | Pre-regulator voltage, when generated using BREG | $V_{BAT}$ requirement depends on external device selected | 5 | 5.5 | 5.8 | V |
| $V_{REGIN\_EXT}$ | Pre-regulator voltage when using externally supplied REGIN | See requirements based on settings of REG1 and REG2 | | | 5.75 | V |
| $\Delta V_{O(TEMP)}$ | Regulator output over temperature | $\Delta V_{REGIN}$ vs $V_{REGIN}$ at 25°C, $I_{REGIN}$ = 50 mA | | ±5 | | % |
| $I_{Max}$ | Maximum current driven out from BREG | Under short circuit conditions ($V_{REGIN}$ = 0 V) | 1 | 3.33 | | mA |
| $C_{EXT}$ | External capacitor REGIN to VSS | | 2.2 | 10 | 22 | nF |
| $C_{BREG}$ | External capacitor BREG to VSS | | | | 25 | pF |

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## REG0 Pre-regulator (continued)

Typical values stated where $T_A$ = 25°C and $V_{BAT}$ = 37.0 V, min and max values stated where $T_A$ = -40°C to 85°C and $V_{BAT}$ = 4.7 V to 55 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $R_{CL}$ | Current limiting resistor from BREG pin to NPN base (1) | | 0 | | 10 | kΩ |

(1) Adding a series resistor in the BASE will effectively limit the maximum current through the NPN.

## 6.13 REG1 LDO

Typical values stated where $T_A$ = 25°C and $V_{BAT}$ = 37.0 V, min and max values stated where $T_A$ = -40°C to 85°C and $V_{BAT}$ = 4.7 V to 55 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{REG1\_1.8}$ | Regulator voltage (nominal 1.8V setting) | $V_{REGIN}$ ≥ 3.0 V, $I_{REG1}$ = 0 mA to 50 mA | 1.6 | 1.8 | 2 | V |
| $V_{REG1\_2.5}$ | Regulator voltage (nominal 2.5V setting) | $V_{REGIN}$ ≥ 3.5 V, $I_{REG1}$ = 0 mA to 50 mA | 2.25 | 2.5 | 2.75 | V |
| $V_{REG1\_3.0}$ | Regulator voltage (nominal 3.0V setting) | $V_{REGIN}$ ≥ 3.8 V, $I_{REG1}$ = 0 mA to 50 mA | 2.7 | 3.0 | 3.3 | V |
| $V_{REG1\_3.3}$ | Regulator voltage (nominal 3.3V setting) | $V_{REGIN}$ ≥ 4.1 V, $I_{REG1}$ = 0 mA to 50 mA | 3.05 | 3.35 | 3.65 | V |
| $V_{REG1\_5.0}$ | Regulator voltage (nominal 5.0V setting) | $V_{REGIN}$ ≥ 5.2 V, $I_{REG1}$ = 0 mA to 50 mA | 4.5 | 5.0 | 5.5 | V |
| $\Delta V_{O(TEMP)}$ | Regulator output over temperature | $\Delta V_{REG1}$ vs ($V_{REG1}$ at 25°C, $I_{REG1}$ = 20 mA, $V_{REGIN}$ = 5.5 V, $V_{REG1}$ set to nominal 3.3 V setting) | | ±0.25 | | % |
| $\Delta V_{O(LINE)}$ | Line regulation | $\Delta V_{REG1}$ vs ($V_{REG1}$ at 25°C, $V_{REGIN}$ = 5.5 V, $I_{REG1}$ = 20 mA), as $V_{REGIN}$ varies from 5 V to 6 V, $V_{REG1}$ set to nominal 3.3 V setting | –1 | | 1 | % |
| $I_{SC}$ | Regulator short-circuit current limit | $V_{REG1}$ = 0 V | 55 | | 80 | mA |
| $C_{EXT}$ | External capacitor REG1 to VSS | | 1 | | | µF |

## 6.14 REG2 LDO

Typical values stated where $T_A$ = 25°C and $V_{BAT}$ = 37.0 V, min and max values stated where $T_A$ = -40°C to 85°C and $V_{BAT}$ = 4.7 V to 55 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{REG2\_1.8}$ | Regulator voltage (nominal 1.8V setting) | $V_{REGIN}$ ≥ 3.0 V, $I_{REG2}$ = 0 mA to 50 mA | 1.6 | 1.8 | 2 | V |
| $V_{REG2\_2.5}$ | Regulator voltage (nominal 2.5V setting) | $V_{REGIN}$ ≥ 3.5 V, $I_{REG2}$ = 0 mA to 50 mA | 2.25 | 2.5 | 2.75 | V |
| $V_{REG2\_3.0}$ | Regulator voltage (nominal 3.0V setting) | $V_{REGIN}$ ≥ 3.8 V, $I_{REG2}$ = 0 mA to 50 mA | 2.7 | 3.0 | 3.3 | V |
| $V_{REG2\_3.3}$ | Regulator voltage (nominal 3.3V setting) | $V_{REGIN}$ ≥ 4.1 V, $I_{REG2}$ = 0 mA to 50 mA | 3.0 | 3.3 | 3.6 | V |
| $V_{REG2\_5.0}$ | Regulator voltage (nominal 5.0V setting) | $V_{REGIN}$ ≥ 5.2 V, $I_{REG2}$ = 0 mA to 50 mA | 4.5 | 5.0 | 5.5 | V |
| $\Delta V_{O(TEMP)}$ | Regulator output over temperature | $\Delta V_{REG2}$ vs ($V_{REG2}$ at 25°C, $I_{REG2}$ = 20 mA, $V_{REGIN}$ = 5.5 V, $V_{REG2}$ set to nominal 3.3 V setting) | | ±0.25 | | % |
| $\Delta V_{O(LINE)}$ | Line regulation | $\Delta V_{REG2}$ vs ($V_{REG2}$ at 25°C, $V_{REGIN}$ = 5.5 V, $I_{REG2}$ = 20 mA), as $V_{REGIN}$ varies from 5 V to 6 V, $V_{REG2}$ set to nominal 3.3 V setting | –1 | | 1 | % |
| $I_{SC}$ | Regulator short-circuit current limit | $V_{REG2}$ = 0 V | 55 | | 80 | mA |
| $C_{EXT}$ | External capacitor REG2 to VSS | | 1 | | | µF |

## 6.15 Voltage References

Typical values stated where $T_A$ = 25°C and $V_{BAT}$ = 37.0 V, min and max values stated where $T_A$ = -40°C to 85°C and $V_{BAT}$ = 4.7 V to 55 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **VOLTAGE REFERENCE 1** | | | | | | |
| $V_{(REF1)}$ | Internal reference voltage (1) | $T_A$ = 25°C | 1.213 | 1.215 | 1.217 | V |

(1) $V_{(REF1)}$ is used for the ADC reference. Its effective value is determined through indirect measurement using the ADC.

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## Voltage References (continued)

Typical values stated where $T_A$ = 25°C and $V_{BAT}$ = 37.0 V, min and max values stated where $T_A$ = -40°C to 85°C and $V_{BAT}$ = 4.7 V to 55 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{(REF1DRIFT)}$ | Internal reference voltage drift (1) | $T_A$ = 0°C to 60°C | | ±27 | | PPM/°C |
| $V_{(REF1DRIFT)}$ | Internal reference voltage drift (1) | $T_A$ = -40°C to 85°C | | ±27 | | PPM/°C |
| **VOLTAGE REFERENCE 2** | | | | | | |
| $V_{(REF2)}$ | Internal reference voltage (2) | $T_A$ = 25°C | 1.23 | 1.24 | 1.25 | V |
| $V_{(REF2DRIFT)}$ | Internal reference voltage drift (2) | $T_A$ = 0°C to 60°C | | ±50 | | PPM/°C |
| $V_{(REF2DRIFT)}$ | Internal reference voltage drift (2) | $T_A$ = -40°C to 85°C | | ±80 | | PPM/°C |

(2) $V_{(REF2)}$ is used for the LDO, coulomb counter, and current measurement.

## 6.16 Coulomb Counter

Typical values stated where $T_A$ = 25°C and $V_{BAT}$ = 37.0 V, min and max values stated where $T_A$ = -40°C to 85°C and $V_{BAT}$ = 4.7 V to 55 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{(CC\_IN)}$ | Input voltage range for measurements | $V_{SRP}$ - $V_{SRN}$ | –0.2 | | 0.2 | V |
| $V_{(CC\_IN)}$ | Input voltage range for measurements | $V_{SRP}$, $V_{SRN}$ | –0.2 | | 0.2 | V |
| $B_{(CC\_INL)}$ | Integral nonlinearity (1) | 16-bit, best fit over input voltage range | | ±5.2 | ±22.3 | LSB (2) |
| $B_{(CC\_DNL)}$ | Differential nonlinearity (1) | 16-bit, no missing codes | | 1 | | LSB (2) |
| $V_{(CC\_OFF)}$ | Offset error | 16-bit, uncalibrated | 1 | | 1 | LSB (2) |
| $V_{(CC\_OFF\_DRIFT)}$ | Offset error drift (1) | 16-bit, post-calibration | –0.0066 | | 0.0066 | LSB/°C (2) |
| $B_{(CC\_GAIN)}$ | Gain error (1) | 16-bit, over ideal input voltage range, post-calibration | –70 | | 70 | LSB (2) |
| $B_{(CC\_GAIN\_DRIFT)}$ | Gain error drift (1) | 16-bit, over ideal input voltage range, post-calibration | –1.2 | | 1.2 | LSB/°C (2) |
| $R_{(CC\_IN)}$ | Effective input resistance (3) | | 2 | | | MΩ |

(1) Specified by characterization.
(2) 1 LSB (16-bit mode, using CC1 filter) = $V_{REF2}$ / (5 x $2^{N-1}$) ≈ 1.24 / (5 x $2^{15}$) = 7.6 µV.
(3) Specified by design.

## 6.17 Coulomb Counter Digital Filter (CC1)

Typical values stated where $T_A$ = 25°C and $V_{BAT}$ = 37.0 V, min and max values stated where $T_A$ = -40°C to 85°C and $V_{BAT}$ = 4.7 V to 55 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{(CC1\_CONV\_FAST)}$ | Conversion-time | Single conversion (when operating from LFO in 262.144kHz mode) | | 250 | | ms |
| $t_{(CC1\_CONV\_SLOW)}$ | Conversion-time | Single conversion (when operating from LFO in 32.768kHz mode) | | 4 | | s |
| $B_{(CC1\_RSL)}$ | Code stability (1) (2) | Single conversion | 15 | | | bits |

(1) Code stability is defined as the resolution such that the data exhibits 3-sigma variation within ±1-LSB.
(2) Specified by a combination of design and production test.

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## 6.18 Current Measurement Digital Filter (CC2)

Typical values stated where $T_A$ = 25°C and $V_{BAT}$ = 37.0 V, min and max values stated where $T_A$ = -40°C to 85°C and $V_{BAT}$ = 4.7 V to 55 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{(CC2\_CONV)}$ | Conversion-time | Single conversion, in NORMAL mode, ***Settings:Configuration:Power Config[FASTADC]*** = 0 | | 2.93 | | ms |
| $t_{(CC2\_CONV\_FAST)}$ | Conversion-time in fast mode | Single conversion, in NORMAL mode, ***Settings:Configuration:Power Config[FASTADC]*** = 1 | | 1.46 | | ms |
| $B_{(CC2\_RES)}$ | Code stability(1) | Single conversion, in NORMAL mode, ***Settings:Configuration:Power Config[FASTADC]*** = 0 | 14 | 15 | | bits |
| $B_{(CC2\_RES\_FAST)}$ | Code stability in fast mode(1) | Single conversion, in NORMAL mode, ***Settings:Configuration:Power Config[FASTADC]*** = 1 | | 14 | | bits |

(1) Code stability is defined as the resolution such that the data exhibits 3-sigma variation within ±1-LSB.

## 6.19 Current Wake Detector

Typical values stated where $T_A$ = 25°C and $V_{BAT}$ = 37.0 V, min and max values stated where $T_A$ = -40°C to 85°C and $V_{BAT}$ = 4.7 V to 55 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{WAKE\_THR}$ | Wakeup voltage threshold error | $T_A$ = 25°C, $V_{WAKE} = V_{SRP} - V_{SRN}$, setting between ±0.5 mV and ±5 mV | - 200 | | 200 | µV |
| $V_{WAKE\_THR}$ | Wakeup voltage threshold error | $T_A$ = 25°C, $V_{WAKE} = V_{SRP} - V_{SRN}$, setting beyond ±5 mV | - 5 | | 5 | % of setting |
| $t_{WAKE}$ | Measurement interval | | | 12 | | ms |

## 6.20 Analog-to-Digital Converter

Typical values stated where $T_A$ = 25°C and $V_{BAT}$ = 37.0 V, min and max values stated where $T_A$ = -40°C to 85°C and $V_{BAT}$ = 4.7 V to 55 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{(ADC\_IN\_CELLS)}$ | Input voltage range (differential cell input mode)(1) | Internal reference (Vref = $V_{REF1}$) | –0.2 | | 5.5 | V |
| $V_{(ADC\_IN)}$ | Input voltage range (ADCIN measurement mode)(2) | Internal reference (Vref = $V_{REF1}$), applicable to ADCIN measurements using the TS1, TS2, TS3, ALERT, CFETOFF, DFETOFF, HDQ, DCHG, and DDSG pins | –0.2 | | $V_{REG18}$ | V |
| $V_{(ADC\_IN\_TS)}$ | Input voltage range (external thermistor measurement mode)(3) | Regulator reference (Vref = $V_{REG18}$), applicable to external thermistor measurements using the TS1, TS2, TS3, ALERT, CFETOFF, DFETOFF, HDQ, DCHG, and DDSG pins | –0.2 | | $V_{REG18}$ | V |
| $V_{(ADC\_IN\_DIV)}$ | Input voltage range (divider measurement mode)(4) | Internal reference (Vref = $V_{REF1}$), applicable to divider measurements using the VC10, PACK, and LD pins relative to VSS. | –0.2 | | 55 | V |
| $B_{(ADC\_INL)}$ | Integral nonlinearity (when using $V_{REF1}$ and differential cell voltage measurement mode at VC0 - VC9)(5) | 16-bit, best fit over -0.1 V to 5.5 V | –6.6 | | 6.6 | LSB(1) |
| | | 16-bit, best fit over -0.2 V to 0.2 V | –13.1 | | 13.1 | LSB(1) |

(1) The 16-bit LSB size of the differential cell voltage measurement is given by 1 LSB = 5 x $V_{REF1}$ / $2^{N-1}$ ≈ 5 x 1.215 V / $2^{15}$ = 185 µV.
(2) The 16-bit LSB size of the ADCIN voltage measurement is given by 1 LSB = 5 / 3 x $V_{REF1}$ / $2^{N-1}$ ≈ 5 / 3 x 1.215 V / $2^{15}$ = 62 µV.
(3) The LSB size of the external thermistor voltage measurement when reported in 32-bit format is given by 1 LSB = 5 / 3 x $V_{REG18}$ / $2^{N-1}$ ≈ 5 / 3 x 1.8 V / $2^{23}$ = 358 nV.
(4) The 16-bit LSB size of the divider voltage measurement is given by 1 LSB = 425 / 3 x $V_{REF1}$ / $2^{N-1}$ ≈ 425 / 3 x 1.215 / $2^{23}$ = 5.25 mV.
(5) Specified by characterization.

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## Analog-to-Digital Converter (continued)

Typical values stated where $T_A$ = 25°C and $V_{BAT}$ = 37.0 V, min and max values stated where $T_A$ = -40°C to 85°C and $V_{BAT}$ = 4.7 V to 55 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $B_{(ADC\_DNL)}$ | Differential nonlinearity(5) | 16-bit, no missing codes, using differential cell voltage measurement at VC10-VC9 | | 1 | | LSB(1) |
| $B_{(ADC\_OFF\_CELL)}$ | Differential cell offset error | 16-bit, uncalibrated, using VC10 - VC9 | –2.6 | 1.3 | 2.6 | LSB(1) |
| $B_{(ADC\_OFF)}$ | ADCIN offset error | 16-bit, uncalibrated, using ADCIN mode on TS1 pin | | TBD | | LSB(2) |
| $B_{(ADC\_OFF\_DIV)}$ | Divider offset error | 16-bit, uncalibrated, using divider mode on PACK pin | | TBD | | LSB(4) |
| $B_{(ADC\_OFF\_DRIFT\_CELL)}$ | Differential cell offset error drift(5) | 16-bit, post-calibration, using VC10 - VC9 | | 0.04 | 0.07 | LSB/°C(1) |
| $B_{(ADC\_GAIN\_ERR)}$ | Gain error | 16-bit, over ideal input voltage range, differential cell input mode on VC10-VC9, uncalibrated | –492 | 131 | 492 | LSB(1) |
| $B_{(ADC\_GAIN\_DRIFT)}$ | Gain error drift(5) | 16-bit, over ideal input voltage range, differential cell input mode on VC10-VC9, uncalibrated | | TBD | TBD | LSB/°C(1) |
| $R_{(ADC\_IN\_CELL)}$ | Effective input resistance(6) | Differential cell input mode on VC10-VC9 | 8 | | | MΩ |
| $R_{(ADC\_IN\_LD)}$ | Effective input resistance | Divider measurement on LD pin | | 2 | | MΩ |
| $R_{(ADC\_IN\_DIV)}$ | Effective input resistance | Divider measurement on VC10 and PACK pins | | 600 | | kΩ |
| $B_{(ADC\_RES)}$ | Code stability(7) | Single conversion, in NORMAL mode, ***Settings:Configuration:Power Config[FASTADC]*** = 0 | 14 | 15 | | bits |
| $B_{(ADC\_RES\_FAST)}$ | Code stability in fast mode(7) | Single conversion, in NORMAL mode, ***Settings:Configuration:Power Config[FASTADC]*** = 1 | | 14 | | bits |
| $t_{(ADC\_CONV)}$ | Conversion-time | Single conversion, in NORMAL mode, ***Settings:Configuration:Power Config[FASTADC]*** = 0 | | 2.93 | | ms |
| $t_{(ADC\_CONV\_FAST)}$ | Conversion-time in fast mode | Single conversion, in NORMAL mode, ***Settings:Configuration:Power Config[FASTADC]*** = 1 | | 1.46 | | ms |

(6) While the voltage ADC is measuring a differential cell input voltage, a bias current of approximately 2 µA will flow through the cell input being measured, in addition to the current associated with the effective ADC input resistance.
(7) Code stability is defined as the resolution such that the data exhibits 3-sigma variation within ±1-LSB.

## 6.21 Cell Balancing

Typical values stated where $T_A$ = 25°C and $V_{BAT}$ = 37.0 V, min and max values stated where $T_A$ = -40°C to 85°C and $V_{BAT}$ = 4.7 V to 55 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $R_{(CB)}$ | Internal cell balancing resistance(1) | $R_{DS(ON)}$ for internal FET switch at 2V < $V_{CELL}$ < 5.5V, $V_{BAT}$ ≥ 4.7 V | 15 | 25 | 45 | Ω |

(1) Cell balancing must be controlled to limit the current based on the absolute maximum allowed current, and to avoid exceeding the recommended device operating temperature. This can be accomplished by appropriate sizing of the offchip cell input resistors and limiting the number of cells that can be balanced simultaneously.

## 6.22 Cell Open Wire Detector

Typical values stated where $T_A$ = 25°C and $V_{BAT}$ = 37.0 V, min/max values stated where $T_A$ = -40°C to 85°C and $V_{BAT}$ = 4.7 V to 55 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{(OW)}$ | Internal cell open wire check current from VCx pin to VSS, 1 ≤ x ≤ 10 | VCx > VSS + 0.8 V, 1 ≤ x ≤ 4; VCx > VSS + 2.8 V, 5 ≤ x ≤ 10 | 22 | 55 | 95 | µA |

## 6.23 Internal Temperature Sensor

Typical values stated where $T_A$ = 25°C and $V_{BAT}$ = 37.0 V, min and max values stated where $T_A$ = -40°C to 85°C and $V_{BAT}$ = 4.7 V to 55 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{(TEMP)}$ | Internal temperature sensor voltage drift(1) | $\Delta V_{BE}$ measurement | 0.405 | 0.410 | 0.419 | mV/°C |

(1) Specified by design.

## 6.24 Thermistor Measurement

Typical values stated where $T_A$ = 25°C and $V_{BAT}$ = 37.0 V, min and max values stated where $T_A$ = -40°C to 85°C and $V_{BAT}$ = 4.7 V to 55 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $R_{(TS\_PU)}$ | Internal pullup resistance(1) | Setting for nominal 18-kΩ | 14.4 | 18 | 21.6 | kΩ |
| | | Setting for nominal 180-kΩ | 144 | 180 | 216 | kΩ |
| $R_{(TS\_PAD)}$ | Internal pad resistance(2) | | | 500 | | Ω |
| $R_{(TS\_PU\_DRIFT)}$ | Internal pullup resistance change over temperature(3) | Change over -40°C/+85°C vs value at 25°C for nominal 18-kΩ | | ±200 | | Ω |
| | | Change over -40°C/+85°C vs value at 25°C for nominal 180-kΩ | | ±2000 | | Ω |

(1) The internal pullup resistance includes only the resistance between the REG18 pin and the point where the voltage is sensed by the ADC.
(2) The internal pad resistance includes the resistance between the point where the voltage is sensed by the ADC and the pin where an external thermistor is attached (which includes the TS1, TS2, TS3, ALERT, CFETOFF, DFETOFF, HDQ, DCHG, and DDSG pins).
(3) Specified by characterization.

## 6.25 Internal Oscillators

Typical values stated where $T_A$ = 25°C and $V_{BAT}$ = 37.0 V, min and max values stated where $T_A$ = -40°C to 85°C and $V_{BAT}$ = 4.7 V to 55 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **High-frequency Oscillator** | | | | | | |
| $f_{HFO}$ | Operating frequency | | | 16.78 | | MHz |
| $f_{HFO(ERR)}$ | Frequency error | $T_A$ = -20°C to +70°C, includes frequency drift | –3.0 | ±0.25 | 3.0 | % |
| | | $T_A$ = -40°C to +85°C, includes frequency drift | –4.0 | ±0.25 | 4.0 | % |
| $f_{HFO(SU)}$ | Start-up time(1) | $T_A$ = -20°C to +85°C, at power-up from SHUTDOWN or exiting DEEPSLEEP mode, oscillator frequency within ±3% of nominal | | | 4 | ms |
| | | $T_A$ = -20°C to +85°C, cases other than power-up from SHUTDOWN or exiting DEEPSLEEP mode, oscillator frequency within ±3% of nominal | | | 120 | µs |
| **Low-frequency Oscillator** | | | | | | |
| $f_{LFO}$ | Operating frequency | Full-speed setting | | 262.144 | | kHz |
| | | Low speed setting | | 32.768 | | kHz |
| $f_{LFO(ERR)}$ | Frequency error | $T_A$ = -20°C to +70°C, includes frequency drift | –1.5 | ±0.25 | 1.5 | % |
| | | $T_A$ = -40°C to +85°C, includes frequency drift | –2.5 | ±0.25 | 2.5 | % |
| $f_{LFO(FAIL)}$ | Failure detection frequency | Detects oscillator failure if the LFO frequency falls below this level. | 9 | 12 | 16 | kHz |

(1) Specified by design.

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## 6.26 High-side NFET Drivers

Typical values stated where $T_A$ = 25°C and $V_{BAT}$ = 37.0 V, min and max values stated where $T_A$ = -40°C to 85°C and $V_{BAT}$ = 4.7 V to 55 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{(FETON\_HI)}$ | CHG pin voltage with respect to BAT, DSG pin voltage with respect to BAT, $V_{LD} \le V_{DSG}$ (1) | CHG/DSG $C_L$ = 20 nF, charge pump high overdrive setting | 10 | 11 | 12 | V |
| $V_{(FETON\_LO)}$ | CHG pin voltage with respect to BAT, DSG pin voltage with respect to BAT, $V_{LD} \le V_{DSG}$ (1) | CHG/DSG $C_L$ = 20 nF, charge pump low overdrive setting | 5 | 5.5 | 6 | V |
| $V_{(SRCFOL\_FETON)}$ | DSG on voltage with respect to BAT | CHG/DSG $C_L$ = 20 nF, source follower mode | | 0 | | V |
| $V_{(CHGFETOFF)}$ | CHG off voltage with respect to BAT | CHG/DSG $C_L$ = 20 nF, steady state value | | | 0.4 | V |
| $V_{(DSGFETOFF)}$ | DSG off voltage with respect to LD | CHG/DSG $C_L$ = 20 nF, steady state value | | | 0.7 | V |
| $t_{(FET\_ON)}$ | CHG and DSG rise time | CHG/DSG $C_L$ = 20 nF, $R_{GATE}$ = 100 Ω, 0 V to 4 V gate-source overdrive, charge pump mode | | 30 | 50 | µs |
| $t_{(CHGFETOFF)}$ | CHG fall time to BAT | CHG $C_L$ = 20 nF, $R_{GATE}$ = 100 Ω, 90% to 10% of $V_{(FETON)}$ | | 20 | 40 | µs |
| $t_{(DSGFETOFF)}$ | DSG fall time to LD | DSG $C_L$ = 20 nF, $R_{GATE}$ = 100 Ω, 90% to 10% of $V_{(FETON)}$ | | 7 | 20 | µs |
| $t_{(CP\_START)}$ | Charge pump start up time | $C_L$ = 20 nF, $C_{(CP1)}$ = 470 nF, 10% to 90% of $V_{(FETON)}$ | | | 100 | ms |
| $C_{(CP1)}$ | Charge pump capacitor (2) | | 100 | 470 | 2200 | nF |

(1) When DSG is enabled and $V_{LD} > V_{DSG}$, $V_{DSG}$ will rise to ≈ $V_{LD}$ - 0.7 V.
(2) Specified by design.

## 6.27 Comparator-Based Protection Subsystem

Typical values stated where $T_A$ = 25°C and $V_{BAT}$ = 37.0 V, min and max values stated where $T_A$ = -40°C to 85°C and $V_{BAT}$ = 4.7 V to 55 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{(OVP)}$ | Overvoltage detection range | Nominal setting (50 mV steps) | | 1.0 V to 5.5 V in 50 mV steps | | V |
| $V_{(OVP\_ACC)}$ | Overvoltage detection voltage threshold accuracy | $T_A$ = +25°C, nominal setting between 1.0 V and 5.5 V | | TBD | | mV |
| | | $T_A$ = +25°C, nominal setting between 3.0 V and 5.0 V | –10 | | 10 | mV |
| | | $T_A$ = 0°C to +60°C, nominal setting between 1.0 V and 5.5 V | | TBD | | mV |
| | | $T_A$ = 0°C to +60°C, nominal setting between 3.0 V and 5.0 V | –15 | | 15 | mV |
| | | $T_A$ = -40°C to +85°C, nominal setting between 1.0 V and 5.5 V | | TBD | | mV |
| | | $T_A$ = -40°C to +85°C, nominal setting between 3.0 V and 5.0 V | –25 | | 25 | mV |
| $V_{(OVP\_DLY)}$ | Overvoltage detection delay (1) | Nominal setting (3.3 ms steps) | | 10 ms to 6753 ms in 3.3 ms steps | | ms |

(1) Cell balancing not active. Timing of overvoltage and undervoltage protection checks is modified when cell balancing is in progress.

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## Comparator-Based Protection Subsystem (continued)

Typical values stated where $T_A$ = 25°C and $V_{BAT}$ = 37.0 V, min and max values stated where $T_A$ = -40°C to 85°C and $V_{BAT}$ = 4.7 V to 55 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{(UVP)}$ | Undervoltage detection range | Nominal setting (50 mV steps) | | 1.0 V to 4.5 V in 50 mV steps | | V |
| $V_{(UVP\_ACC)}$ | Undervoltage detection voltage threshold accuracy | $T_A$ = +25°C, nominal setting between 1.0 V and 4.5 V | | TBD | | mV |
| | | $T_A$ = +25°C, nominal setting between 1.5 V and 3.5 V | –10 | | 10 | mV |
| | | $T_A$ = 0°C to +60°C, nominal setting between 1.0 V and 4.5 V | | TBD | | mV |
| | | $T_A$ = 0°C to +60°C, nominal setting between 1.5 V and 3.5 V | –15 | | 15 | mV |
| | | $T_A$ = -40°C to +85°C, nominal setting between 1.0 V and 4.5 V | | TBD | | mV |
| | | $T_A$ = -40°C to +85°C, nominal setting between 1.5 V and 3.5 V | –25 | | 25 | mV |
| $V_{(UVP\_DLY)}$ | Undervoltage detection delay(1) | Nominal setting (3.3 ms steps) | | 10 ms to 6753 ms in 3.3 ms steps | | ms |
| $V_{(SCD)}$ | Short circuit in discharge voltage threshold range | Nominal settings, threshold based on $V_{SRP}$ - $V_{SRN}$ | | –10, –20, –40, –60, –80, –100, –125, –150, –175, –200, –250, –300, –350, –400, –450, –500 | | mV |
| $V_{(SCD\_ACC)}$ | Short circuit in discharge voltage threshold detection accuracy | $T_A$ = 0°C to +60°C | –10 | | 10 | % of nominal threshold |
| | | $T_A$ = -40°C to +85°C | –15 | | 15 | % of nominal threshold |
| $V_{(SCD\_DLY)}$ | Short circuit in discharge detection delay | Fastest setting (with 3 mV overdrive) | 5 | 8 | 11 | µs |
| | | Fastest setting (with 25 mV overdrive) | 400 | | 800 | ns |
| | | Setting for 15 µs (with 3 mV overdrive) | 15 | 20 | 25 | µs |
| | | Setting for 15 µs (with 25 mV overdrive) | 10 | 15 | 20 | µs |
| | | Settings for 50 µs | 40 | 50 | 60 | µs |
| | | Setting for 100 µs | 90 | 100 | 110 | µs |
| | | Setting for 200 µs | 180 | 200 | 220 | µs |
| | | Setting for 400 µs | 360 | 400 | 440 | µs |
| $V_{(OCC)}$ | Overcurrent in charge (OCC) voltage threshold range | Nominal settings, threshold based on $V_{SRP}$ - $V_{SRN}$ | | 4 mV to 124 mV in 2 mV steps | | mV |

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## Comparator-Based Protection Subsystem (continued)

Typical values stated where $T_A$ = 25°C and $V_{BAT}$ = 37.0 V, min and max values stated where $T_A$ = -40°C to 85°C and $V_{BAT}$ = 4.7 V to 55 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{(OCD)}$ | Overcurrent in discharge (OCD1, OCD2) voltage threshold ranges | Nominal settings, thresholds based on $V_{SRP}$ - $V_{SRN}$ | | –4 mV to –200 mV in 4 mV steps | | mV |
| $V_{(OC\_ACC)}$ | Overcurrent (OCC, OCD1, OCD2) detection voltage threshold accuracy | \|Setting\| < 20 mV | –1 | | 1 | mV |
| | | \|Setting\| = 20 mV ~ 56 mV | –3 | | 3 | mV |
| | | \|Setting\| = 56 mV ~ 100 mV | –5 | | 5 | mV |
| | | \|Setting\| > 100 mV | –5 | | 5 | mV |
| $V_{(OC\_DLY)}$ | Overcurrent (OCC, OCD1, OCD2) detection delay (independent delay setting for each protection) | Nominal setting (3.3 ms steps) | | 10 ms to 425 ms in 3.3 ms steps | | ms |

## 6.28 Timing Requirements - I²C Interface, 100kHz Mode

Typical values stated where $T_A$ = 25°C and $V_{BAT}$ = 37.0 V, min and max values stated where $T_A$ = -40°C to 85°C and $V_{BAT}$ = 4.7 V to 55 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{SCL}$ | Clock operating frequency | SCL duty cycle = 50% | | | 100 | kHz |
| $t_{HD:STA}$ | START condition hold time | | 4.0 | | | µs |
| $t_{LOW}$ | Low period of the SCL clock | | 4.7 | | | µs |
| $t_{HIGH}$ | High period of the SCL clock | | 4.0 | | | µs |
| $t_{SU:STA}$ | Setup repeated START | | 4.7 | | | µs |
| $t_{HD:DAT}$ | Data hold time (SDA input) | | 0 | | | ns |
| $t_{SU:DAT}$ | Data setup time (SDA input) | | 250 | | | ns |
| $t_r$ | Clock rise time | 10% to 90% | | | 1000 | ns |
| $t_f$ | Clock fall time | 90% to 10% | | | 300 | ns |
| $t_{SU:STO}$ | Setup time STOP condition | | 4.0 | | | µs |
| $t_{BUF}$ | Bus free time STOP to START | | 4.7 | | | µs |
| $t_{RST}$ | I²C bus reset | Bus interface is reset if SCL is detected low for this duration | 1.9 | | 2.1 | s |
| $R_{PULLUP}$ | Pullup resistor(1) | Pullup voltage rail ≤ 5 V | 1.1 | | | kΩ |

(1) Specified by characterization.

## 6.29 Timing Requirements - I²C Interface, 400kHz Mode

Typical values stated where $T_A$ = 25°C and $V_{BAT}$ = 37.0 V, min and max values stated where $T_A$ = -40°C to 85°C and $V_{BAT}$ = 4.7 V to 55 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{SCL}$ | Clock operating frequency | SCL duty cycle = 50% | | | 400 | kHz |
| $t_{HD:STA}$ | START condition hold time | | 0.6 | | | µs |
| $t_{LOW}$ | Low period of the SCL clock | | 1.3 | | | µs |
| $t_{HIGH}$ | High period of the SCL clock | | 600 | | | ns |
| $t_{SU:STA}$ | Setup repeated START | | 600 | | | ns |
| $t_{HD:DAT}$ | Data hold time (SDA input) | | 0 | | | ns |
| $t_{SU:DAT}$ | Data setup time (SDA input) | | 100 | | | ns |
| $t_r$ | Clock rise time | 10% to 90% | | | 300 | ns |
| $t_f$ | Clock fall time | 90% to 10% | | | 300 | ns |
| $t_{SU:STO}$ | Setup time STOP condition | | 0.6 | | | µs |

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### Timing Requirements - I²C Interface, 400kHz Mode (continued)

Typical values stated where $T_A$ = 25°C and $V_{BAT}$ = 37.0 V, min and max values stated where $T_A$ = -40°C to 85°C and $V_{BAT}$ = 4.7 V to 55 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{BUF}$ | Bus free time STOP to START | | 1.3 | | | µs |
| $t_{RST}$ | $I^2C$ bus reset | Bus interface is reset if SCL is detected low for this duration | 1.9 | | 2.1 | s |
| $R_{PULLUP}$ | Pullup resistor(1) | Pullup voltage rail ≤ 5 V | 1.1 | | | kΩ |

(1) Specified by characterization.

## 6.30 Timing Requirements - HDQ Interface

Typical values stated where $T_A$ = 25°C and $V_{BAT}$ = 37.0 V, min and max values stated where $T_A$ = -40°C to 85°C and $V_{BAT}$ = 4.7 V to 55 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_B$ | Break Time | | 190 | | | µs |
| $t_{BR}$ | Break Recovery Time | | 40 | | | µs |
| $t_{HW1}$ | Host Write 1 Time | Host drives HDQ | 0.5 | | 50 | µs |
| $t_{HW0}$ | Host Write 0 Time | Host drives HDQ | 86 | | 145 | µs |
| $t_{CYCH}$ | Cycle Time, Host to device | Device drives HDQ | 190 | | | µs |
| $t_{CYCD}$ | Cycle Time, device to Host | Device drives HDQ | 190 | 205 | 250 | µs |
| $t_{DW1}$ | Device Write 1 Time | Device drives HDQ | 32 | | 50 | µs |
| $t_{DW0}$ | Device Write 0 Time | Device drives HDQ | 80 | | 145 | µs |
| $t_{RSPS}$ | Device Response Time | Device drives HDQ | 190 | | 950 | µs |
| $t_{TRND}$ | Host Turn Around Time | Host drives HDQ after device drives HDQ | 210 | | | µs |
| $t_{RISE}$ | HDQ Line Rising Time to Logic 1 | | | | 1.8 | µs |
| $t_{RST}$ | HDQ Bus Reset | Host holds bus low to initiate device interface reset | 1.9 | | 2.1 | s |
| $R_{PULLUP}$ | Pullup Resistor(1) | Pullup voltage rail ≤ 5 V | 1.1 | | | kΩ |

(1) Specified by characterization.

## 6.31 Timing Requirements - SPI Interface

Typical values stated where $T_A$ = 25°C and $V_{BAT}$ = 37.0 V, min and max values stated where $T_A$ = -40°C to 85°C and $V_{BAT}$ = 4.7 V to 55 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{SCK}$ | SPI clock period | | 500 | | | ns |
| $t_{LEAD}$ | Enable lead-time | | 625 | | | ns |
| $t_{LAG}$ | Enable lag time | | 50 | | | ns |
| $t_{TD}$ | Sequential transfer delay | | TBD | | | ns |
| $t_{SU}$ | Data setup time | | 50 | | | ns |
| $t_{HI}$ | Data hold time (inputs) | | 50 | | | ns |
| $t_{HO}$ | Data hold time (outputs) | | 0 | | | ns |
| $t_A$ | Slave access time | | | | 50 | ns |
| $t_{DIS}$ | Slave DOUT disable time | | | | 50 | ns |
| $t_V$ | Data valid | | | | 50 | ns |
| $t_R$ | Rise time(1) | Up to 25pF load | | | 30 | ns |

(1) Specified by characterization.

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## Timing Requirements - SPI Interface (continued)

Typical values stated where $T_A$ = 25°C and $V_{BAT}$ = 37.0 V, min and max values stated where $T_A$ = -40°C to 85°C and $V_{BAT}$ = 4.7 V to 55 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_F$ | Fall time(1) | Up to 25pF load | | | 30 | ns |
| $t_{INF}$ | Pulse width of input spikes suppressed | | | | 200 | ns |
| $t_{RST}$ | SPI bus reset | Bus interface is reset if SPI_CS is low and SPI_SCLK is detected unchanged for this duration | 1.9 | | 2.1 | s |

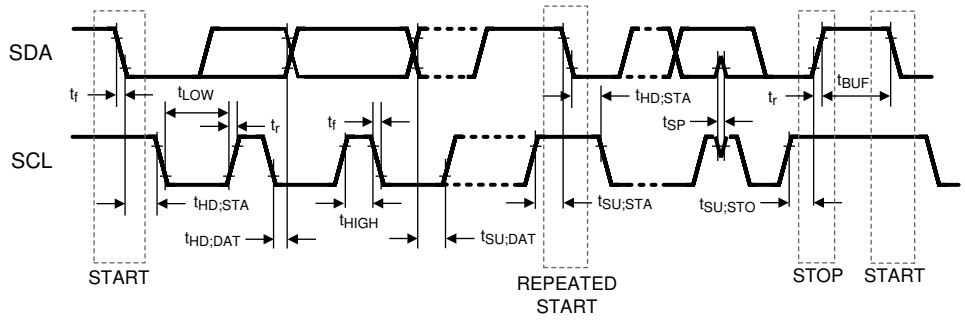


**Figure 1. I²C interface timing**

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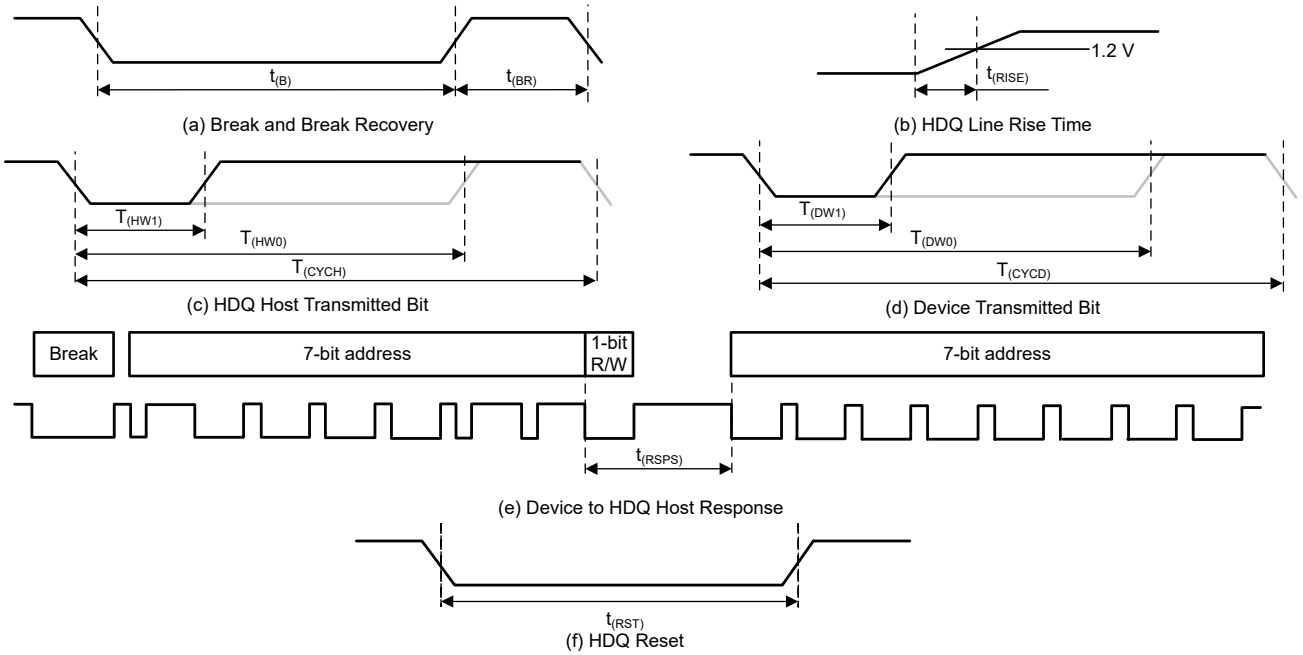


a. HDQ Breaking
b. Rise time of HDQ line
c. HDQ Host to Device communication
d. Device to HDQ Host communication
e. Device to HDQ Host response format
f. HDQ Host to Device

**Figure 2. HDQ interface bus timing**

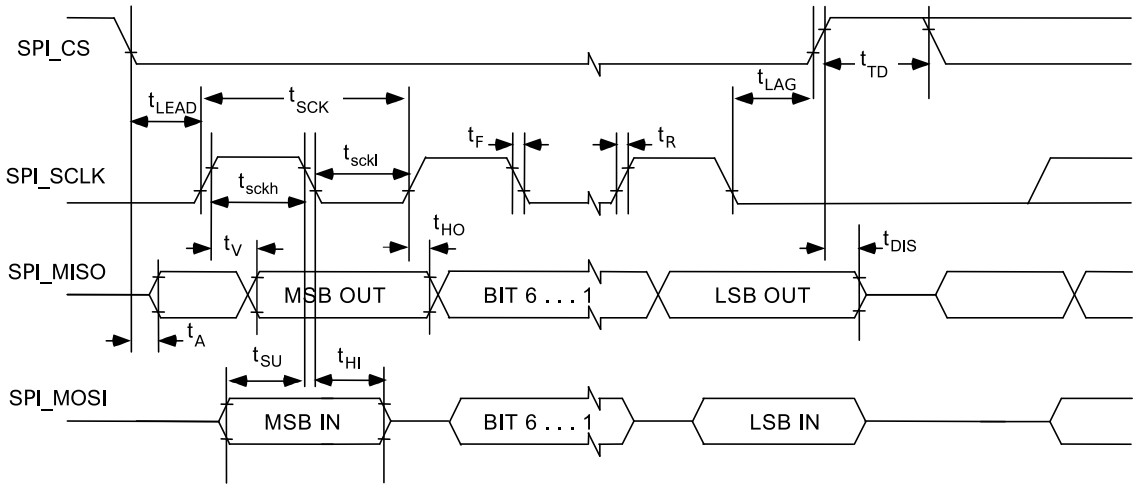


**Figure 3. SPI interface bus timing**

ADVANCE INFORMATION

# 7 Detailed Description

## 7.1 Overview

The BQ76942 product is a highly integrated, accurate battery monitor and protector for 3-series to 10-series Li-Ion, Li-Polymer, and LiFePO4 battery packs. A high accuracy voltage, current, and temperature measurement accuracy provides data for host-based algorithms and control. A feature-rich and highly configurable protection subsystem provides a wide set of protections which can be triggered and recovered completely autonomously by the device or under full control of a host processor. The integrated charge pump with high-side protection NFET drivers allows host communication with the device even when FETs are off by preserving the ground connection to the pack. Dual programmable LDOs are included for external system use, with each independently programmable to voltages of 1.8 V, 2.5 V, 3.0 V, 3.3 V, and 5.0 V, capable of providing up to 50 mA each.

The BQ76942 device includes one-time-programmable (OTP) memory for customers to setup device operation on their own production line. Multiple communications interfaces are supported, including 400-kHz $I^2C$, SPI, and HDQ one-wire standards. Multiple digital control and status data are available through several multifunction pins on the device, including an interrupt to the host processor, and independent controls for host override of each high-side protection NFET. Three dedicated pins are provided for temperature measurement using external thermistors, and multifunction pins can be programmed to use for additional thermistors, supporting a total of up to 9 thermistors, in addition to an internal die temperature measurement. The following sections detail the major component blocks of the BQ76942 device.

## 7.2 Functional Block Diagram

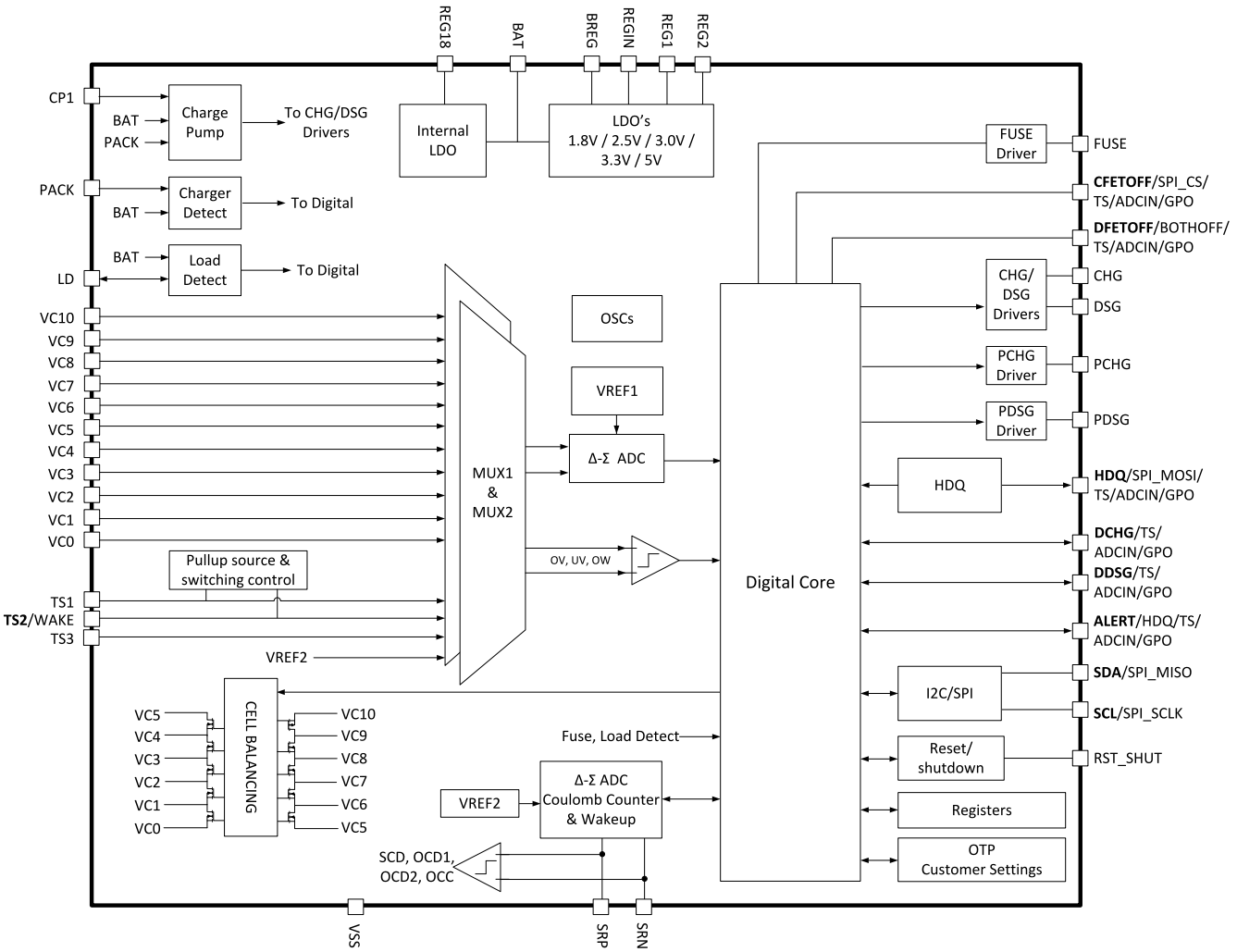


**Figure 4. Block Diagram of the BQ76942**

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## 7.3 Feature Description

### 7.3.1 Device Configuration - Direct Commands and Subcommands

The BQ76942 device includes support for direct commands and subcommands. The direct commands are accessed using a 7-bit command address that is sent from a host through the device serial communications interface and either triggers an action, or provides a data value to be written to the device, or instructs the device to report data back to the host. Subcommands are additional commands that are accessed indirectly using the 7-bit command address space and provide capability for block data transfers. When a subcommand is initiated, a 16-bit subcommand address is first written to the 7-bit command addresses 0x3E (lower byte) and 0x3F (upper byte). The device initially assumes a read-back of data may be needed, and auto-populates existing data into the 32-byte transfer buffer (which uses 7-bit command addresses 0x40 - 0x5F), and writes the checksum for this data into address 0x60. If the host instead intends to write data into the device, the host will overwrite the new data into the transfer buffer, a checksum for the data into address 0x60, and the data length into address 0x61. As soon as address 0x61 is written, the device checks the checksum written into 0x60 with the data written into 0x40-0x5F, and if this is correct, it proceeds to transfer the data from the transfer buffer into the device's memory. The checksum is the 8-bit sum of the subcommand bytes (0x3E and 0x3F) plus the number of bytes

## Feature Description (continued)

used in the transfer buffer, then this result is bitwise inverted. The verification cannot take place until the data length is written, so the device realizes how many bytes in the transfer buffer are included. The checksum and data length must be written together as a word to be valid. The data length includes the two bytes in 0x3E and 0x3F, the two bytes in 0x60 and 0x61, and the length of the transfer buffer. Therefore, if the entire 32-byte transfer buffer is used, the data length will be 0x24.

Some subcommands are only to initiate an action and do not involve sending or receiving data. In these cases, the host can simply write the subcommand into 0x3E and 0x3F, it is not necessary to write the length and checksum or any further data.

The commands supported in the device are described in Commands and Subcommands. Single-byte commands are direct commands, while two-byte commands are subcommands. Data formats are described in Data Formats

To read data from a subcommand, the most efficient approach (to minimize bus traffic) is shown below:

1. Write lower byte of subcommand to 0x3E.
2. Write upper byte of subcommand to 0x3F.
3. Read 0x3E and 0x3F. If this returns 0xFF, this indicates the subcommand has not completed operation yet. When the subcommand has completed, the readback will return what was originally written. Continue reading 0x3E and 0x3F until it returns what was written originally. Note: this response only applies to subcommands that return data to be read back.
4. Read the length of response from 0x61.
5. Read buffer starting at 0x40 for the expected length.
6. Read the checksum at 0x60 and verify it matches the data read.

An easier approach that is less efficient on bus traffic is:

1. Write lower byte of subcommand to 0x3E.
2. Write upper byte of subcommand to 0x3F.
3. Read 0x3E and 0x3F. If this returns 0xFF, this indicates the subcommand has not completed operation yet. When the subcommand has completed, the readback will return what was originally written. Continue reading 0x3E and 0x3F until it returns what was written originally. Note: this response only applies to subcommands that return data to be read back.
4. Read 0x40 to 0x61 in a block. Ensure the checksum at 0x60 is correct over the length designated by 0x61. This means sometimes more bytes are read than necessary, but it also makes it possible to use a standard function that can be called for all subcommands.

Note: 0x61 provides the length of the buffer data plus 4 (that is, length of the buffer data plus the length of 0x3E and 0x3F plus the length of 0x60 and 0x61).

The checksum is calculated over 0x3E, 0x3F, and the buffer data, it does not include the checksum or length in 0x60 and 0x61.

If the checksum and length are read together, this can trigger an auto increment in some cases, in which case the buffer will be populated with another block's data. So, generally the checksum and length should not be read together unless the buffer has already been read, or if auto incrementing is intended.

### 7.3.2 Device Memory

#### *7.3.2.1 Configuration Using OTP or Registers*

The BQ76942 device includes registers, which are stored in the RAM, and are integrated in one-time programmable (OTP) memory. At initial power-up, the device loads OTP settings into registers, which are used by the device firmware during operation. The device can also perform a reset on demand if the *0x0012 RESET()* or *0x0041 RESET()* subcommands are sent (these have identical functionality). The recommended procedure is for the customer to write settings into OTP on the manufacturing line, in which case the device will use these settings whenever it is powered up. Alternatively, the host processor can initialize registers after power-up, without using the OTP memory, but the registers will need to be re-initialized after each power cycle of the device. Register values are preserved while the device is in NORMAL, SLEEP, or DEEPSLEEP modes. If the device enters SHUTDOWN mode, all register memory is cleared, and the device will return to default parameters when powered again.

## Feature Description (continued)

The OTP memory in the BQ76942 device is initially all-zeros, each bit can be left as a "0" or written to a "1," but cannot be written from a "1" back to a "0." The OTP memory includes two full images of the Data Memory configuration settings. At power-up, the device will XOR each setting in the first OTP image with the corresponding setting in the second OTP image and with the default value for the corresponding setting, with the resulting value stored into the RAM register for use during operation. This allows any setting to be changed from the default value using the first image, then changed back to the default once using the second image. The OTP memory also includes a 16-bit signature, which is calculated over most of the settings and stored in OTP. When the device is powered up, it will read the OTP settings and check that the signature matches that stored, to provide robustness against bit errors in reading or corruption of the memory. If a signature error is detected, the device will boot into the default configuration (as if the OTP is cleared). The device supports up to 8 different signature values, so up to 8 partial changes in OTP can be made, with the signature updated accordingly.

The OTP memory is typically written after the device is assembled onto the PCB, but before cells are attached to the board. Programming the OTP memory requires a voltage of approximately 12 V applied on the BAT pin, and the temperature to be within allowed limits. All configuration settings are then loaded into registers using the serial communication interface (see Serial Communications Interfaces). The *0x00A0 OTP_WR_CHECK()* subcommand can be sent to initiate a self-check whether OTP writing can be accomplished. The device must be in FULLACCESS and CONFIG_UPDATE mode when this subcommand is sent. The device returns information as shown below.

**Table 1. *0x00A0 OTP_WR_CHECK()* Bit Definitions**

| Byte-0 | | |
|---|---|---|
| **Bit** | **Name** | **Description** |
| 7 | Programming OK | If this bit is set, conditions are met for programming, and none of the remaining bits in this byte will be set. |
| 6 | Locked | The device is not in FULLACCESS and CONFIG_UPDATE mode, or the OTP Lock bit has been set to prevent further modification |
| 5 | Reserved | |
| 4 | No_SIG | Signature cannot be written (indicating the signature has already been written too many times) |
| 3 | No_DATA | Could not program data (indicating data has been programmed too many times, no XOR bits left) |
| 2 | HighTemp | The measured internal temperature is above the allowed OTP programming temperature range |
| 1 | LowVoltage | The measured stack voltage is below the allowed OTP programming voltage |
| 0 | HighVoltage | The measured stack voltage is above the allowed OTP programming voltage |
| **Bytes-1,2** | | |
| If byte-0, bit-3 is set, then byte-1 and byte-2 will contain the LSB and MSB of the address of the first data value which could not be programmed. | | |

If the self-check is successful, then the actual OTP write can be initiated by sending the *0x00A1 OTP_WRITE()* subcommand. This subcommand provides the same feedback as the *0x00A0 OTP_WR_CHECK()* subcommand above, with byte-0, bit-7 being set if programming completed successfully.

### 7.3.3 Measurement System

#### *7.3.3.1 Voltage Measurement*

The BQ76942 device integrates a voltage ADC which is multiplexed between measurements of cell voltages, an internal temperature sensor, up to 9 external thermistors, and also performs measurements of the voltage at the VC10 pin, the PACK pin, the LD pin, the internal Vref used by the coulomb counter, and the VSS rail (for diagnostic purposes). The BQ76942 device supports measurement of individual differential cell voltages in a series configuration, ranging from 3 series cells to 10 series cells. Each cell voltage measurement is a differential measurement of the voltage between two adjacent cell input pins, such as VC1-VC0, VC2-VC1, and so forth. The cell voltage measurements are processed based on trim and calibration corrections, and then reported in 16-

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bit resolution using units of 1 mV. The raw 24-bit digital output of the ADC is also available for readout using 32-bit subcommands. The cell voltage measurements can support a recommended voltage range from -0.2 V to 5.5 V. The voltage ADC saturates at a level of 5 × VREF1 (approximately 6.25 V) when measuring cell voltages, although for best performance it is recommended to stay at a maximum input of 5.5 V. The 16-bit cell and VC10 (Stack), PACK, and LD pin voltage measurements are available by using the commands listed below.

**Table 2. Commands to read 16-bit voltage measurements**

| Command | Name | Unit |
|---|---|---|
| 0x14 and 0x15 | Cell 1 Voltage | mV |
| 0x16 and 0x17 | Cell 2 Voltage | mV |
| 0x18 and 0x19 | Cell 3 Voltage | mV |
| 0x1A and 0x1B | Cell 4 Voltage | mV |
| 0x1C and 0x1D | Cell 5 Voltage | mV |
| 0x1E and 0x1F | Cell 6 Voltage | mV |
| 0x20 and 0x21 | Cell 7 Voltage | mV |
| 0x22 and 0x23 | Cell 8 Voltage | mV |
| 0x24 and 0x25 | Cell 9 Voltage | mV |
| 0x26 and 0x27 | Cell 10 Voltage | mV |
| 0x34 and 0x35 | Stack (VC10 pin) voltage | userV |
| 0x36 and 0x37 | PACK pin voltage | userV |
| 0x38 and 0x39 | LD pin voltage | userV |



#### 7.3.3.1.1 Voltage Measurement Schedule

The BQ76942 device's voltage measurements are taken in a measurement loop that consists of multiple measurement slots. All 10 cell voltages are measured on each loop, then one slot is used for one of the VC10 or PACK or LD pin voltages, one slot is used for internal temperature or Vref or VSS measurement, then up to three slots are used to measure thermistors or multifunction pin voltages (ADCIN functionality). Over the course of three loops, a full set of measurements is completed. One measurement loop consists of either 12 (if no thermistors or ADCIN are enabled), 13 (if one thermistor or ADCIN is enabled), 14 (if two thermistors or ADCIN are enabled), or 15 (if three or more thermistors or ADCIN are enabled) measurement slots.

The speed of a measurement loop can be controlled by settings. Each voltage measurement (slot) takes 3 ms (or 1.5 ms if ***Settings:Configuration:Power Config:FASTADC*** is set), so a typical measurement loop with 15 slots per loop takes 45 ms (or 22.5 ms if ***Settings:Configuration:Power Config:FASTADC*** is set). If measurement data is not required as quickly, the timing for the measurement loop can be programmed to slower speeds, which injects idle slots in each loop after the measurement slots. Using slower loop cycle time will reduce the power dissipation of the device when in NORMAL mode. This is set using the ***Settings:Configuration:Power Config:LOOP_SLOW_0*** and ***LOOP_SLOW_1*** configuration bits, as shown below.

**Table 3. Voltage measurement schedule**

| LOOP_SLOW_1 | LOOP_SLOW_0 | Measurement Loop Cycle Time |
|---|---|---|
| 0 | 0 | 45 ms |
| 0 | 1 | 90 ms |
| 1 | 0 | 180 ms |
| 1 | 1 | 360 ms |

#### 7.3.3.1.2 Usage of VC Pins for Cells Versus Interconnect

If the BQ76942 device is used in a system with fewer than 10 series cells, the additional cell inputs can be utilized to improve measurement performance. For example, a long connection may exist between two cells in a pack, such that there may be significant interconnect resistance between the cells, such as shown in Figure 5 between CELL-A and CELL-B. By connecting VC7 close to the positive terminal of CELL-B, and connecting VC8 close to the negative terminal of CELL-A, more accurate cell voltage measurements are obtained for CELL-A and

CELL-B, since the I·R voltage across the interconnect resistance between the cells is not included in either cell voltage measurement. Since the device reports the voltage across the interconnect resistance and the synchronized current in *DASTATUS1–3()*, the resistance of the interconnect between CELL-A and CELL-B can also be calculated and monitored during operation. It is recommended to include the series resistance and bypass capacitor on cell inputs connected in this manner, as shown below.

Note: it is important that the differential input for each cell input not fall below -0.3 V (the Absolute Maximum datasheet limit), with the recommended minimum voltage of -0.2 V. Therefore, it is important that the I·R voltage drop across the interconnect resistance not cause a violation of this requirement.

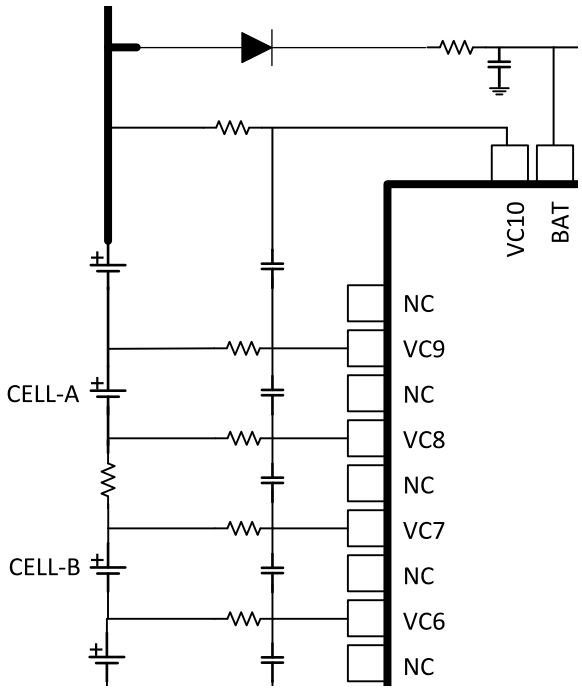


**Figure 5. Using cell input pins for interconnect measurement**

If this connection across an interconnect is not needed (or it is preferred to avoid the extra resistor and capacitor), then unused cell input pins should be shorted to adjacent cell input pins, as shown in Figure 6 for VC8.

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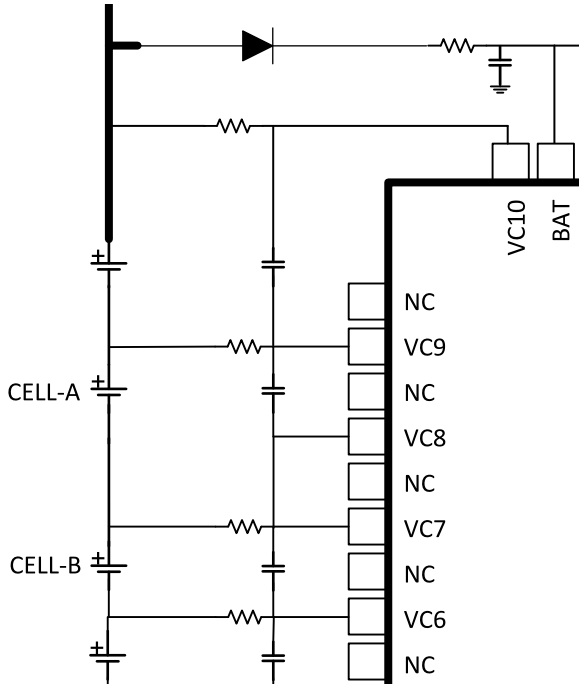


**Figure 6. Terminating an unused cell input pin**

The ***Settings:Configuration:Vcell mode*** configuration register is used to specify which cell inputs are used for actual cells. The device uses this information to disable cell voltage protections associated with inputs which are used to measure interconnect or are not used at all. Voltage measurements for all inputs are reported in 16-bit format (in units of mV) as well as 32-bit format (in units of raw ADC counts), irrespective of whether they are used for cells or not.

#### 7.3.3.1.3 Cell Interconnect Resistance

If measurement of an interconnect between cells is not practical or desired, the BQ76942 device also includes fixed settings for cell interconnect resistance in ***Settings:Interconnect Resistances:Cell 1 Interconnect – Cell 10 Interconnect*** in units of mΩ. The device will subtract the measured current times these interconnect resistance values from each differential cell voltage measurement before reporting the final cell voltage value.

### *7.3.3.2 General Purpose ADCIN Functionality*

Several multifunction pins on the BQ76942 device can be used for general purpose ADC input (ADCIN) measurement, if not being used for other purposes. This includes the TS1, TS2, TS3, CFETOFF, DFETOFF, HDQ, DCHG, DDSG, and ALERT pins. When used for ADCIN functionality, the internal bandgap reference is used by the ADC, and the input range of the ADC is limited to the REG18 pin voltage. The digital fullscale range of the ADC is effectively 1.6667 × VREF1, which is approximately 2.08 V during normal operation. To configure the multifunction pins for this functionality, see the Multifunction Pin Controls section of this document.

When a pin is configured for ADCIN functionality, the voltage is reported in mV using the command that normally reports thermistor temperature on that pin. For example, if TS1 is configured for ADCIN functionality, the *0x70 TS1 Temperature()* command will return a 16-bit signed value corresponding to the pin voltage in mV.

The BQ76942 device also reports the raw ADC counts in *0x0076 DASTATUS6()* when a measurement is taken using the TS1 pin. This data can be used during manufacturing to better calibrate the ADCIN functionality.

#### 7.3.3.3 Coulomb Counter and Digital Filters

The BQ76942 device monitors pack current using a low-side sense resistor, which connects to the SRP and SRN pins through an external RC filter, which should be connected such that a charging current will create a positive voltage on SRP relative to SRN. The device supports sense resistors of 1 mΩ or below. The differential voltage between SRP and SRN is digitized by an integrated coulomb counter ADC, which can digitize voltages over a ±200 mV range and uses multiple digital filters to provide optimized measurement of the instantaneous, averaged, and integrated current. The pins can also support higher positive voltages relative to VSS, such as which may occur during overcurrent or short circuit in discharge conditions, without damage to the device, although the current is not accurately digitized in this case. Multiple digitized current values are available, including two using separate hardware digital filters, CC1 and CC2, as well as a firmware filter CC3.

The units for the current reporting are in userA (userAmps), which can be programmed to be 0.1 mA, 1 mA, 10 mA, or 100 mA using the ***Settings:Configuration:DA Configuration:[USER_AMPS_1:0]*** configuration setting. Given the 16-bit values can range from -32768 to +32767, this allows representation of currents ranging from -3276 A to +3276 A.

**Table 4. Current Measurement Units**

| USER_AMPS_1 | USER_AMPS_0 | Units for Reporting |
|---|---|---|
| 0 | 0 | 0.1 mA |
| 0 | 1 | 1 mA |
| 1 | 0 | 10 mA |
| 1 | 1 | 100 mA |

The CC1 filter generates a 16-bit current measurement that is used for charge integration and other decision purposes, with one output generated every 250 ms when the device is operating in NORMAL mode. The CC1 data is available from the *0x0075 DAStatus5()* subcommand.

The CC2 filter generates a 24-bit current measurement that is used for current reporting, with one output every 3ms when the device is operating in NORMAL mode (which can be reduced to one output every 1.5 ms when the ***Settings:Configuration:Power Config[FASTADC]*** bit is set, with reduced measurement resolution). It is reported in 16-bit format using the *0x3A CC2 Current()* command. The 32-bit CC2 data is available as raw coulomb counter ADC counts from the 0x0071 - 0x0073 subcommands.

The CC3 filter output is an average of a programmable number of CC2 current samples (up to 255), which are set using the ***Settings:Configuration:CC3 Samples*** configuration setting. The CC3 output is reported in 32-bit format using the *0x0075 DASTATUS5()* subcommand, in units of userA.

The integrated passed charge is available as a 64-bit value from the *0x0076 DASTATUS6()* subcommand, which includes the upper 32-bits of accumulated charge in units of userAh, the lower 32-bits of accumulated charge as the fractional portion, and a 32-bit accumulated time over which the charge has been integrated in units of seconds. The accumulated charge integration and timer can be reset using the *0x0082 RESET_PASSQ()* subcommand.

#### 7.3.3.4 Synchronized Voltage and Current Measurement

While the cell voltages are digitized sequentially using a single muxed ADC during normal operation, the current is digitized continuously by the dedicated coulomb counter ADC. The current is measured synchronously with each cell voltage measurement, and can be used for individual cell impedance analysis. The ongoing periodic current measurements can be read out through the digital communication interface, while the measurements taken that were synchronized with particular cell voltage measurements are stored paired with the associated cell voltage measurement for separate readout. The synchronous voltage and current data are available in units of raw ADC counts through the 0x0071-0x0073 subcommands. The Cell-1 voltage is measured and stored as *Cell 1 Voltage Cnts()*, the current is simultaneously measured and stored as *Cell 1 Current Cnts()*, and similarly for all other cells. Reading this data from the block subcommands ensures the synchronously aligned voltage and current data are read out together.

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#### 7.3.3.5 Subcommands 0x0071 DASTATUS1(), 0x0072 DASTATUS2(), and 0x0073 DASTATUS3() - Cell Voltage and Synchronized Current Counts

The *0x0071 DASTATUS1()*, *0x0072 DASTATUS2()*, and *0x0073 DASTATUS3()* subcommands provide raw ADC counts in 32-bit format of the cell voltage measurements, as well as the synchronized current measurements taken simultaneously with each cell voltage measurement. Note: only 24-bit raw data is generated by the data converters, but it is provided in a 32-bit numerical format. The raw ADC data provided for cell voltage measurements uses a digital fullscale range of ± (5 × VREF1), although cell voltage measurements more negative than -0.2 V cannot practically be measured. The raw coulomb counter ADC data provided for current measurements uses a digital fullscale range of ± (VREF2 / 5).

Further detail is shown in the table below.

**Table 5. Cell Voltage and Synchronized Current Counts**

| Subcommand Address | Bytes within Block | Name | Unit |
|---|---|---|---|
| 0x0071 | 0 - 3 | Cell 1 Voltage Cnts | ADC counts |
| | 4 - 7 | Cell 1 Current Cnts | ADC counts |
| | 8 - 11 | Cell 2 Voltage Cnts | ADC counts |
| | 12 - 15 | Cell 2 Current Cnts | ADC counts |
| | 16 - 19 | Cell 3 Voltage Cnts | ADC counts |
| | 20 - 23 | Cell 3 Current Cnts | ADC counts |
| | 24 - 27 | Cell 4 Voltage Cnts | ADC counts |
| | 28 - 31 | Cell 4 Current Cnts | ADC counts |
| 0x0072 | 0 - 3 | Cell 5 Voltage Cnts | ADC counts |
| | 4 - 7 | Cell 5 Current Cnts | ADC counts |
| | 8 - 11 | Cell 6 Voltage Cnts | ADC counts |
| | 12 - 15 | Cell 6 Current Cnts | ADC counts |
| | 16 - 19 | Cell 7 Voltage Cnts | ADC counts |
| | 20 - 23 | Cell 7 Current Cnts | ADC counts |
| | 24 - 27 | Cell 8 Voltage Cnts | ADC counts |
| | 28 - 31 | Cell 8 Current Cnts | ADC counts |
| 0x0073 | 0 - 3 | Cell 9 Voltage Cnts | ADC counts |
| | 4 - 7 | Cell 9 Current Cnts | ADC counts |
| | 8 - 11 | Cell 10 Voltage Cnts | ADC counts |
| | 12 - 15 | Cell10 Current Cnts | ADC counts |
| | 16 - 31 | Reserved | - |

#### 7.3.3.6 Subcommands 0x0075 DASTATUS5() and 0x0076 DASTATUS6() - Additional Voltage, Current, Charge, and Temperature Measurements

The *0x0075 DASTATUS5()* subcommand provides voltage measurements of the voltage reference used by the coulomb counter (VREF2), the VSS pin, as well as calculated values for the minimum, maximum, and sum of cell voltage measurements. It also provides the readings used for cell and FET temperature, minimum, maximum, and average cell temperature, and both CC1 and CC3 current values.

Since the VREF2 measurement is measured by the voltage ADC using VREF1, this measurement provides a ratio of one reference versus the other and should stay approximately constant. This measurement can be used as a diagnostic check to determine if one reference changes value versus the other.

The VSS measurement is included as an additional diagnostic measurement to ensure that the ADC input mux is working properly. This measurement should normally result in a value near zero. If an internal fault were to occur that caused the ADC input mux to be stuck at a particular setting, such as a cell input, then the VSS measurement would be significantly higher. If the mux were stuck at a setting such as an interconnect measurement or VSS, the cell voltage measurements would be reported as very low voltage.

The Battery Voltage Sum is the sum of all enabled cell voltage measurements, reported in cV. This value can be compared with the *0x34 Stack Voltage()* and used as a diagnostic check. Note: since the measurements are taken by the same ADC at different times, transient changes in the cell voltages can cause differences in the sum versus the stack measurement and will need to be comprehended.

Further detail is shown in the table below.

**Table 6. *0x0075 DASTATUS5()* Subcommand Detail**

| Subcommand Address | Bytes within Block | Name | Unit |
|---|---|---|---|
| 0x0075 | 0 - 1 | Vref | 16-bit ADC counts |
| | 2 - 3 | VSS | 16-bit ADC counts |
| | 4 - 5 | Max Cell Voltage | mV |
| | 6 - 7 | Min Cell Voltage | mV |
| | 8 - 9 | Battery Voltage Sum | cV |
| | 10 - 11 | Avg Cell Temperature | 0.1°K |
| | 12 - 13 | FET Temperature | 0.1°K |
| | 14 - 15 | Max Cell Temperature | 0.1°K |
| | 16 - 17 | Min Cell Temperature | 0.1°K |
| | 18 - 19 | Avg Cell Temperature | 0.1°K |
| | 20 - 21 | CC3 Current | userA |
| | 22 - 23 | CC1 Current | userA |
| | 24 - 27 | Raw CC2 Counts | 32-bit ADC counts |
| | 28 - 31 | Raw CC3 Counts | 32-bit ADC counts |

The *0x0076 DASTATUS6()* subcommand provides the accumulated charge value and associated timer. It also includes the 32-bit raw ADC count for the TS1 measurement, which can be used for customer calibration of the general purpose ADC input measurement capability of the device. The details of this subcommand are shown below.

**Table 7. *0x0076 DASTATUS6()* Subcommand Detail**

| Subcommand Address | Bytes within Block | Name | Unit |
|---|---|---|---|
| 0x0076 | 0 - 3 | Accumulated charge (integer portion) | 32-bit signed integer portion in userAh |
| | 4 - 7 | Accumulated charge (fractional portion), initialized to 0.5 userAh when reset | 32-bit fractional portion in userAh |
| | 8 - 11 | Accumulated Time | 32-bit unsigned integer in seconds |
| | 12 - 15 | TS1 Raw ADC Counts | 32-bit ADC counts |
| | 16 - 31 | Reserved | - |

#### *7.3.3.7 Internal Temperature Measurement*

The BQ76942 device integrates the capability to measure its internal die temperature by digitizing an internal transistor base-emitter voltage. This voltage is measured periodically as part of the measurement loop and is processed to provide a temperature value using the *0x68 Int Temperature()* command.

This internal temperature measurement can be used for cell temperature protections and logic that uses minimum, maximum, or average cell temperature by setting the ***Settings:Configuration:DA Configuration[TINT_EN]*** configuration bit and keeping the ***Settings:Configuration:DA Configuration[TINT_FETT]*** bit cleared. The internal temperature measurement can instead be used for FET temperature by setting both ***Settings:Configuration:DA Configuration[TINT_EN]*** and ***Settings:Configuration:DA Configuration[TINT_FETT]***, although in this case it will not be used for cell temperature.

The calculation of temperature is performed as follows:

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Internal Temperature (in units of 0.1°K) = (ADC value) × ***Calibration:Internal Temp Model:Int Gain*** / 65536 + ***Calibration:Internal Temp Model:Int base offset*** + ***Calibration:Temperature:Internal Temp Offset***

except if (ADC value) > ***Calibration:Internal Temp Model:Int Maximum AD***, then the reported internal temperature is calculated using the ***Calibration:Internal Temp Model:Int Maximum AD*** as the ADC value. If internal temperature is calculated > ***Calibration:Internal Temp Model:Int Maximum Temp***, the reported internal temperature is set to ***Calibration:Internal Temp Model:Int Maximum Temp***.

#### *7.3.3.8 Thermistor Temperature Measurement*

The BQ76942 device includes an on-chip temperature measurement and can also support up to nine external thermistors on multifunction pins (TS1, TS2, TS3, CFETOFF, DFETOFF, ALERT, HDQ, DCHG, and DDSG). The device includes an internal pullup resistor to bias a thermistor during measurement.

The internal pull-up resistor has two options which can set the pull-up resistor to either 18-kΩ or 180-kΩ (or none at all). The 18-kΩ option is intended for use with thermistors such as the Semitec 103-AT, which has 10-kΩ resistance at room temperature. The 180-kΩ is intended for use with higher resistance thermistors such as the Semitec 204AP-2, which has 200-kΩ resistance at room temperature. The resistor values are measured during factory production and stored within the device for use during temperature calculation. The individual pin configuration registers determine which pin is used for a thermistor measurement, what value of pull-up resistor is used, as well as whether the thermistor measurement is used for a cell or FET temperature reading. For more detail on these pin configuration registers, see Multifunction Pin Controls.

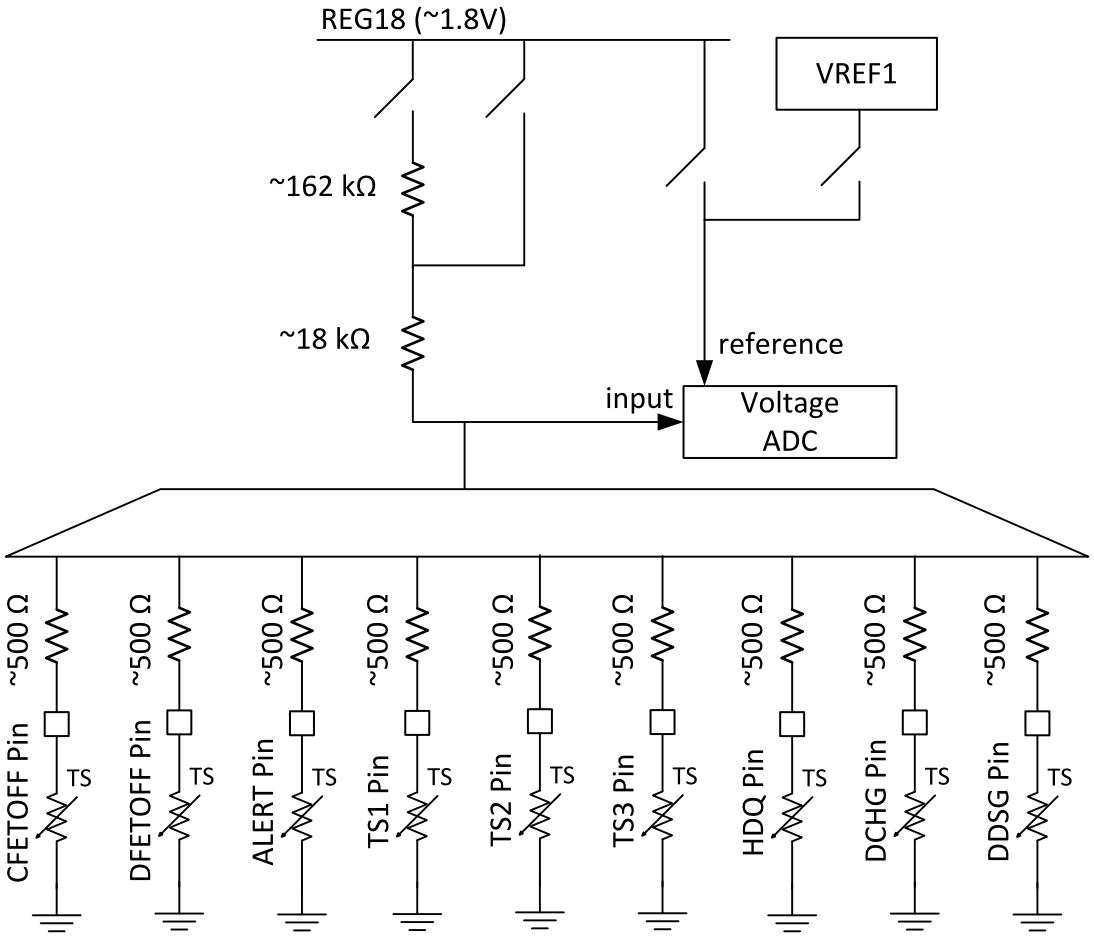


**Figure 7. External Thermistor Biasing**

**Table 8. Temperature Measurement Commands**

| Command Address | Name | Comment |
|---|---|---|
| 0x68 | Int Temperature | Internal die temperature |
| 0x6A | CFETOFF Temperature | CFETOFF pin thermistor |
| 0x6C | DFETOFF Temperature | DFETOFF pin thermistor |
| 0x6E | ALERT Temperature | ALERT pin thermistor |
| 0x70 | TS1 Temperature | TS1 pin thermistor |
| 0x72 | TS2 Temperature | TS2 pin thermistor |
| 0x74 | TS3 Temperature | TS3 pin thermistor |
| 0x76 | HDQ Temperature | HDQ pin thermistor |
| 0x78 | DCHG Temperature | DCHG pin thermistor |
| 0x7A | DDSG Temperature | DDSG pin thermistor |

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The calculation of temperature from the measured ADC value is performed using a temperature model, which includes gain, offset, and a polynomial computation. The device includes configuration registers for one temperature model based on the 18-kΩ pull-up resistor in ***Calibration:18K Temperature Model***, and a second temperature model based on the 180-kΩ pull-up resistor in ***Calibration:180K Temperature Model***. This allows one type of thermistor to be used for measuring cell temperature, versus another type may be used for measuring FET temperature. The default parameters for the models match the Semitec 103-AT and 204AP-2 thermistors.

In order to provide a high precision temperature result, the device uses the same 1.8 V LDO voltage for the ADC reference as is used for biasing the thermistor pullup resistor, thereby implementing a ratiometric measurement that removes the error contribution from the LDO voltage level. The device processes the digitized thermistor voltage to calculate the temperature based on multiorder polynomials, which can be programmed by the user based on the specific thermistor selected.

#### *7.3.3.9 Factory Trim of Voltage ADC*

The BQ76942 device includes factory trim for the cell voltage ADC measurements in order to optimize the voltage measurement performance even if no further calibration is performed by the customer. Calibration can be performed by the customer on the production line to further optimize the performance in the system. The trim information is used to correct the raw ADC readings before they are reported as 16-bit voltage values. The 32-bit ADC voltage data, which is generated in units of ADC counts, is modified before reporting by subtracting a stored offset trim value. The resulting reported data does not include any further correction (such as for gain), therefore the customer will need to process them before use.

The device also includes a factory gain trim for the voltage measurements performed using the general purpose ADC input capability on the multifunction pins as well as the TS1, TS2, and TS3 pins. The raw ADC reading is provided for the TS1 pin in 32-bit ADC counts using the *0x0076 DASTATUS6()* subcommand.

#### *7.3.3.10 Voltage Calibration (ADC Measurements)*

The BQ76942 device includes optional capability for the customer to calibrate each cell voltage gain and the gain for the stack voltage, the PACK pin voltage, and the LD pin voltage individually, and multifunction pin general ADC measurements. An offset calibration value ***Calibration:Vcell Offset:Vcell Offset*** is included for use with the cell voltage measurements, and ***Calibration:Vdiv Offset:Vdiv Offset*** is for use with the TOS (stack), PACK, and LD voltage measurements. The cell voltage gains determined during calibration are written in ***Calibration:Voltage:Cell 1 Gain – Cell 10 Gain***, where ***Cell 1 Gain*** is used for the measurement of VC1-VC0, ***Cell 2 Gain*** is used for the measurement of VC2-VC1, and so forth. Similarly, the calibration voltage gain for the TOS voltage should be written in ***Calibration:Voltage:TOS Gain***, the PACK pin voltage gain in ***Calibration:Voltage:Pack Gain***, the LD pin voltage gain in ***Calibration:Voltage:LD Gain***, and multifunction pin general purpose ADCIN measurement gain in ***Calibration:Voltage:ADC Gain***.

If values for the calibration gain configuration are not written, the BQ76942 device will use factory trim or default values for the respective gain values. When a calibration gain configuration value is written, the device will use that in place of any factory trim or default gain. The raw ADC measurement data (in units of counts) is corrected by first subtracting a stored offset trim value, then the gain is applied, then the ***Calibration:Vcell Offset:Vcell Offset*** (for cell voltage measurements) or the ***Calibration:Vdiv Offset:Vdiv Offset*** (for TOS, PACK, or LD voltage measurements) is subtracted, before the final voltage value is reported.

The factory trim values for the Cell Gain parameters can be read from the Cell Gain data memory registers while in FULLACCESS mode but not in CONFIG_UPDATE mode, if the data memory values have not been overwritten. While in CONFIG_UPDATE mode, the Cell Gain values will read back either all zeros if they have not been overwritten, or whatever values have been written to these registers. Upon exiting CONFIG_UPDATE mode, readback of the Cell Gain parameters will provide the values presently used in operation.

The cell voltage calibration can be implemented by applying two precise DC voltages to the cell input (such as 2.5 V and 4.5 V) and averaging multiple raw ADC measurements in 32-bit counts obtained from the *0x0071 - 0x0073 DASTATUS1–3()* subcommands for each voltage. The gain can then be calculated as:

$$\text{Cell Gain} = \frac{2^{24} \times \left(\text{Voltage\_1}_{\text{in mV}} - \text{Voltage\_2}_{\text{in mV}}\right)}{\left(\text{32-bit ADC counts}\right)_{\text{Voltage\_1}} - \left(\text{32-bit ADC counts}\right)_{\text{Voltage\_2}}}$$

The offset for the cell voltage measurement can now be calculated as shown below:

$$\text{Cell Offset} = \frac{(\text{Cell Gain}) \times (\text{32-bit ADC counts})_{\text{Voltage\_2}}}{2^{24}} - \text{Voltage\_2}_{\text{in mV}}$$

The calibration for the TOS, PACK pin, and LD pin gain measurements can be implemented by similarly applying two precise DC voltages to the input and averaging multiple raw ADC measurements, which are provided in 16-bit counts from the *0xF081 READ_CAL1()* subcommand. Note: one of the voltages can be skipped to reduce calibration time. The gain can then be calculated as:

$$\text{TOS / PACK / LD Gain} = \frac{2^{16} \times \left(\text{Voltage\_1}_{\text{in cV}} - \text{Voltage\_2}_{\text{in cV}}\right)}{(\text{16-bit ADC counts})_{\text{Voltage\_1}} - (\text{16-bit ADC counts})_{\text{Voltage\_2}}}$$

The ADCIN measurement can be calibrated by setting ***Calibration:Voltage:ADC Gain*** = 32767, which results in the 16-bit counts reported in place of the pin voltage. For example, if the CFETOFF pin is being used for ADCIN functionality, when ***Calibration:Voltage:ADC Gain*** is set to 32767, the raw 16-bit ADC counts can be obtained from the *0x6A CFETOFF Temperature()* command. This then allows the gain calibration by applying one or two precise DC voltages to the selected pin, and the 16-bit counts are obtained from temperature command for each voltage. The gain can then be calculated as:

$$\text{ADC Gain} = \frac{2^{16} \times \left(\text{Voltage\_1}_{\text{in mV}} - \text{Voltage\_2}_{\text{in mV}}\right)}{(\text{16-bit ADC counts})_{\text{Voltage\_1}} - (\text{16-bit ADC counts})_{\text{Voltage\_2}}}$$

The ADCIN measurement can also be calibrated using the TS1 pin. Similar to the cell voltage gain calibration, one or two precise DC voltages can be applied to the TS1 pin, and the 32-bit counts obtained from the *0x0076 DASTATUS6()* subcommand for each voltage. The gain can then be calculated as:

$$\text{ADC Gain} = \frac{2^{24} \times \left(\text{Voltage\_1}_{\text{in mV}} - \text{Voltage\_2}_{\text{in mV}}\right)}{(\text{32-bit ADC counts})_{\text{Voltage\_1}} - (\text{32-bit ADC counts})_{\text{Voltage\_2}}}$$

The effective fullscale digital range of the cell measurement is 5 × VREF1, and the effective fullscale digital range of the ADCIN measurement is 1.667 × VREF1, although the voltages applied for these measurement should be limited based on the specifications in Specifications. Using a value for VREF1 of 1.25 V, the nominal gain for the cell measurements is 12409, while the nominal gain for the ADCIN measurements is 4166. The reported voltages are calculated as:

*Cell # Voltage()* = ***Calibration:Voltage:Cell # Gain*** × (16-bit ADC counts) / 65536 - ***Calibration:Vcell Offset:Vcell Offset***

*Stack Voltage()* = ***Calibration:Voltage:TOS Gain*** × (16-bit ADC counts) / 65536 - ***Calibration:Vdiv Offset:Vdiv Offset***

*PACK Pin Voltage()* = ***Calibration:Voltage:Pack Gain*** × (16-bit ADC counts) / 65536 - ***Calibration:Vdiv Offset:Vdiv Offset***

*LD Pin Voltage()* = ***Calibration:Voltage:LD Gain*** × (16-bit ADC counts) / 65536 - ***Calibration:Vdiv Offset:Vdiv Offset***

ADCIN Voltage = ***Calibration:Voltage:ADC Gain*** × (16-bit ADC counts) / 65536

Note: *Cell # Voltage()* and ***Calibration:Vcell Offset:Vcell Offset*** both have units of mV. The divider voltages (*Stack Voltage()*, *PACK Pin Voltage()*, and *LD Pin Voltage()*) and ***Calibration:Vdiv Offset:Vdiv Offset*** all have units of userV.

#### *7.3.3.11 Voltage Calibration (COV and CUV Protections)*

The BQ76942 device includes optional capability for the customer to calibrate the COV (cell overvoltage) and CUV (cell undervoltage) protection thresholds on the production line, in order to improve threshold accuracy in system or to realize a threshold between the preset thresholds available from the device.

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This calibration is performed while the device is in CONFIG_UPDATE mode. To calibrate the COV threshold, an external voltage is first applied between VC10 and VC9 that is equal to the desired COV threshold. Next, the *CAL_COV()* subcommand is sent by the host, which causes the BQ76942 device to perform a search for the appropriate calibration coefficients to realize a COV threshold at or close to the applied voltage level. When this search is completed, the resulting calibration coefficient is returned by the subcommand and automatically written into the ***Protections:COV:COV Threshold Override*** configuration parameter. If this parameter is nonzero, the device will not use its factory trim settings but will instead use this value.

The CUV threshold is calibrated similarly, an external voltage is applied between VC10 and VC9 equal to the desired CUV threshold. Next, while in CONFIG_UPDATE mode, the *CAL_CUV()* subcommand is sent by the host, which causes the BQ76942 device to perform a search for the appropriate calibration coefficients to realize a CUV threshold at or close to the applied voltage level. When this search is completed, the resulting calibration coefficient is returned by the subcommand and automatically written into the ***Protections:CUV:CUV Threshold Override*** configuration parameter.

#### 7.3.3.12 Current Calibration

The BQ76942 device coulomb counter ADC measures the differential voltage between the SRP and SRN pins to calculate the system current. The device includes the optional capability for the customer to calibrate the coulomb counter offset and current gain on the production line.

The ***Calibration:Current Offset:CC Offset*** configuration register contains an offset value in units of 32-bit coulomb counter ADC counts and ***Calibration:Current Offset:Coulomb Counter Offset Samples***. The value of ***Calibration:Current Offset:CC Offset*** / ***Calibration:Current Offset:Coulomb Counter Offset Samples*** is subtracted from the raw coulomb counter ADC counts, then the result is multiplied by ***Calibration:Current:CC Gain*** and scaled to provide the final result in units of userA.

The BQ76942 device uses the ***Calibration:Current:CC Gain*** and ***Calibration:Current:Capacity Gain*** configuration values to convert from the ADC value to current. The ***CC Gain*** reflects the value of the sense resistor used in the system, while the ***Capacity Gain*** is simply the ***CC Gain*** multiplied by 298261.6178.

Both the ***CC Gain*** and ***Capacity Gain*** are encoded using a 32-bit IEEE-754 floating point format. The effective value of the sense resistor is given by:

***CC Gain*** = 7.4768 / (Rsense in mΩ)

#### 7.3.3.13 Temperature Calibration

The BQ76942 device enables the customer to calibrate the internal as well as external temperature measurements on the production line, by storing an offset value which is added to the calculated measurement before reporting. A separate offset for each temperature measurement can be stored in the configuration registers shown below.

**Table 9. Temperature Calibration Settings**

| Section | Subsection | Register Description | Comment | Units |
|---|---|---|---|---|
| Calibration | Temperature | Internal Temp Offset | | 0.1°K |
| Calibration | Temperature | CFETOFF Temp Offset | CFETOFF pin thermistor | 0.1°K |
| Calibration | Temperature | DFETOFF Temp Offset | DFETOFF pin thermistor | 0.1°K |
| Calibration | Temperature | ALERT Temp Offset | ALERT pin thermistor | 0.1°K |
| Calibration | Temperature | TS1 Temp Offset | TS1 pin thermistor | 0.1°K |
| Calibration | Temperature | TS2 Temp Offset | TS2 pin thermistor | 0.1°K |
| Calibration | Temperature | TS3 Temp Offset | TS3 pin thermistor | 0.1°K |
| Calibration | Temperature | HDQ Temp Offset | HDQ pin thermistor | 0.1°K |
| Calibration | Temperature | DCHG Temp Offset | DCHG pin thermistor | 0.1°K |
| Calibration | Temperature | DDSG Temp Offset | DDSG pin thermistor | 0.1°K |

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### 7.3.4 Integrated Protection Subsystem

An extensive protection subsystem is integrated within BQ76942, which can monitor a variety of parameters, initiate protective actions, and autonomously recover based on conditions. The device also includes a wide range of flexibility, such that the device can be configured to monitor and initiate protective action, but with recovery controlled by the host processor, or such that the device only monitors and alerts the host processor whenever conditions warrant protective action, but with action and recovery fully controlled by the host processor.

The primary protection subsystem includes a suite of individual protections which can be individually enabled and configured, including cell undervoltage and overvoltage, overcurrent in charge, three separate overcurrent in discharge protections, short circuit current in discharge, cell overtemperature and undertemperature in charge and discharge, FET overtemperature, a host processor communication watchdog timeout, and pre-charge mode timeout. The cell undervoltage and overvoltage, overcurrent in charge, overcurrent in discharge 1 and 2, and short circuit in discharge protections are based on comparator thresholds, while the remaining protections (such as those involving temperature, host watchdog, and precharging) are based on firmware on the internal controller.

The device integrates NFET drivers for high-side CHG and DSG protection FETs, which can be configured in a series or parallel configuration. An integrated charge pump generates a voltage which is driven onto the NFET gates based on host command or the on-chip protection subsystem settings. Support is also included for high-side PFETs used to implement a precharge and predischarge functionality.

The secondary protection suite within the BQ76942 device can react to more serious faults and take action to permanently disable the pack, by initiating a Permanent Fail (PF). The secondary safety provides protection against safety cell undervoltage and overvoltage, safety overcurrent in charge and discharge, safety overtemperature for cells and FETs, excessive cell voltage imbalance, internal memory faults, and internal diagnostic failures.

When a Permanent Fail has occurred, the BQ76942 device can be configured to either simply provide a flag, or to indefinitely disable the protection FETs, or to assert the FUSE pin to permanently disable the pack. The FUSE pin can be used to blow an in-line fuse and also can monitor if a separate secondary protector IC has attempted to blow the fuse.

#### *7.3.4.1 Protections*

The BQ76942 device integrates a broad suite of protections for battery management and provides the capability to enable individual protections, as well as to select which protections will result in autonomous control of the FETs. The ***Settings:Manufacturing:Mfg Status Init[FET_EN]*** configuration bit determines whether the device is in autonomous control mode (when set) or in FET test mode (when cleared). The FET test mode is primarily for use on a customer production line, to test individual FETs. The autonomous control mode is recommended for field operation, which still allows the host to disable FETs through serial communications or using the CFETOFF and DFETOFF pins, and block their re-enabling by the device until the host allows.

The individual protections can be enabled by setting the related ***Settings:Protection:Enabled Protections A – C*** configuration registers. The protections controlled by ***Settings:Protection:Enabled Protections A*** are comparator-based, while those in ***Settings:Protection:Enabled Protections B and C*** are partly or entirely firmware-based.

Each protection that has been enabled can also be controlled regarding whether it will disable a particular FET or not by setting related configuration bits. The bits in ***Settings:Protection:CHG FET Protections A – C*** determine which protections will trigger the CHG FET being disabled, while those in ***Settings:Protection:DSG FET Protections A – C*** determine which will trigger the DSG FET being disabled. Note: protections which are configured to disable the CHG FET will also disable the predischarge FET when it is enabled. Similarly, protections configured to disable the DSG FET will also disable the predischarge FET when it is enabled.

Most protections involve the device checking for a violation of a particular condition, such as a voltage or current threshold. As soon as a violating condition is detected for an enabled protection, a safety alert is set. Flags showing which safety alerts may be present are available through the *0x02 Safety Alert A*, *0x04 Safety Alert B*, and *0x06 Safety Alert C* commands, and their presence can generate an interrupt to a host processor on the ALERT pin.

Most protections also include a delay, such that if the violating condition persists for some time interval, a safety fault is triggered. Flags showing which safety faults may be present are available through the *0x03 Safety Status A*, *0x05 Safety Status B*, and *0x07 Safety Status C* commands, and their presence can generate an interrupt to a host processor on the ALERT pin.

The format of the safety alert and safety status commands is shown below.

**Table 10. Format for *0x02 Safety Alert A()* Command**

| Bit | Name | Description |
|---|---|---|
| 7 | SCD | Short Circuit in Discharge safety alert is present |
| 6 | OCD2 | Overcurrent in Discharge 2 safety alert is present |
| 5 | OCD1 | Overcurrent in Discharge 1 safety alert is present |
| 4 | OCC | Overcurrent in Charge safety alert is present |
| 3 | COV | Cell Overvoltage safety alert is present |
| 2 | CUV | Cell Undervoltage safety alert is present |
| 1 | RSVD | Reserved |
| 0 | RSVD | Reserved |

**Table 11. Format for *0x03 Safety Status A()* Command**

| Bit | Name | Description |
|---|---|---|
| 7 | SCD | Short Circuit in Discharge safety fault is present |
| 6 | OCD2 | Overcurrent in Discharge 2 safety fault is present |
| 5 | OCD1 | Overcurrent in Discharge 1 safety fault is present |
| 4 | OCC | Overcurrent in Charge safety fault is present |
| 3 | COV | Cell Overvoltage safety fault is present |
| 2 | CUV | Cell Undervoltage safety fault is present |
| 1 | RSVD | Reserved |
| 0 | RSVD | Reserved |

**Table 12. Format for *0x04 Safety Alert B()* Command**

| Bit | Name | Description |
|---|---|---|
| 7 | OTF | FET Overtemperature safety alert is present |
| 6 | OTINT | Internal Die Overtemperature safety alert is present |
| 5 | OTD | Overtemperature in Discharge safety alert is present |
| 4 | OTC | Overtemperature in Charge safety alert is present |
| 3 | RSVD | Reserved |
| 2 | UTINT | Internal Die Undertemperature safety alert is present |
| 1 | UTD | Undertemperature in Discharge safety alert is present |
| 0 | UTC | Undertemperature in Charge safety alert is present |

**Table 13. Format for *0x05 Safety Status B()* Command**

| Bit | Name | Description |
|---|---|---|
| 7 | OTF | FET Overtemperature safety fault is present |
| 6 | OTINT | Internal Die Overtemperature safety fault is present |
| 5 | OTD | Overtemperature in Discharge safety fault is present |
| 4 | OTC | Overtemperature in Charge safety fault is present |
| 3 | RSVD | Reserved |
| 2 | UTINT | Internal Die Undertemperature safety fault is present |
| 1 | UTD | Undertemperature in Discharge safety fault is present |
| 0 | UTC | Undertemperature in Charge safety fault is present |

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**Table 14. Format for *0x06 Safety Alert C()* Command**

| Bit | Name | Description |
|---|---|---|
| 7 | OCD3 | Overcurrent in Discharge 3 safety alert is present |
| 6 | SCDL | Latched Short Circuit in Discharge safety alert is present |
| 5 | OCDL | Latched Overcurrent in Discharge safety alert is present |
| 4 | COVL | Latched Cell Overvoltage safety alert is present |
| 3 | PTOS | Precharge timer is suspended due to current below ***Protections:PTO:Charge Threshold*** |
| 2 | RSVD | Reserved |
| 1 | HWDF | Host watchdog safety alert is present |
| 0 | RSVD | Reserved |

**Table 15. Format for *0x07 Safety Status C()* Command**

| Bit | Name | Description |
|---|---|---|
| 7 | OCD3 | Overcurrent in Discharge 3 safety fault is present |
| 6 | SCDL | Latched Short Circuit in Discharge safety fault is present |
| 5 | OCDL | Latched Overcurrent in Discharge safety fault is present |
| 4 | COVL | Latched Cell Overvoltage safety fault is present |
| 3 | RSVD | Reserved |
| 2 | PTO | Precharge Timeout safety fault is present |
| 1 | HWDF | Host watchdog safety fault is present |
| 0 | RSVD | Reserved |

#### *7.3.4.2 High-Side NFET Drivers*

The BQ76942 device includes an integrated charge pump and high-side NFET drivers for driving CHG and DSG protection FETs. The charge pump uses an external capacitor connected between the BAT and CP1 pins that is charged to an overdrive voltage when the charge pump is enabled (controlled using the ***Settings:FET:Chg Pump Control[CPEN]*** configuration bit). Due to the time required for the charge pump to bring the overdrive voltage on the external CP1 pin to full voltage, it is recommended to leave the charge pump powered whenever it may be needed quickly to drive the CHG or DSG FETs.

The DSG FET driver includes a special option (denoted source follower mode) to drive the DSG FET with the BAT pin voltage during SLEEP mode. This capability is included to provide low power in SLEEP mode, when there is no significant charge or discharge current flowing. It is recommended to keep the charge pump enabled even when the source follower mode is enabled, so whenever a discharge current is detected, the device can quickly transition to driving the DSG FET using the charge pump voltage. The source follower mode is enabled by setting the ***Settings:FET:Chg Pump Control[SFMODE_SLEEP]*** configuration bit. The source follower mode is not intended to be used when significant charging or discharging current is flowing, since the FET will exhibit a large drain-source voltage and may undergo excessive heating.

The overdrive level of the charge pump voltage can be set to 5.5 V or 11 V, using the ***Settings:FET:Chg Pump Control[LVEN]*** configuration bit. In general, the 5.5 V setting results in lower power dissipation when a FET is being driven, while the higher 11 V overdrive reduces the on-resistance of the FET. If a FET exhibits significant gate leakage current when driven at the higher overdrive level, this can result in a higher device current for the charge pump to support this. In this case, using the lower overdrive level can reduce the leakage current and thus the device current.

The BQ76942 device supports a system with FETs in a series or parallel configuration, where the parallel configuration includes a separate path for the charger connection versus the discharge (load) connection. The control logic for the device operates slightly differently in these two cases, which is set based on the ***Settings:FET:FET Options[SFET]*** configuration bit. See FET Configuration for more information on this operation.

The FET drivers in the BQ76942 device can be controlled in several different manner, depending on customer requirements:

**Fully autonomous**

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The BQ76942 device can detect protection faults and autonomously disable the FETs, monitor for a recovery condition, and autonomously re-enable the FETs, without requiring any host processor involvement.

This mode is enabled by setting the ***Settings:Manufacturing:Mfg Status Init[FET_EN]*** configuration bit. The FETs may be disabled when a fault occurs based on settings in ***Settings:Protection:CHG FET Protections A/B/C*** and ***Settings:Protection:DSG FET Protections A/B/C.***

**Partially autonomous**

The BQ76942 device can detect protection faults and autonomously disable the FETs. When the host receives an interrupt and recognizes the fault, the host can write the *0x0093 DSG_PDSG_OFF()* or *0x0094 CHG_PCHG_OFF()* or *0x0095 ALL_FETS_OFF()* commands to keep the FETs off until the host decides to release them. The *0x0097 FET_CONTROL()* subcommand can also be used to enable or disable each FET individually.

Alternatively, the host can assert the CFETOFF or DFETOFF pins to keep the FETs off. When the host decides to allow the FETs to turn on again, it writes the *0x0096 ALL_FETS_ON()* command, and the BQ76942 device will re-enable the FETs if nothing is blocking them being re-enabled (such as fault conditions still present, or the CFETOFF or DFETOFF pins are asserted).

**Manual control**

The BQ76942 device can detect protection faults and provide an interrupt to a host processor over the ALERT pin. The host processor can read the status information of the fault over the communication bus (if desired) and can quickly force the CHG or DSG FETs off by driving the CFETOFF or DFETOFF pins from the host processor, or using the *0x0093 DSG_PDSG_OFF()* or *0x0094 CHG_PCHG_OFF()*, *0x0095 ALL_FETS_OFF()*, or *0x0097 FET_CONTROL()* subcommands.

When the host decides to allow the FETs to turn on again, it writes the *0x0096 ALL_FETS_ON()* command or deasserts the CFETOFF and DFETOFF pins, and the BQ76942 device will re-enable the FETs if nothing is blocking them being re-enabled.

The status of the FET drivers is provided by the *[DSG_FET]* and *[CHG_FET]* bits in the *0x7F FET Status()* command. Depending on the device mode and fault status, there may be cases when only one FET is enabled, and the other FET is disabled. For example:

During SLEEP mode, the CHG FET may be disabled (if ***Settings:FET:FET Options[SLEEPCHG]*** is cleared), while the DSG FET is enabled.

If a COV fault has occurred, the CHG FET may be disabled, while the DSG FET may still be enabled, to allow discharge.

If a CUV fault has occurred, the DSG FET may be disabled, while the CHG FET may still be enabled, to allow charging.

If the device is in series FET configuration and a single FET is on, it is possible for current to flow through the off-FET body diode. This current can damage the FET if high enough for a long enough time. In this case, when the BQ76942 device is autonomously controlling the FETs, if a current is detected above a level given by ***Settings:Protection:Body Diode Threshold***, the device will automatically turn on the off-FET, to prevent further damage. This configuration register should be a positive value, it is used as a charging current level when deciding to turn on the DSG FET, and it is used as a discharging current level when deciding to turn on the CHG FET.

If the high-side NFET drivers will not be used in the application, the charge pump and FET drivers can be disabled by clearing the ***Settings:FET:Chg Pump Control[CPEN]*** and ***Settings:FET:FET Options[FET_CTRL_EN]*** configuration bits.

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#### 7.3.4.3 Cell Overvoltage Protection

The BQ76942 device integrates Cell Overvoltage Protection (COV), monitoring the voltage of every cell using a comparator-based circuit, and triggering a COV alert or fault when a cell voltage exceeds the COV threshold. The COV threshold is programmable from 1.0 V to 5.5 V in 50 mV steps and is set by the ***Protections:COV:Threshold*** configuration register. The COV protection is enabled using the ***Settings:Protection:Enabled Protections A:[COV]*** configuration bit.

The COV circuitry triggers an alert signal when an overvoltage event is first detected, then will trigger a fault after a programmable detection delay, COV_DLY, which can be set from 10 ms to 6762 ms in units of 3.3 ms, with the actual delay being 3.3 ms × (2 + setting). The setting 0x0 disables the protection. The delay is set by the ***Protections:COV:Delay*** configuration register.

When a COV fault is triggered, it will recover if the maximum cell voltage drops below the COV threshold by a COV_HYS hysteresis level, which is programmable from 100 mV to 1 V in steps of 50 mV, for ***Protections:Recovery:Time***. The COV_HYS hysteresis level is set by the ***Protections:COV:Recovery Hysteresis*** configuration register.

When an COV fault is triggered, the device will turn off the CHG FET if configured for autonomous FET control based on setting in ***Settings:Protection:CHG FET Protections A[COV]*** (the DSG FET remains enabled if already enabled). The device will recover (if configured for autonomous FET control) based on all cell voltages being below COV threshold – COV_HYS for ***Protections:Recovery:Time***.

The BQ76942 device also includes a Cell Overvoltage Latch (COVL) protection, which can create a fault if multiple COV failures occur within a programmable time window. Whenever a COV fault is triggered, the COVL latch counter is incremented. After the device recovers, it will decrement the COVL counter after a programmable recovery time window (given by ***Protections:COVL:Counter Dec Delay***) if no further COV faults are detected. If the COVL counter reaches a programmable latch limit (given by ***Protections:COVL:Latch Limit***), it will trigger a COVL fault.

The COVL protection recovers after a programmable delay given by ***Protections:COVL:Recovery Time***. The COVL protection is enabled using the ***Settings:Protection:Enabled Protections C:[COVL]*** configuration bit. Further detail is described in the table below. Note: timing on COV changes while cell balancing is active, as described in Table 34

**Table 16. Overvoltage Protection Operation**

| Status | Condition | Action |
|---|---|---|
| Normal | Max cell voltage < ***Protections:COV:Threshold*** | *Safety Alert A()[COV]* = 0<br>Decrement COVL counter by one after each ***Protections:COVL:Counter Dec Delay*** period if COVL counter > 0 |
| Alert | Max cell voltage ≥ ***Protections:COV:Threshold*** | *Safety Alert A()[COV]* = 1 |
| Trip | Max cell voltage ≥ ***Protections:COV:Threshold*** for ***Protections:COV:Delay*** duration | *Safety Alert A()[COV]* = 0<br>*Safety Status A()[COV]* = 1<br>*Alarm Raw Status()[XCHG]* = 1 if autonomous FET control is enabled<br>Increment COVL counter |
| Recovery | *Safety Status A()[COV]* = 1 and<br>Max cell voltage < ***Protections:COV:Threshold*** - ***Protections:COV:Recovery Hysteresis*** for ***Protections:Recovery:Time*** | *Safety Status A()[COV]* = 0<br>*Alarm Raw Status()[XCHG]* = 0 if autonomous FET control is enabled |
| Latch Alert | COVL counter > 0 | *Safety Alert C()[COVL]* = 1 |
| Latch Trip | COVL counter ≥ ***Protections:COVL:Latch Limit*** | *Safety Status C()[COVL]* = 1<br>*Safety Alert C()[COVL]* = 0<br>*Alarm Raw Status()[XCHG]* = 1 if autonomous FET control is enabled |

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**Table 16. Overvoltage Protection Operation (continued)**

| Status | Condition | Action |
|---|---|---|
| Latch Reset | *SafetyStatus()[COVL]* = 1 for ***Protections:COVL:Recovery Time*** duration | *Safety Status C()[COVL]* = 0<br>Reset COVL counter<br>*Alarm Raw Status()[XCHG]* = 0 if *Safety Status A()[COV]* = 0 and autonomous FET control is enabled |

When a COV fault is triggered, a snapshot of all cell voltages is captured and can be accessed through the *0x0081 COV_SNAPSHOT()* subcommand, which has format as shown below.

**Table 17. *0x0081 COV_SNAPSHOT()* Subcommand Format**

| Subcommand Address | Bytes within Block | Name | Unit |
|---|---|---|---|
| 0x0081 | 0 - 1 | Cell 1 Voltage at COV | mV |
| | 2 - 3 | Cell 2 Voltage at COV | mv |
| | 4 - 5 | Cell 3 Voltage at COV | mV |
| | 6 - 7 | Cell 4 Voltage at COV | mV |
| | 8 - 9 | Cell 5 Voltage at COV | mV |
| | 10 - 11 | Cell 6 Voltage at COV | mV |
| | 12 - 13 | Cell 7 Voltage at COV | mV |
| | 14 - 15 | Cell 8 Voltage at COV | mV |
| | 16 - 17 | Cell 9 Voltage at COV | mV |
| | 18 - 19 | Cell 10 Voltage at COV | mV |
| | 20 - 31 | Reserved | - |

#### *7.3.4.4 Cell Undervoltage Protection*

The BQ76942 device integrates Cell Undervoltage Protection (CUV), monitoring the voltage of every cell using a comparator-based circuit, and triggering a CUV alert or fault when a cell voltage falls below the CUV threshold. The CUV threshold is programmable from 1.0 V to 4.5 V in 50 mV steps and is set by the ***Protections:CUV:Threshold*** configuration register. The CUV protection is enabled using the ***Settings:Protection:Enabled Protections A:[CUV]*** configuration bit.

The CUV circuitry triggers an alert signal when an undervoltage event is first detected, then will trigger a fault after a programmable detection delay, CUV_DLY, which can be set from 10 ms to 6765 ms in units of 3.3 ms, with the actual delay being 3.3ms × (2 + setting). The setting 0x0 disables the protection. The delay is set by the ***Protections:CUV:Delay*** configuration register.

When a CUV fault is triggered, the fault will recover if the voltage rises above the CUV threshold by a value of CUV_HYS, which is programmable from 100 mV to 1 V in steps of 50 mV, for ***Protections:Recovery:Time***. This hysteresis level is set by the ***Protections:CUV:Recovery Hysteresis*** configuration register.

When CUV is triggered, the device will turn off the DSG FET if configured for autonomous FET control based on setting in ***Settings:Protection:DSG FET Protections A[CUV]*** (the CHG FET remains enabled if already enabled). The device will recover (if configured for autonomous recovery) based on all cell voltages being above CUV threshold + CUV_HYS. Further detail is described in the table below. Note: timing on CUV changes while cell balancing is active, as described in Table 34

**Table 18. Undervoltage Protection Operation**

| Status | Condition | Action |
|---|---|---|
| Normal | Min cell voltage > ***Protections:CUV:Threshold*** | *Safety Alert A()[CUV]* = 0 |
| Alert | Min cell voltage ≤ ***Protections:CUV:Threshold*** | *Safety Alert A()[CUV]* = 1 |

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**Table 18. Undervoltage Protection Operation (continued)**

| Status | Condition | Action |
|---|---|---|
| Trip | Min cell voltage ≤ ***Protections:CUV:Threshold*** for ***Protections:CUV:Delay*** duration | *Safety Alert A()[CUV]* = 0<br>*Safety Status A()[CUV]* = 1<br>*Alarm Raw Status()[XDSG]* = 1 if configured for autonomous FET control |
| Recovery | *Safety Status A()[CUV]* = 1 and<br>Min cell voltage > ***Protections:CUV:Threshold*** + ***Protections:CUV:Recovery Hysteresis*** for ***Protections:Recovery:Time*** | *Safety Status A()[CUV]* = 0<br>*Alarm Raw Status()[XDSG]* = 0 if configured for autonomous FET control |

When a CUV fault is triggered, a snapshot of all cell voltages is captured and can be accessed through the *0x0080 CUV_SNAPSHOT()* subcommand, which has format as shown below.

**Table 19. *0x0080 CUV_SNAPSHOT()* Subcommand Format**

| Subcommand Address | Bytes within Block | Name | Unit |
|---|---|---|---|
| 0x0080 | 0 - 1 | Cell 1 Voltage at CUV | mV |
| | 2 - 3 | Cell 2 Voltage at CUV | mv |
| | 4 - 5 | Cell 3 Voltage at CUV | mV |
| | 6 - 7 | Cell 4 Voltage at CUV | mV |
| | 8 - 9 | Cell 5 Voltage at CUV | mV |
| | 10 - 11 | Cell 6 Voltage at CUV | mV |
| | 12 - 13 | Cell 7 Voltage at CUV | mV |
| | 14 - 15 | Cell 8 Voltage at CUV | mV |
| | 16 - 17 | Cell 9 Voltage at CUV | mV |
| | 18 - 19 | Cell 10 Voltage at CUV | mV |
| | 20 - 31 | Reserved | - |

#### *7.3.4.5 Short Circuit in Discharge Protection*

The BQ76942 device integrates Short Circuit in Discharge Protection (SCD) using a dedicated comparator that monitors the differential voltage across the SRN - SRP pins and triggers an SCD alert or fault when the voltage exceeds a programmable threshold VSCD. The VSCD threshold is programmable as 10 mV, 20 mV, 40 mV, 60 mV, 80 mV, 100 mV, 125 mV, 150 mV, 175 mV, 200 mV, 250 mV, 300 mV, 350 mV, 400 mV, 450 mV, and 500 mV, and is set by the ***Protections:SCD:Threshold*** configuration register. The SCD protection is enabled using the ***Settings:Protection:Enabled Protections A:[SCD]*** configuration bit.

The SCD circuitry triggers an alert signal when a short circuit event is first detected, then will trigger a fault after a programmable detection delay, SCD_DLY, which can be set to fastest, or 15 µs to 450 µs in steps of 15 µs. The fastest setting can result in detection of a short circuit with only comparator delay, which may be < 1 µs depending on the overdrive of the threshold. The setting 0x0 disables the protection. The delay is set by the ***Protections:SCD:Delay*** configuration register.

When an SCD fault is triggered, the device will turn off the DSG FET if configured for autonomous FET control in ***Settings:Protection:DSG FET Protections A***. The CHG FET may also be disabled autonomously based on setting in ***Settings:Protection:CHG FET Protections A***. The device will recover (if configured for autonomous recovery) after a programmable delay given by ***Protections:SCD:Recovery Time***.

The BQ76942 device also includes a Short Circuit in Discharge Latch (SCDL) protection, which can create a fault and Permanent Fail (PF) if multiple SCD failures occur within a programmable time window. Whenever an SCD fault is triggered, the SCDL latch counter is incremented. After the device recovers, it will decrement the SCDL counter after a programmable time of ***Protections:SCDL:Counter Dec Delay*** if no further SCD faults are detected. If the SCDL counter reaches a programmable latch limit given by ***Protections:SCDL:Latch Limit***, it will trigger an SCDL fault and can also trigger an SCDL PF.

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The SCDL protection is enabled using the ***Settings:Protection:Enabled Protections C:[SCDL]*** configuration bit. If the SCDL protection fault is triggered, the device can recover if the load detect feature (see Load Detect Functionality) is enabled and detects the load is removed, or if charging current is detected, or after a programmable time, or the host sends a *0x009C SCDL_RECOVER()* subcommand. In order to recover based on charging current, the ***Settings:Protection:Protection Configuration[SCDL_CURR_RECOV]*** must be set, the device must be in series FET configuration, and the CHG FET must be enabled. The device will then recover from SCDL if a current is detected greater than or equal to ***Protections:SCDL:Recovery Threshold*** for ***Protections:SCDL:Recovery Time*** duration. If recovery is preferred based only on time, then the recovery based on charging current can be used, with the current threshold set to a small discharge current.

Further detail is described in the table below.

**Table 20. Short Circuit in Discharge Protection Operation**

| Status | Condition | Action |
|---|---|---|
| Normal | $V_{SRN}$ - $V_{SRP}$ ≤ setting selected by***Protections:SCD:Threshold*** | *Safety Alert A()[SCD]* = 0<br>*PF Alert B()[SCDL]* = 0<br>Decrement SCDL counter by one after each ***Protections:SCDL:Counter Dec Delay*** period if SCDL counter > 0 |
| Alert | $V_{SRN}$ - $V_{SRP}$ > setting selected by***Protections:SCD:Threshold*** | *Safety Alert A()[SCD]* = 1 |
| Trip | $V_{SRN}$ - $V_{SRP}$ > setting selected by***Protections:SCD:Threshold*** for ***Protections:SCD:Delay*** duration | *Safety Alert A()[SCD]* = 0<br>*Safety Status A()[SCD]* = 1<br>*Alarm Raw Status()[XDSG]* = 1 if autonomous FET control is enabled<br>*Alarm Raw Status()[XCHG]* = 1 depending on setting<br>Increment SCDL counter |
| Recovery | *Safety Status A()[SCD]* = 1 and<br>$V_{SRN}$ - $V_{SRP}$ ≤ setting selected by***Protections:SCD:Threshold*** for ***Protections:SCD:Recovery Time*** duration | *Safety Status A()[SCD]* = 0<br>*Alarm Raw Status()[XDSG]* = 0 if autonomous FET control is enabled<br>*Alarm Raw Status()[XCHG]* = 0 depending on setting |
| Latch Alert | SCDL counter > 0 | *Safety Alert C()[SCDL]* = 1<br>*PF Alert B()[SCDL]* = 1 |
| Latch Trip | SCDL counter ≥ ***Protections:SCDL:Latch Limit*** | *Safety Status C()[SCDL]* = 1<br>*PF Status B()[SCDL]* = 1<br>*PF Alert B()[SCDL]* = 1<br>*Safety Alert C()[SCDL]* = 0<br>*Alarm Raw Status()[XDSG]* = 1 if autonomous FET control is enabled<br>*Alarm Raw Status()[XCHG]* = 1 depending on setting |
| Latch Reset (based on Load Detect) | *Safety Status C()[SCDL]* = 1 and load is detected removed using the Load Detect function | *Safety Status C()[SCDL]* = 0<br>Reset SCDL counter<br>*Alarm Raw Status()[XDSG]* = 0 and *Alarm Raw Status()[XCHG]* = 0<br>if *Safety Status A()[SCD]* = 0 and autonomous FET control is enabled |
| Latch Reset (based on charging current and time) | *Safety Status C()[SCDL]* = 1 and CC1 Current ≥ ***Protections:SCDL:Recovery Threshold*** for ***Protections:SCDL:Recovery Time*** duration, if ***Settings:Protection:Protection Configuration[SCDL_CURR_RECOV]*** = 1 | *Safety Status C()[SCDL]* = 0<br>Reset SCDL counter<br>*Alarm Raw Status()[XDSG]* = 0 and *Alarm Raw Status()[XCHG]* = 0<br>if *Safety Status A()[SCD]* = 0 and autonomous FET control is enabled |

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**Table 20. Short Circuit in Discharge Protection Operation (continued)**

| Status | Condition | Action |
|---|---|---|
| Latch Reset (host-command) | *Safety Status C()[SCDL]* = 1 and host sends *0x009C SCDL_RECOVER()* | *Safety Status C()[SCDL]* = 0<br>Reset SCDL counter<br>*Alarm Raw Status()[XDSG]* = 0 and *Alarm Raw Status()[XCHG]* = 0<br>if *Safety Status A()[SCD]* = 0 and autonomous FET control is enabled |

### 7.3.4.6 Overcurrent in Charge Protection

The BQ76942 device integrates Overcurrent in Charge Protection (OCC) using a comparator that monitors the differential voltage across the SRP - SRN pins and triggers an OCC alert or fault when the voltage exceeds a programmable threshold VOCC. The VOCC threshold is programmable from 4 mV to 124 mV in 2 mV steps using the ***Protections:OCC:Threshold*** configuration register. The OCC protection is enabled using the ***Settings:Protection:Enabled Protections A:[OCC]*** configuration bit.

The OCC circuitry triggers an alert signal when an overcurrent in charge event is first detected, then will trigger a fault after a programmable detection delay, OCC_DLY, which can be set from 10 ms to 426 ms in units of 3.3 ms, with the actual delay being 3.3 ms × (2 + setting). The setting 0x0 disables the protection. The delay is set by the ***Protections:OCC:Delay*** configuration register.

When an OCC fault is triggered, the device will turn off the CHG FET if configured for autonomous FET control using ***Settings:Protection:CHG FET Protections A.*** (the DSG FET may remain enabled if already enabled). The device will recover (if configured for autonomous recovery) when the voltage measured on the PACK pin falls at least ***Protections:OCC:PACK-TOS Delta*** below the voltage measured at the top-of-stack for a duration of ***Protections:Recovery:Time***, or a current less than or equal to ***Protections:OCC:Recovery Threshold*** (that is, a discharge current) is present for a duration of ***Protections:Recovery:Time***.

Further detail is described in the table below.

**Table 21. Overcurrent in Charge Protection Operation**

| Status | Condition | Action |
|---|---|---|
| Normal | $V_{SRP}$ - $V_{SRN}$ ≤ setting selected by ***Protections:OCC:Threshold*** | *Safety Alert A()[OCC]* = 0 |
| Alert | $V_{SRP}$ - $V_{SRN}$ > setting selected by ***Protections:OCC:Threshold*** | *Safety Alert A()[OCC]* = 1 |
| Trip | $V_{SRP}$ - $V_{SRN}$ > setting selected by ***Protections:OCC:Threshold*** for ***Protections:OCC:Delay*** duration | *Safety Alert A()[OCC]* = 0<br>*Safety Status A()[OCC]* = 1<br>*Alarm Raw Status()[XCHG]* = 1 if autonomous FET control is enabled |
| Recovery (charger detached) | *Safety Status A()[OCC]* = 1 and<br>*PACK Voltage()* ≤ *Stack Voltage()* - ***Protections:OCC:PACK-TOS Delta*** or<br>CC1 Current ≤ ***Protections:OCC:Recovery Threshold*** for ***Protections:Recovery:Time*** duration. | *Safety Status A()[OCC]* = 0<br>*Alarm Raw Status()[XCHG]* = 0 if autonomous FET control is enabled |

### 7.3.4.7 Overcurrent in Discharge 1, 2, and 3 Protections

The BQ76942 device integrates Overcurrent in Discharge 1 (OCD1) and Overcurrent in Discharge 2 (OCD2) Protections using a comparator that monitors the differential voltage across the SRN - SRP pins and triggers an OCD1 or OCD2 alert or fault when the voltage exceeds a programmable threshold VOCD1 or VOCD2. The VOCD1 and VOCD2 thresholds are independently programmable from 4 mV to 124 mV in 2 mV steps using the ***Protections:OCD1:Threshold*** and ***Protections:OCD2:Threshold*** configuration registers. The OCD1 and OCD2 protections are enabled using the ***Settings:Protection:Enabled Protections A:[OCD1]*** and ***Settings:Protection:Enabled Protections A:[OCD2]*** configuration bits.

The OCD1 and OCD2 circuitry triggers an alert signal when an overcurrent in discharge event is first detected, then will trigger a fault when this condition persists for a programmable detection delay, OCD1_DLY or OCD2_DLY, which can be independently set from 10 ms to 426 ms in units of 3.3 ms, with the actual delay being 3.3 ms × (2 + setting). The setting 0x0 disables the protection. The delay is set by the ***Protections:OCD1:Delay*** and ***Protections:OCD2:Delay*** configuration registers.

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The device also integrates an Overcurrent in Discharge 3 (OCD3) Protection using the CC1 current measurement from the coulomb counter ADC, triggering an OCD3 alert or fault when the current is more negative (that is, an excessive discharge current) than a programmable threshold given by ***Protections:OCD3:Threshold***. An alert signal is triggered when an overcurrent in discharge event is first detected, then a fault signal is triggered when this condition persists for a programmable detection delay, OCD3_DLY, which can be set from 0 sec to 255 sec in units of 1 sec. The delay is set by the ***Protections:OCD3:Delay*** configuration register. The OCD3 protection is enabled using the ***Settings:Protection:Enabled Protections C:[OCD3]*** configuration bit.

When an OCD1, OCD2, or OCD3 fault is triggered, the device will turn off the DSG FET if configured for autonomous FET control using ***Settings:Protection:DSG FET Protections A[OCD2][OCD1]*** or ***Settings:Protection:DSG FET Protections C[OCD3]*** configuration bits. The device will recover when a charging current is detected greater than or equal to ***Protections:OCD:Recovery Threshold*** for ***Protections:Recovery:Time*** duration.

The BQ76942 device also includes an Overcurrent in Discharge Latch (OCDL) protection, which can create a fault if multiple OCD1 or OCD2 or OCD3 failures occur within a programmable time window. Whenever an OCD1 or OCD2 or OCD3 fault is triggered, the OCDL latch counter is incremented. After the device recovers, it will decrement the OCDL counter after a programmable recovery time of ***Protections:OCDL:Counter Dec Delay*** if no further OCD1 or OCD2 or OCD3 faults are detected. If the OCDL counter exceeds a programmable latch limit given by ***Protections:OCDL:Latch Limit***, it will trigger an OCDL fault. An OCDL alert is generated whenever the OCDL counter is greater than zero.

The OCDL protection is enabled using the ***Settings:Protection:Enabled Protections C:[OCDL]*** configuration bit. If the OCDL protection fault is triggered, the device can recover if the load detect feature (see Load Detect Functionality) is enabled and detects the load is removed, or if charging current is detected, or after a programmable time, or the host sends a *0x009B OCDL_RECOVER()* subcommand. In order to recover based on charging current, the ***Settings:Protection:Protection Configuration[OCDL_CURR_RECOV]*** must be set, the device must be in series FET configuration, and the CHG FET must be enabled. The device will then recover from OCDL if a current is detected greater than or equal to ***Protections:OCDL:Recovery Threshold*** for ***Protections:OCDL:Recovery Time*** duration. If recovery is preferred based only on time, then the recovery based on charging current can be used, with the current threshold set to a small discharge current.

Further detail is described in the table below.

**Table 22. Overcurrent in Discharge 1, 2 and 3 Protection Operation**

| Status | Condition | Action |
|---|---|---|
| Normal | $V_{SRN}$ - $V_{SRP}$ ≤ setting selected by ***Protections:OCD1:Threshold***<br>$V_{SRN}$ - $V_{SRP}$ ≤ setting selected by ***Protections:OCD2:Threshold***<br>CC1 Current > ***Protections:OCD3:Threshold*** | *Safety Alert A()[OCD1]* = 0<br>*Safety Alert A()[OCD2]* = 0<br>*Safety Alert C()[OCD3]* = 0<br>Decrement OCDL counter by one after each ***Protections:OCDL:Counter Dec Delay*** period if OCDL counter > 0 |
| Alert | $V_{SRN}$ - $V_{SRP}$ > setting selected by ***Protections:OCD1:Threshold*** | *Safety Alert A()[OCD1]* = 1 |
| Alert | $V_{SRN}$ - $V_{SRP}$ > setting selected by ***Protections:OCD2:Threshold*** | *Safety Alert A()[OCD2]* = 1 |
| Alert | CC1 Current ≤ ***Protections:OCD3:Threshold*** | *Safety Alert C()[OCD3]* = 1 |
| Trip | $V_{SRN}$ - $V_{SRP}$ > setting selected by ***Protections:OCD1:Threshold*** for ***Protections:OCD1:Delay*** duration | *Safety Alert A()[OCD1]* = 0<br>*Safety Status A()[OCD1]* = 1<br>*Alarm Raw Status()[XDSG]* = 1 if autonomous FET control is enabled;<br>Increment OCDL counter |
| Trip | $V_{SRN}$ - $V_{SRP}$ > setting selected by ***Protections:OCD2:Threshold*** for ***Protections:OCD2:Delay*** duration | *Safety Alert A()[OCD2]* = 0<br>*Safety Status A()[OCD2]* = 1<br>*Alarm Raw Status()[XDSG]* = 1 if autonomous FET control is enabled;<br>Increment OCDL counter |

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**Table 22. Overcurrent in Discharge 1, 2 and 3 Protection Operation (continued)**

| Status | Condition | Action |
|---|---|---|
| Trip | CC1 Current ≤ ***Protections:OCD3:Threshold*** for ***Protections:OCD3:Delay*** duration | *Safety Alert C()[OCD3]* = 0<br>*Safety Status C()[OCD3]* = 1<br>*Alarm Raw Status()[XDSG]* = 1 if autonomous FET control is enabled;<br>Increment OCDL counter |
| Recovery | *Safety Status A()[OCD1]* = 1 or *Safety Status A()[OCD2]* = 1 or *Safety Status C()[OCD3]* = 1 and CC1 Current > ***Protections:OCD:Recovery Threshold*** for ***Protections:Recovery:Time*** duration | *Safety Status A()[OCD1]* = 0<br>*Safety Status A()[OCD2]* = 0<br>*Safety Status C()[OCD3]* = 0<br>*Alarm Raw Status()[XDSG]* = 0 |
| Latch Alert | OCDL counter > 0 | *Safety Alert C()[OCDL]* = 1 |
| Latch Trip | OCDL counter ≥ ***Protections:OCDL:Latch Limit*** | *Safety Status C()[OCDL]* = 1<br>*Safety Alert C()[OCDL]* = 0<br>*Alarm Raw Status()[XDSG]* = 1 if autonomous FET control is enabled; |
| Latch Reset (based on Load Detect) | *Safety Status C()[OCDL]* = 1 and load is detected removed using the Load Detect function | *Safety Status C()[OCDL]* = 0<br>Reset OCDL counter<br>*Alarm Raw Status()[XDSG]* = 0 if *Safety Status A()[OCD1]* = 0 and *Safety Status A()[OCD2]* = 0 and *Safety Status C()[OCD3]* = 0 |
| Latch Reset (based on charging current) | *Safety Status C()[OCDL]* = 1 and CC1 Current > ***Protections:OCDL:Recovery Threshold*** | *Safety Status C()[OCDL]* = 0<br>Reset OCDL counter<br>*Alarm Raw Status()[XDSG]* = 0 if *Safety Status A()[OCD1]* = 0 and *Safety Status A()[OCD2]* = 0 and *Safety Status C()[OCD3]* = 0 |
| Latch Reset (host-command) | *Safety Status C()[OCDL]* = 1 and host sends *0x009B OCDL_RECOVER()* | *Safety Status C()[OCDL]* = 0<br>Reset OCDL counter<br>*Alarm Raw Status()[XDSG]* = 0 if *Safety Status A()[OCD1]* = 0 and *Safety Status A()[OCD2]* = 0 and *Safety Status C()[OCD3]* = 0 |

#### *7.3.4.8 Overtemperature in Charge Protection*

The BQ76942 device integrates an Overtemperature in Charge (OTC) Protection that triggers an alert or fault when the cell temperature is greater than or equal to a programmable threshold TOTC. The TOTC threshold is programmable from -40°C to 120°C in 1°C steps using the ***Protections:OTC:Threshold*** configuration register. The OTC protection is enabled using the ***Settings:Protection:Enabled Protections B:[OTC]*** configuration bit.

The OTC protection triggers an alert signal when an overtemperature in charge event is first detected, then will trigger a fault after a programmable detection delay, OTC_DLY, which can be set from 0-sec to 255-sec in units of 1-sec. The delay is set by the ***Protections:OTC:Delay*** configuration register.

When an OTC fault is triggered, the device will turn off the CHG FET if configured for autonomous FET control, based on the setting in ***Settings:Protection:CHG FET Protections B[OTC].*** The device will recover when the temperature is less than or equal to the threshold set by ***Protections:OTC:Recovery*** for ***Protections:Recovery:Time*** duration.

The temperature used by the OTC protection is the maximum of all temperature readings that are designated for cell temperature, and can include the internal temperature measurement as well as all external thermistors which are enabled.

#### *7.3.4.9 Overtemperature in Discharge Protection*

The BQ76942 device integrates an Overtemperature in Discharge (OTD) Protection that triggers an alert or fault when the cell temperature is greater than or equal to a programmable threshold TOTD. The TOTD threshold is programmable from -40°C to 120°C in 1°C steps using the ***Protections:OTD:Threshold*** configuration register. The OTD protection is enabled using the ***Settings:Protection:Enabled Protections B:[OTD]*** configuration bit.

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The OTD protection triggers an alert signal when an overtemperature in discharge event is first detected, then will trigger a fault after a programmable detection delay, OTD_DLY, which can be set from 0-sec to 255-sec in units of 1-sec. The delay is set by the ***Protections:OTD:Delay*** configuration register.

When an OTD fault is triggered, the device will turn off the DSG FET if configured for autonomous FET control, based on the setting in ***Settings:Protection:DSG FET Protections B[OTD]***. The device will recover when the temperature is less than or equal to the temperature set by ***Protections:OTD:Recovery*** for ***Protections:Recovery:Time*** duration.

The temperature used by the OTD protection is the maximum of all temperature readings that are designated for cell temperature, and can include the internal temperature measurement as well as all external thermistors which are enabled.

#### *7.3.4.10 Overtemperature FET Protection*

The BQ76942 device integrates an Overtemperature FET (OTF) Protection that triggers an alert or fault when the FET temperature is greater than or equal to a programmable threshold TOTF. The TOTF threshold is programmable from 0°C to 150°C in 1°C steps using the ***Protections:OTF:Threshold*** configuration register. The OTF protection is enabled using the ***Settings:Protection:Enabled Protections B:[OTF]*** configuration bit.

The OTF protection triggers an alert signal when an overtemperature FET event is first detected, then will trigger a fault after a programmable detection delay, OTF_DLY, which can be set from 0-sec to 255-sec in units of 1-sec. The delay is set by the ***Protections:OTF:Delay*** configuration register.

When an OTF fault is triggered, the device will turn off the DSG FET, the CHG FET, or both FETs if configured for autonomous FET control, based on settings in ***Settings:Protection:DSG FET Protections B[OTF]*** and ***Settings:Protection:CHG FET Protections B[OTF]***. The device will recover (if configured for autonomous recovery) when the temperature is less than or equal to the threshold set by ***Protections:OTF:Recovery*** for ***Protections:Recovery:Time*** duration.

The temperature used by the OTF protection is the maximum of all temperature readings that are designated for FET temperature, and can include the internal temperature measurement as well as all external thermistors which are enabled.

#### *7.3.4.11 Internal Overtemperature Protection*

The BQ76942 device integrates an Internal Overtemperature (OTINT) Protection that triggers an alert or fault when the internal temperature is greater than or equal to a programmable threshold TOTINT. The TOTINT threshold is programmable from -40°C to 120°C in 1°C steps using the ***Protections:OTINT:Threshold*** configuration register. The OTINT protection is enabled using the ***Settings:Protection:Enabled Protections B:[OTINT]*** configuration bit.

The OTINT protection triggers an alert signal when an internal overtemperature event is first detected, then will trigger a fault after a programmable detection delay, OTINT_DLY, which can be set from 0-sec to 255-sec in units of 1-sec. The delay is set by the ***Protections:OTINT:Delay*** configuration register.

When an OTINT fault is triggered, the device will turn off the DSG FET, the CHG FET, or both FETs if configured for autonomous FET control, based on settings in ***Settings:Protection:DSG FET Protections B[OTINT]*** and ***Settings:Protection:CHG FET Protections B[OTINT]***. The device will recover (if configured for autonomous recovery) when the temperature is less than or equal to the threshold set by ***Protections:OTINT:Recovery*** for ***Protections:Recovery:Time*** duration.

#### *7.3.4.12 Undertemperature in Charge Protection*

The BQ76942 device integrates an Undertemperature in Charge (UTC) Protection that triggers an alert or fault when the cell temperature is less than or equal to a programmable threshold TUTC. The TUTC threshold is programmable from -40°C to 120°C in 1°C steps using the ***Protections:UTC:Threshold*** configuration register. The UTC protection is enabled using the ***Settings:Protection:Enabled Protections B:[UTC]*** configuration bit.

The UTC protection triggers an alert signal when an undertemperature in charge event is first detected, then will trigger a fault after a programmable detection delay, UTC_DLY, which can be set from 0-sec to 255-sec in units of 1-sec. The delay is set by the ***Protections:UTC:Delay*** configuration register.

When a UTC fault is triggered, the device will turn off the CHG FET if configured for autonomous FET control, based on the setting in ***Settings:Protection:CHG FET Protections B[UTC]***. The device will recover when the temperature is greater than or equal to the threshold set by ***Protections:UTC:Recovery*** for ***Protections:Recovery:Time*** duration.

The temperature used by the UTC protection is the minimum of all temperature readings that are designated for cell temperature, and can include the internal temperature measurement as well as all external thermistors which are enabled.

#### *7.3.4.13 Undertemperature in Discharge Protection*

The BQ76942 device integrates an Undertemperature in Discharge (UTD) Protection that triggers an alert or fault when the cell temperature is less than or equal to a programmable threshold TUTD. The TUTD threshold is programmable from -40°C to 120°C in 1°C steps using the ***Protections:UTD:Threshold*** configuration register. The UTD protection is enabled using the ***Settings:Protection:Enabled Protections B:[UTD]*** configuration bit.

The UTD protection triggers an alert signal when an undertemperature in charge event is first detected, then will trigger a fault after a programmable detection delay, UTD_DLY, which can be set from 0-sec to 255-sec in units of 1-sec. The delay is set by the ***Protections:UTD:Delay*** configuration register.

When a UTD fault is triggered, the device will turn off the DSG FET if configured for autonomous FET control, based on the setting in ***Settings:Protection:DSG FET Protections B[UTD]***. The device will recover when the temperature is greater than or equal to the threshold set by ***Protections:UTD:Recovery*** for ***Protections:Recovery:Time*** duration.

The temperature used by the UTD protection is the minimum of all temperature readings that are designated for cell temperature, and can include the internal temperature measurement as well as all external thermistors which are enabled.

#### *7.3.4.14 Internal Undertemperature Protection*

The BQ76942 device integrates an Internal Undertemperature (UTINT) Protection that triggers an alert or fault when the internal temperature is less than or equal to a programmable threshold TUTINT. The TUTINT threshold is programmable from -40°C to 120°C in 1°C steps using the ***Protections:UTINT:Threshold*** configuration register. The UTINT protection is enabled using the ***Settings:Protection:Enabled Protections B:[UTINT]*** configuration bit.

The UTINT protection triggers an alert signal when an undertemperature in charge event is first detected, then will trigger a fault after a programmable detection delay, UTINT_DLY, which can be set from 0-sec to 255-sec in units of 1-sec. The delay is set by the ***Protections:UTINT:Delay*** configuration register.

When a UTINT fault is triggered, the device will turn off the DSG FET, the CHG FET, or both FETs if configured for autonomous FET control, based on settings in ***Settings:Protection:DSG FET Protections B[UTINT]*** and ***Settings:Protection:CHG FET Protections B[UTINT]***. The device will recover (if configured for autonomous recovery) when the temperature is less than or equal to the threshold set by ***Protections:UTINT:Recovery*** for ***Protections:Recovery:Time*** duration.

#### *7.3.4.15 Host Watchdog Protection*

The BQ76942 device integrates a Host Watchdog (HWD) Protection that triggers a fault when no communications are received for a programmable delay HWD_DLY. The HWD_DLY delay is programmable from 0-sec to 255-sec in 1-sec steps using the ***Protections:HWD:Delay*** configuration register. The HWD protection is enabled using the ***Settings:Protection:Enabled Protections C:[HWDF]*** configuration bit.

When an HWD fault is triggered, the device will turn off the DSG FET, the CHG FET, or both FETs if configured for autonomous FET control, based on settings in ***Settings:Protection:DSG FET Protections C[HWDF]*** and ***Settings:Protection:CHG FET Protections C[HWDF]***. The device will recover (if configured for autonomous recovery) when valid communications are received.

If there is a concern that the HWD fault is caused by the host processor no longer operating properly, the BQ76942 device can be configured to disable or toggle the external REG1 and REG2 LDOs when the fault occurs. Based on ***Settings:Configuration:HWD Regulator Options***, the device can either leave the LDOs unchanged, disable the LDOs indefinitely, or disable the LDOs for a time period up to 15-sec, then re-enable them again. This is controlled using the ***Settings:Configuration:HWD Regulator Options*** configuration register.

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Note: if the toggling is enabled and the device disables the LDOs after a HWD fault, after the toggle delay is completed the device will recover the LDOs to their state in ***Settings:REG12 Config[REG1_EN] and [REG2_EN]***, which may not be their state when the HWD fault occurred.

#### *7.3.4.16 Precharge Timeout Protection*

The BQ76942 device integrates a Precharge Timeout (PTO) Protection that triggers a fault when the device has been in precharge mode for a time duration PTO_DLY. The PTO_DLY duration is programmable from 0-sec to 65535-sec in 1-sec steps using the ***Protections:PTO:Delay*** configuration register. The timer for PTO_DLY only increments while the device is in precharge mode and the CC1 current exceeds a threshold given by ***Protections:PTO:Charge Threshold***. When the device is in precharge mode and the current is less than or equal to this threshold, the *Safety Alert C()[PTOS]* bit is set (which stands for Precharge Timeout Suspend). The PTO timer is reset if a continuous discharge occurs with current larger in magnitude than ***Settings:Current Thresholds:Dsg Current Threshold*** and an amount of charge is accumulated equal or greater than a programmable level given by ***Protections:PTO:Reset***. The PTO protection is enabled using the ***Settings:Protection:Enabled Protections C:[PTO]*** configuration bit.

When a PTO fault is triggered, the device will turn off the PCHG FET if configured for autonomous FET control, based on the setting in ***Settings:Protection:CHG FET Protections C[PTO]***and enable the CHG FET for normal charging, if no other condition is present which would block this.

#### *7.3.4.17 Load Detect Functionality*

When a Short Circuit in Discharge Latch or Overcurrent in Discharge Latch protection fault has occurred and the DSG FET is off, the device can be configured to recover when load removal is detected. This feature is useful if the system has a removable pack, such that the user can remove the pack from the system when a fault occurs, or if the effective system load that remains on the battery pack is higher than ≈20-kΩ when the DSG FET is disabled. The device will periodically enable a current source out the LD pin and will recover the fault if a voltage is detected at the LD pin above a 3 V level. If a low-impedance load is still present on the pack, the voltage the device measures on the LD pin will generally be below 3 V, preventing recovery based on Load Detect. If the pack has been removed from the system and the effective load is high, such that the current source generates a voltage on the LD pin above a 3 V level, then the device can recover from the fault. Note: typically a 10-kΩ resistor is connected between the PACK+ terminal and the LD pin, this resistance should be comprehended when considering the load impedance.

The Load Detect current is enabled for a time duration given by ***Protections:Load Detect:Active Time***, then is disabled for a time duration given by ***Protections:Load Detect:Retry Delay***, with this sequence repeating until the load has been detected as removed, or the accumulated time reaches ***Protections:Load Detect:Timeout***. The timeout is included to prevent the device continuously attempting Load Detect indefinitely and causing long-term drain on the pack. If the timeout is met, the Load Detect function will no longer operate until the latched faults have recovered through another means, or the *0x009D LOAD_DETECT_RESTART()*subcommand to restart the Load Detect is received.

If the ***Protections:Load Detect:Active Time*** is set to 0, then the Load Detect function is disabled. If the ***Protections:Load Detect:Retry Delay*** is set to 0, then the Load Detect current source will remain on continuously until timeout or recovery occurs.

The Load Detect current can be forced on or off through subcommands. If the ***Protections:Load Detect:Active Time*** is set to 0 and the *0x009E LOAD_DETECT_ON()* subcommand is sent, the Load Detect current source will be enabled. If the *0x009F LOAD_DETECT_OFF()* subcommand is sent, the Load Detect current source will be disabled.

When an SCDL or OCDL fault occurs and the DSG FET is disabled, the device may enter SLEEP mode, in which measurements of the LD pin voltage are only taken at intervals given by ***Power:Sleep:Voltage Time***. It is recommended to set the ***Protections:Load Detect:Active Time*** longer than ***Power:Sleep:Voltage Time***, to be sure that during each window when the current source is enabled, at least one measurement of the LD pin voltage will occur. The status of the Load Detect function is provided in *0x00 Control Status()[LD_TIMEOUT, LD_ON]*.

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### *7.3.4.18 Protection FETs*

#### 7.3.4.18.1 FET Configuration

The BQ76942 device supports both a series configuration and a parallel configuration for the protection FETs in the system, as well as a system which does not use one or both FETs. If the device FET drivers are not used at all, the charge pump should be disabled by clearing ***Settings:FET:Chg Pump Control[CPEN]*** and clearing ***Settings:FET:FET Options[FET_CTRL_EN].*** The ***Settings:FET:FET Options[SFET]*** configuration bit should be set when FETs are used in a series configuration, and should be cleared if FETs are used in a parallel configuration. If the system will only use a single FET (such as a CHG FET with no DSG FET), the device can be configured for parallel configuration with the DFETF Permanent Fail disabled.

When a series FET configuration is used, the BQ76942 device provides body diode protection for the case when one FET is off and one FET is on. This situation might occur in SLEEP mode (when the DSG FET is on and the CHG FET may be off) or in a cell undervoltage fault condition, when the DSG FET may be off, but the CHG FET may still be on.

If the CHG FET is off, the DSG or PDSG FET is on, and a discharge current greater in magnitude than***Settings:Protection:Body Diode Threshold*** (that is, a significant discharging current) is detected, the device will turn on the CHG FET, to avoid current flowing through the CHG FET body diode and damaging the FET. When the current rises above the threshold (that is, less discharge current flowing), the CHG FET will be turned off again if the reasons for its turn-off are still present.

If the DSG FET is off, the CHG or PCHG FET is on, and a current in excess of +***Settings:Protection:Body Diode Threshold*** (that is, a significant charging current) is detected, the device will turn on the DSG FET, to avoid current flowing through the DSG FET body diode and damaging the FET. When the current falls below the threshold (that is, less charging current flowing), the DSG FET will be turned off again if the reasons for its turn-off are still present.

When a parallel configuration is used (***Settings:FET:FET Options[SFET]*** = 0), the body diode protection is disabled.

#### 7.3.4.18.2 FET Control

The protection FETs can be controlled in several different ways, depending on system requirements. If FETs will not be used in the system or driven from the device, the ***Settings:FET:FET Options[FET_CTRL_EN]*** bit can be cleared, and the charge pump disabled by clearing the ***Settings:FET:Chg Pump Control[CPEN]*** bit.

The device includes a FET Test mode for use during manufacturing, in which the device will not enable the FETs unless FET Test subcommands are sent. The device may still enable FETs based on body diode protection in this mode. The device is put into FET Test mode by clearing ***Settings:Manufacturing:Mfg Status Init[FET_EN]***. The *0x0022 FET_EN_TOGGLE()* subcommand can be used to toggle the [FET_EN] bit setting. The FET Test subcommands are shown below.

**Table 23. FET Test Mode Subcommands**

| Subcommand | Description |
|---|---|
| 0x001C PDSGTEST() | Only functional in FET Test mode, toggles PDSG FET state |
| 0x001E PCHGTEST() | Only functional in FET Test mode, toggles PCHG FET state |
| 0x001F CHGTEST() | Only functional in FET Test mode, toggles CHG FET state |
| 0x0020 DSGTEST() | Only functional in FET Test mode, toggles DSG FET state |

In normal operation, the FETs can be controlled autonomously by the device or manually using FET Control subcommands from the host. The ***Settings:FET:FET Options[FET_CTRL_EN]*** must be set for the device to enable the FETs at all. When this is set, the device will generally enable the FETs if there is nothing present which would block them, such as a protection fault or control from the host. Even if the host plans to control the FETs manually, the device may still change FET states based on the device settings, such as if body diode

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protection is enabled. If the intent is for the device to monitor and provide an interrupt or flag for a protection event, but the device is not to autonomously disable a FET in response to it, the appropriate configuration bit in ***Settings:Protection:CHG FET Protections A – C*** and ***Settings:Protection:DSG FET Protections A – C*** can be cleared. In this case, the host can monitor the interrupt or flags and decide whether to manually disable the FET.

For the CHG FET turnoff action to occur immediately when a fault is detected, the value of ***Settings:Protection:CHG FET Protections A*** should only be set to 0x18 or 0x98. Setting it to other values can cause FET turnoff action to be delayed by up to 250 ms in NORMAL mode or 1 second in SLEEP mode.

For the DSG FET turnoff action to occur immediately when a fault is detected, the value of ***Settings:Protection:DSG FET Protections A*** should only be set to 0x80 or 0xE4. Setting it to other values can cause FET turnoff action to be delayed by up to 250 ms in NORMAL mode or 1 second in SLEEP mode.

During normal operation, the host can disable the FETs by asserting the CFETOFF or DFETOFF pins or by sending FET Control subcommands (Table 24). When the FET Control subcommands are used to disable one or more FETs, a signal is latched blocking one or more FETs from being enabled. In order to allow one or more FETs to be re-enabled, it is first necessary to clear the latched signal by sending the appropriate FET Control subcommand to release the block (such as *0x0096 ALL_FETS_ON()*), and ensuring the CFETOFF or DFETOFF pins are deasserted.

The FETs can only be enabled if nothing exists to block them (such as the latched FET Control subcommand signal, or the CFETOFF or DFETOFF signal asserted, or a separate enabled safety fault present).

The FET control subcommands for use during normal operation are shown below.

**Table 24. FET Control Subcommands**

| Subcommand | Description |
|---|---|
| 0x0093 DSG_PDSG_OFF() | Causes the DSG and PDSG FETs to be disabled |
| 0x0094 CHG_PCHG_OFF() | Causes the CHG and PCHG FETs to be disabled |
| 0x0095 ALL_FETS_OFF() | Causes the DSG, PDSG, CHG, and PCHG FETs to be disabled |
| 0x0096 ALL_FETS_ON() | Allows all FETs to be enabled if nothing else is blocking them |
| 0x0097 FET_CONTROL() | An 8-bit field is sent with bits 3:0 matching those in *0x7F FET Status()*. When a bit is set using this subcommand, the corresponding FET is blocked from being enabled. |

For security purposes, the device can be set to either allow or ignore the host FET Control commands while in SEALED mode using ***Settings:FET:FET Options[HOST_FET_EN].***.

The present status of the FET drivers is provided in *0x0057 Manufacturing Status()* subcommand, which includes the status bits described below.

**Table 25. *0x0057 Manufacturing Status()* Bit Definitions**

| Bit | Name | Description |
|---|---|---|
| 7 | OTPW_EN | The OTP is not blocked from being written. |
| 6 | PF_EN | Permanent Fails are enabled |
| 5 | PDSG_TEST | PDSG FET is enabled in FET Test mode |
| 4 | FET_EN | FETs are enabled for device operation, otherwise the device is in FET Test mode |
| 3 | RSVD | Reserved |
| 2 | DSG_TEST | DSG FET is enabled in FET Test mode |
| 1 | CHG_TEST | CHG FET is enabled in FET Test mode |
| 0 | PCHG_TEST | PCHG FET is enabled in FET Test mode |

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#### 7.3.4.18.2.1 Precharge Mode

The BQ76942 device includes precharge functionality, which can be used to reduce the charging current for an under-voltage battery by charging using a high-side PCHG PFET (driven from the PCHG pin) with series resistor until the battery reaches a programmable voltage level. When the minimum cell voltage is less than ***Settings:FET:Precharge Start Voltage***, the PCHG FET will be used for charging. Setting this threshold to 0 will disable precharge mode. Precharge mode will be deactivated when the minimum cell voltage reaches or exceeds a level given by ***Settings:FET:Precharge Stop Voltage***. The status of the PCHG FET is provided in the *0x7F FET Status()[PCHG_FET]* register bit.

#### 7.3.4.18.2.2 Predischarge Mode

The BQ76942 device includes predischarge functionality, which can be used to reduce inrush current when the load is initially powered, by first enabling a high-side PDSG PFET (driven from the PDSG pin) with series resistor, which allows the load to slowly charge. If predischarge mode is enabled, whenever the DSG FET is to be turned on to power the load, the device will first enable the PDSG FET, then eventually transition to turning on the DSG FET and turning off the PDSG FET. The predischarge mode is enabled when ***Settings:FET:FET Options[PDSG_EN]*** is set.

When predischarge mode has been activated, the device will remain in this mode until either a timeout is reached, or the voltage at the LD pin rises to within a programmable delta of the top-of-stack voltage, or both. The timeout can be set from 10 ms to 2550 ms in steps of 10 ms using ***Settings:FET:Predischarge Timeout***. If the timeout is set to 0, then the device will not use a timeout and will exit when the voltage condition is met. The voltage delta is programmable from 10 mV to 2550 mV in steps of 10 mV using ***Settings:FET:Predischarge Stop Delta***. If the voltage delta is set to 0, the device will not use a voltage condition and will exit based on the timeout. Note: the voltage delta is only checked by the device every 250 ms. The status of the PDSG FET is provided in the *0x7F FET Status()[PDSG_FET]* register bit.

### 7.3.5 Voltage References

The BQ76942 device includes two voltage references, VREF1 and VREF2, with VREF1 used by the voltage ADC for most measurements except external thermistors. VREF2 is used by the integrated 1.8 V LDO, internal oscillators, and integrated coulomb counter ADC, and is also provided as an input to the voltage ADC for diagnostic purposes.

### 7.3.6 ADC Multiplexer

The ADC multiplexer connects various signals to the voltage ADC, including the individual differential cell voltage pins, the on-chip temperature sensor, the biased thermistor pins, the VREF2 reference voltage, the VSS pin voltage, and internal dividers connected to the VC10, PACK, and LD pins.

### 7.3.7 LDOs

The BQ76942 device contains an integrated 1.8 V LDO (REG18) that provides a regulated 1.8 V supply voltage for the device's internal circuitry and digital logic. This regulator uses an external capacitor connected to the REG18 pin, it should only be used for internal circuitry.

The device also integrates two separately programmable LDOs (REG1 and REG2) for external circuitry, such as a host processor or external transceiver circuitry, which can be programmed to independent output voltages. The REG1 and REG2 LDOs take their input from the REGIN pin, with this voltage either provided externally or generated by an on-chip pre-regulator (referred to as REG0). The REG1 and REG2 LDOs can provide an output current of up to ≈50 mA each.

#### 7.3.7.1 Pre-Regulator Control

The REG1 and REG2 LDOs take their input from the REGIN pin, which should be approximately 5.5 V. This REGIN pin voltage can be supplied externally (such as by a separate DC/DC converter) or using the integrated voltage pre-regulator (referring to as REG0), which drives the base of an external NPN BJT (using the BREG pin) to provide the 5.5 V REGIN pin voltage. When the pre-regulator is being used, special care should be taken to ensure the device retains sufficient voltage on its BAT pin, per the specifications in Specifications.

When the ***Settings:Configuration:REG0 Config[REG0_EN]*** configuration bit is set, the device will enable the pre-regulator.

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If neither REG1 nor REG2 will be used in the system, or if the REGIN voltage will be supplied externally, then the ***Settings:Configuration:REG0 Config[REG0_EN]*** configuration bit should be cleared.

The REG1 and REG2 LDOs can only be powered if ***Settings:Configuration:REG0 Config[REG0_EN]*** is set, otherwise the device will not enable the LDOs. This is true when REG1 or REG2 is powered through subcommand, but this is not checked at initial boot from OTP.

Note: there is a diode connection between the REGIN pin (anode) and the BAT pin (cathode), so the voltage on REGIN should not exceed the voltage on BAT.

#### *7.3.7.2 REG1 and REG2 LDO Controls*

The REG1 and REG2 LDOs in the BQ76942 device are for customer use, and their output voltages can be programmed independently to 1.8 V, 2.5 V, 3.0 V, 3.3 V, or 5.0 V. The voltage levels are selected using the ***Settings:Configuration:REG12 Config[REG1V_2:REG1V_0]*** and ***Settings:Configuration:REG12 Config[REG2V_2:REG2V_0]*** configuration bits as shown below. The LDOs are enabled using the ***Settings:Configuration:REG12 Config[REG1_EN]*** and ***Settings:Configuration:REG12 Config[REG2_EN]*** configuration bits, and their settings can be modified during operation using the *0x0098 REG12_CONTROL()* subcommand. This subcommand takes an 8-bit value that matches the bits in the ***Settings:Configuration:REG12 Config*** configuration register. It is important that the voltage selection not be changed in CONFIG_UPDATE mode while the LDO is enabled.

**Table 26. REG1 and REG2 LDO Voltage Settings**

| REG1V_2:0, REG2V_2:0 | REG1, REG2 Voltage (V) |
|---|---|
| 0x0 - 0x3 | 1.8 |
| 0x4 | 2.5 |
| 0x5 | 3.0 |
| 0x6 | 3.3 |
| 0x7 | 5.0 |

The REG1 and REG2 LDOs and the REG0 pre-regulator are disabled by default in the BQ76942 device, with the REG1 and REG2 pulled to VSS with an internal resistance of ≈2.5-kΩ. If the pull-up resistors for the serial communications are connected to the REG1 voltage output, the REG1 voltage can be overdriven from an external voltage supply on the manufacturing line, to allow communications with the device. The BQ76942 device can then be programmed to enable REG0 and REG1 with the desired configuration, and this setting can be programmed into OTP memory. Thus, at each later power-up, the device will autonomously load the OTP settings and enable the LDO as configured, without requiring communications first.

### 7.3.8 Standalone Versus Host Interface

The BQ76942 device can be configured to operate in a completely standalone mode, without any host processor in the system, or together with a host processor. If in standalone mode, the device can monitor conditions, control FETs and an in-line fuse based on threshold settings, and recover FETs when conditions allow, all without requiring any interaction with an external processor. If a host processor is present, the device can still be configured to operate fully autonomously, while the host processor can read measurements and exercise control as desired. In addition, the device can be configured for manual host control, such that the device can monitor and provide a flag when a protection alert or fault has occurred, but will rely on the host to disable FETs.

The host processor can interface with the BQ76942 device through a serial bus as well as selected pin controls. Serial bus communication through $I^2C$ (supporting speeds up to 400 kHz), SPI (supporting speeds up to 2 MHz) or HDQ is available, with the serial bus configured for $I^2C$ by default. The pin controls available include RST_SHUT, ALERT, CFETOFF, DFETOFF, DDSG, and DCHG, which are described in detail below.

### 7.3.9 Multifunction Pin Controls

The BQ76942 device provides flexibility regarding the multifunction pins on the device, which includes the TS1, TS2, TS3, CFETOFF, DFETOFF, ALERT, HDQ, DCHG, and DDSG pins. Several of the pins can be used as active-high outputs with configurable output level. The digital output driver for these pins can be configured to drive an output powered from the REG1 LDO or from the internal REG18 LDO, and thus when asserted active-high will drive out the voltage of the selected LDO.

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Note: the REG18 LDO is not capable of driving high current levels, so it is recommended to only use this LDO to provide a digital output if it will be driving a very high resistance (such as > 1 MΩ) or light capacitive load. Otherwise the REG1 should be powered and used to drive the output signal.

The options supported on each pin include:

**ALERT**

Alarm interrupt output. It can be configured as follows:

Hi-Z when no alarm is triggered, versus driven low when triggered.

Driven high when no alarm is triggered, versus driven low when triggered.

Driven low when no alarm is triggered, versus driven high when triggered.

HDQ communications

Can be used for HDQ communications with a host processor.

**CFETOFF**

Input to control the CHG FET (that is, CFETOFF functionality). It can be configured as follows:

A high input forces the CHG FET off, a low input allows the CHG FET to be turned on (by host or device itself).

A low input forces the CHG FET off, a high input allows the CHG FET to be turned on (by host or device itself).

**DFETOFF**

Input to control the DSG FET (that is, DFETOFF functionality). It can be configured as follows:

A high input forces the DSG FET off, a low input allows the DSG FET to be turned on (by host or device itself).

A low input forces the DSG FET off, a high input allows the DSG FET to be turned on (by host or device itself).

Input to control both the DSG and CHG FETs (that is, BOTHOFF functionality). It can be configured as follows:

A high input forces both FETs off, a low input allows the FETs to be turned on (by host or device itself).

A low input forces both FETs off, a high input allows the FETs to be turned on (by host or device itself).

**HDQ**

HDQ communications

Can be used for HDQ communications with a host processor.

SPI MOSI pin

MOSI pin for SPI communications.

**DCHG**

DCHG functionality

A logic-level output corresponding to a fault which would normally cause the CHG driver to be disabled.

**DDSG**

DDSG functionality

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A logic-level output corresponding to a fault which would normally cause the DSG driver to be disabled

**ALERT, CFETOFF, DFETOFF, HDQ, DCHG, and DDSG**

General purpose digital output

Can be driven high or low by command

Can be configured for an active-high output to be driven from the REG1 LDO or the REG18 LDO

Can be configured to have a weak pull-down to VSS or weak pull-up to REG1 enabled continuously

**ALERT, CFETOFF, DFETOFF, TS1, TS2, TS3, HDQ, DCHG, and DDSG**

Thermistor temperature measurement

A thermistor can be attached between the pin and VSS

ADCIN

Pin can be used for general purpose ADC measurement



These pin configurations are controlled by the ***Settings:Configuration:ALERT Pin Config, CFETOFF Pin Config, DFETOFF Pin Config, TS1 Config, TS2 Config, TS3 Config, HDQ Pin Config, DCHG Pin Config, and DDSG Pin Config*** configuration registers. The [PIN_FXN1:0] bits in each configuration register determine how the pin will be used:

**Table 27. Multifunction Pin Function Controls**

| PIN_FXN1 | PIN_FXN0 | Pin Function |
|---|---|---|
| 0 | 0 | Pin is used for communications, or not used at all |
| 0 | 1 | General purpose digital output (GPO) |
| 1 | 0 | Alternate function (ALT) |
| 1 | 1 | Thermistor measurement or general purpose ADC input (AD) |

The ALT (Alternate function) setting refers to special functions that are only available on particular pins. The alternate functions available for pins are:

| Pin | ALT (Alternate function) |
|---|---|
| ALERT | Alarm interrupt output |
| CFETOFF | CFETOFF functionality (CHG and PCHG FET control) |
| DFETOFF | DFETOFF functionality (DSG and PDSG FET control) |
| | BOTHOFF functionality (combined CHG and PCHG, and DSG and PDSG FET control) |
| DCHG | DCHG functionality (logic-level protection signal) |
| DDSG | DDSG functionality (logic-level protection signal) |

Each pin configuration register includes ***[OPT5:0]*** bits which set the operation of the pin. When a pin is configured for ALT or GPO, these bits are used as shown below.

**Table 28. Multifunction Pin Options for ALT or GPO Pins**

| Bit | Function |
|---|---|
| OPT5 | Polarity for ALERT, CFETOFF, DFETOFF. HDQ, DCHG, adn DDSG pins only.<br>0: selects active-high.<br>1: selects active-low. |

**Table 28. Multifunction Pin Options for ALT or GPO Pins (continued)**

| | |
|---|---|
| OPT4 | Only used for DFETOFF pin.<br>0: selects ALT = DFETOFF<br>1: selects ALT = BOTHOFF |
| OPT3 | GPO drive level for ALERT, CFETOFF, DFETOFF, HDQ, DCHG, and DDSG pins only.<br>0: output high drive uses REG18.<br>1: output high drive uses REG1. |
| OPT2 | GPO weak pull-up control for ALERT, CFETOFF, DFETOFF, HDQ, DCHG, and DDSG pins only.<br>0: weak pull-up to REG1 is disabled.<br>1: weak pull-up to REG1 is enabled.<br>Note: this should only be selected if OPT[3] = 0 and OPT[1] = 0 |
| OPT1 | GPO drive mode for ALERT, CFETOFF, DFETOFF, HDQ, DCHG, and DDSG pins only.<br>0: pin drives tri-state when controlled to be driven "high."<br>1: pin drives active-high when controlled to be driven "high." |
| OPT0 | GPO weak pulldown control for ALERT, CFETOFF, DFETOFF, HDQ, DCHG, and DDSG pins only.<br>0: weak pulldown to VSS is disabled.<br>1: weak pulldown to VSS is enabled. |

When a pin is selected for thermistor or ADCIN functionality, the ***[OPT5:0]*** bits are used as shown below.

**Table 29. Multifunction Pin Options for Thermistor or ADCIN Pins**

| Bit | Function |
|---|---|
| OPT5:OPT4 | Pull-up control<br>00: selects 18 kΩ pull-up for thermistor measurement<br>01: selects 180 kΩ pull-up for thermistor measurement<br>10: selects no pull-up (used for ADCIN) |
| OPT3:2 | Polynomial selection for thermistor temperature measurement<br>00: selects ***Calibration:18K Temperature Model***<br>01: selects ***Calibration:180K Temperature Model***<br>10: selects ***Calibration:Custom Temperature Model***<br>11: no polynomial is used, raw ADC counts are reported |
| OPT1:0 | Measurement type<br>00: general purpose ADC input<br>01: thermistor temperature measurement, used for cell temperature protections<br>10: thermistor temperature measurement, reported but not used for protections<br>11: thermistor temperature measurement, used for FET temperature protection |

When a pin is configured for use as a general purpose digital output, its output state can be controlled by the subcommands shown below.

**Table 30. General Purpose Digital Output Control Subcommands**

| Subcommand | Description |
|---|---|
| 0x2800 CFETOFF_LO() | If the CFETOFF pin is configured as a GPO, this subcommand sets it to drive a low output. |
| 0x2801 DFETOFF_LO() | If the DFETOFF pin is configured as a GPO, this subcommand sets it to drive a low output. |
| 0x2802 ALERT_LO() | If the ALERT pin is configured as a GPO, this subcommand sets it to drive a low output. |
| 0x2806 HDQ_LO() | If the HDQ pin is configured as a GPO, this subcommand sets it to drive a low output. |
| 0x2807 DCHG_LO() | If the DCHG pin is configured as a GPO, this subcommand sets it to drive a low output. |
| 0x2808 DDSG_LO() | If the DDSG pin is configured as a GPO, this subcommand sets it to drive a low output. |
| 0x2810 CFETOFF_HI() | If the CFETOFF pin is configured as a GPO, this subcommand sets it to drive a high output. |
| 0x2811 DFETOFF_HI() | If the DFETOFF pin is configured as a GPO, this subcommand sets it to drive a high output. |
| 0x2812 ALERT_HI() | If the ALERT pin is configured as a GPO, this subcommand sets it to drive a high output. |
| 0x2816 HDQ_HI() | If the HDQ pin is configured as a GPO, this subcommand sets it to drive a high output. |
| 0x2817 DCHG_HI() | If the DCHG pin is configured as a GPO, this subcommand sets it to drive a high output. |
| 0x2818 DDSG_HI() | If the DDSG pin is configured as a GPO, this subcommand sets it to drive a high output. |

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### 7.3.10 RST_SHUT Pin Operation

The RST_SHUT pin provides a simple way to reset or shutdown the BQ76942 device without needing to use serial bus communication. During normal operation, the RST_SHUT pin should be driven low. When the pin is driven high, the device will immediately reset most of the digital logic, including that associated with the serial communications bus. However, it does not reset the logic that holds the state of the protection FETs and FUSE, these remain as they were before the pin was driven high. If the pin continues to be driven high for 1 second, the device will then transition into SHUTDOWN mode, which involves disabling external protection FETs, and powering off the internal oscillators, the REG18 LDO, the on-chip pre-regulator, and the REG1 and REG2 LDOs.

### 7.3.11 CFETOFF, DFETOFF, BOTHOFF Pin Functionality

The BQ76942 device includes two pins (CFETOFF and DFETOFF) which can be used to disable the protection FET drivers quickly, without going through the host serial communications interface. When the selected pin is asserted, the device disables the respective protection FET. Note: when the selected pin is deasserted, the respective FET will only be enabled if there are no other items blocking them being re-enabled, such as if the host also sent a *0x0097 FET_CONTROL()* subcommand to disable the FETs using the serial communications interface after setting the selected pin. Both the CFETOFF and DFETOFF pins can be used for other functions if the FET turnoff feature is not required.

The CFETOFF pin can optionally be used to disable the CHG and PCHG FETs, and the DFETOFF pin can optionally be used to disable the DSG and PDSG FETs. The device also includes the option to configure the DFETOFF pin as BOTHOFF functionality, such that if that pin is asserted, the CHG, PCHG, DSG, and PDSG FETs will be disabled. This allows the CFETOFF pin to be used for an additional thermistor in the system, while still providing pin control to disable the FETs.

The CFETOFF or BOTHOFF functionality disables both the CHG FET and the PCHG FET when asserted.

The DFETOFF or BOTHOFF functionality disables both the DSG FET and the PDSG FET when asserted.

### 7.3.12 ALERT Pin Operation

The ALERT pin is a multifunction pin that can be configured either as ALERT (to provide an interrupt to a host processor), a thermistor input, a general purpose ADC input, a general purpose digital output, or an HDQ serial communication interface. The pin can be configured as active-high, active-low, or open-drain, to accommodate different system design preference. When configured as the HDQ interface pin, the pin will operate in open-drain mode.

When the pin is configured to drive an active high output, the output voltage is driven from either the REG18 1.8 V LDO or the REG1 LDO (which can be programmed from 1.8 V to 5.0 V). Note: if a DC or significant transient current may be driven by this pin, then the output should be configured to drive using the REG1 LDO, not the REG18 LDO.

The BQ76942 device includes functionality to generate an alarm signal at the ALERT pin, which can be used as an interrupt to a host processor. This functionality is optional, it can be enabled by setting the ***Settings:Configuration:ALERT Pin Config[PIN_FXN1:0]*** = 0b10. When used for the alarm function, the pin can be programmed to drive the signal as an active-lo or hi-Z signal, an active-high or low signal, or an active-low or high signal (that is, inverted polarity). The alarm function within the BQ76942 device includes a programmable mask, to allow the customer to decide which of many flags or events can trigger an alarm. The *0x64 Alarm Raw Status()* command provides the present (unlatched) value of the bits described below:

**Table 31. *Alarm Raw Status()* Bit Definitions**

| Bit | Name | Description |
|---|---|---|
| 15 | SSBC | Safety Status - set if a bit in *Safety Status B-–C()* is set. |
| 14 | SSA | Hardware Safety Status - set if a bit in *Safety Status A()* is set. |
| 13 | PF | Permanent Fail Status - set if a bit in *PF Status A–D()* is set. |
| 12 | MSK_SFALERT | Masked Safety Alerts - set if a bit in *Safety Alert A–C()* is set and the corresponding bit in ***Settings:Alarm:SF Alert Mask A–C*** is set. |
| 11 | MSK_PFALERT | Masked Permanent Fail Alerts - set if a bit in *PF Alert A–D()* is set and the corresponding bit in ***Settings:Alarm:PF Alert Mask A–D*** is set. |
| 10 | INITSTART | Initialization started (sets quickly after device powers up) |
| 9 | INITCOMP | Initiatlization completed (sets after device has powered and completed one measurement scan) |

**Table 31. *Alarm Raw Status()* Bit Definitions (continued)**

| Bit | Name | Description |
|---|---|---|
| 8 | RSVD | Reserved |
| 7 | FULLSCAN | Full Voltage Scan Complete. The necessary multiple ADC scans have been completed to collect the full voltage measurement loop data (including cell voltages, pin or thermistor voltages, etc). This bit sets after the first full scan completes, then remains set. |
| 6 | XCHG | CHG FET is off |
| 5 | XDSG | DSG FET is off |
| 4 | SHUTV | Stack voltage is below ***Power:Shutdown:Shutdown Stack Voltage*** |
| 3 | FUSE | FUSE Pin Driven. FUSE pin is being driven by either the BQ76942 device or the secondary protector. |
| 2 | CB | Cell Balancing Enabled. |
| 1 | ADSCAN | Voltage ADC Scan Complete. A single ADC scan is complete (cell voltages are measured on each scan). This bit sets after the first ADC scan completes, then remains set. |
| 0 | WAKE | Wake. Device is wakened from SLEEP mode. |

The bits in *0x64 Alarm Raw Status()* can be selected to be latched and included in the alarm interrupt output based on mask registers. Note that the bits in *0x64 Alarm Raw Status()* are not latched, so they may set only briefly. Whenever a masked flag transitions from low to high, it latches a corresponding bit in *0x62 Alarm Status()*. The [ADSCAN] and [FULLSCAN] bits are exceptions, they will be latched in *0x62 Alarm Status()* when scans complete if masked, even though the corresponding bits in *0x64 Alarm Raw Status()* do not toggle.

The masking is determined if the corresponding mask bit is set in the ***Settings:Alarm:Default Alarm Mask***, ***Settings:Alarm:SF Alert Mask A–C***, and ***Settings:Alarm:PF Alert Mask A–D*** configuration registers. The host can poll *0x62 Alarm Status()*, or use the alarm interrupt signal (the OR of all bits in *0x62 Alarm Status()*) mapped to the ALERT pin.

Whenever bits are latched into *0x62 Alarm Status()*, the host can read the status and clear those latched bits by writing the *0x62 Alarm Status()* command with a '1' in one or more of the bits to be cleared, and '0s' in all other bits (which leaves the other bits unchanged). This prevents unintentional clearing of any additional *0x62 Alarm Status()* bits that may have been set just before the clearing signal was sent from the host processor.

The *0x66 Alarm Enable()* command can be read to see the present mask applied to the *0x64 Alarm Raw Status()* bits. The *0x66 Alarm Enable()* command can also be written by the host to change the masking during operation.

The status of the ALERT pin is provided in the *0x7F FET Status()[ALRT_PIN]* register bit.

### 7.3.13 DDSG and DCHG Pin Operation

The BQ76942 device includes two multifunction pins, DDSG and DCHG, which can be configured as logic-level outputs to provide a fault-related signal to a host processor or external circuitry (that is, DDSG and DCHG functionality), as a thermistor input, a general purpose ADC input, or a general purpose digital output.

When used as a digital output, the pins can be configured to drive an active high output, with the output voltage driven from either the REG18 1.8 V LDO or the REG1 LDO (which can be programmed from 1.8 V to 5.0 V). Note: if a DC or significant transient current may be driven by a pin, then the output should be configured to drive using the REG1 LDO, not the REG18 LDO.

When the pins are configured for DDSG and DCHG functionality, they provide signals related to protection faults that (on the DCHG pin) would normally cause the CHG driver to be disabled, or (on the DDSG pin) would normally cause the DSG driver to be disabled. These signals can be used to control external protection circuitry, if the integrated high-side NFET drivers will not be used in the system. They can also be used as interrupts in manual FET control mode for the host processor to decide whether to disable the FETs through commands or using the CFETOFF and DFETOFF pins.

For example, if the DDSG pin is configured for DDSG functionality, and the Cell Overvoltage (COV) protection is enabled, the DDSG pin will be deasserted while there is no fault present. When a COV fault occurs, the DDSG pin will be asserted. When the device recovers from the COV fault, the DDSG pin will be deasserted. The polarity of the drive signal on the pin is also programmable.

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### 7.3.14 Operational Modes

This device supports four operational modes, to support optimized features and power dissipation, with the device able to transition between modes either autonomously or controlled by a host processor.

- NORMAL mode: In this mode, the device performs frequent measurements of system current, cell voltages, internal and thermistor temperature, and various other voltages, operates protections as configured, and provides data and status updates.
- SLEEP mode: In this mode, the DSG FET is enabled, the CHG FET can optionally be disabled, and the device performs measurements, calculations, and data updates in adjustable time intervals. Battery protections are still enabled. Between the measurement intervals, the device is operating in a reduced power stage to minimize total average current consumption.
- DEEPSLEEP mode: In this mode, the CHG, PCHG, DSG, and PDSG FETs are disabled, all battery protections are disabled, and no current or voltage measurements are taken. The REG1 and REG2 LDOs can be kept powered, in order to maintain power to external circuitry, such as a host processor.
- SHUTDOWN mode: The device is completely disabled (including the internal, REG1, and REG2 LDOs), the CHG, PCHG, DSG, and PDSG FETs are all disabled, all battery protections are disabled, and no measurements are taken. This is the lowest power state of the device, which may be used for shipment or long-term storage. All register settings are lost when in SHUTDOWN mode.

The device also includes a CONFIG_UPDATE mode, which is used for parameter updates. Transitioning between operational modes is shown below.

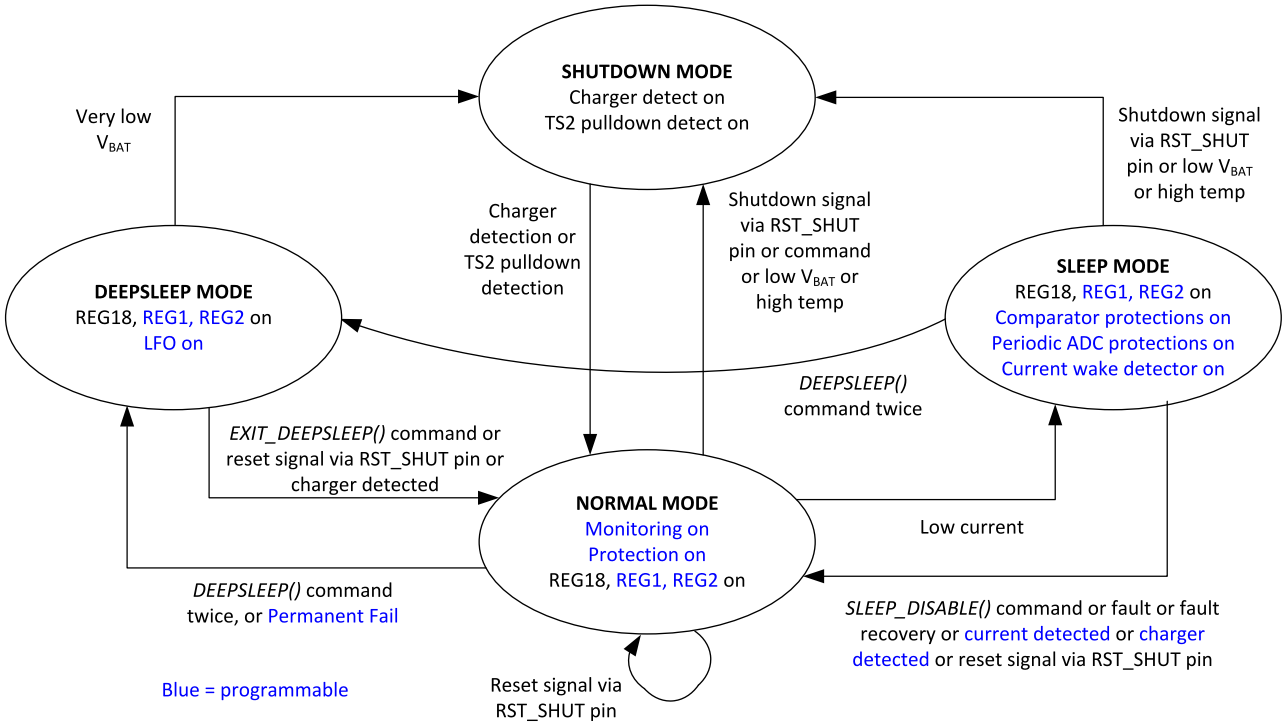


**Figure 8. Operational Modes**

#### *7.3.14.1 NORMAL Mode*

NORMAL mode is the highest performance mode of the device, in which the device is making regular measurement of voltage, current, and temperature, the LFO (low frequency oscillator) is operating, and the internal processor powers up (as needed) for data processing and control. Full battery protections are operating, based on device configuration settings. System current is measured at intervals of 3 ms, with cell voltages measured at intervals of 45 ms or slower, depending on configuration. If the ***FASTADC*** configuration bit is set, the conversion speed for both voltages and currents is doubled, with a reduction in measurement resolution.

The device will generally be in NORMAL mode whenever any active charging or discharging is underway. When the CC1 Current measurement falls below a SLEEP current threshold given by ***Power:Sleep:Sleep Current***, the system is considered in relax mode, and the BQ76942 device can autonomously transition into SLEEP mode, depending on configuration.

#### *7.3.14.2 SLEEP Mode*

SLEEP mode is a reduced functionality state that can be optionally used to reduce power dissipation when there is little or no system load current or charging in progress, but still provides voltage at the battery pack terminals to keep the system alive. At initial power up, the ***Settings:Configuration:Power Config[SLEEP]*** configuration bit determines whether the device can enter SLEEP mode. After initialization, SLEEP mode can be allowed or disallowed using the *0x0099 SLEEP_ENABLE()* and *0x009A SLEEP_DISABLE()* subcommands. The *0x12 Battery Status()[SLEEP_EN]* bit indicates whether the device is presently allowed to enter SLEEP mode or not, while the *0x12 Battery Status()[SLEEP]* bit indicates whether it is presently in SLEEP mode or not.

When the magnitude of the CC1 Current measurement falls below a current threshold given by ***Power:Sleep:Sleep Current***, the system is considered in relax mode, and the BQ76942 device will autonomously transition into SLEEP mode, if settings permit. During SLEEP mode, comparator-based protections operate the same as during NORMAL mode. ADC-based current, voltage, and temperature measurements are taken every ***Power:Sleep:Voltage Time*** seconds. While in SLEEP mode, the device begins a 4-sec current measurement 1-sec after completing voltage and temperature measurements, therefore it is recommended to set this parameter to 5-sec or (4 × n + 1) seconds. All temperature protections use the ADC measurements taken at the ***Power:Sleep:Voltage Time*** intervals, so they will update at a reduced rate during SLEEP mode.

The BQ76942 device will exit SLEEP mode if a protection fault occurs, or current begins flowing, or a charger is attached, or the *0x009A SLEEP_DISABLE()* subcommand is sent, or if the RST_SHUT pin is asserted for < 1-sec. When exiting based on current flow, the device will quickly enable the FETs (if the CHG FET was off, or the DSG FET was in source follower mode), but the standard measurement loop is not restarted until the next 1-sec boundary occurs within the device timing. Therefore, new data may not be available for up to ≈1-sec after the device exits SLEEP mode.

The coulomb counter ADC operates in a reduced power and speed mode to monitor current during SLEEP mode. The current is measured every 12 ms and, if it exceeds ***Power:Sleep:Wake Comparator Current*** in magnitude, the device quickly transitions back to NORMAL mode. In addition to this check, if the 4-sec current measurement taken at each ***Power:Sleep:Voltage Time*** interval exceeds ***Power:Sleep:Sleep Current***, the device will exit SLEEP mode.

The device monitors the PACK pin voltage and the top-of-stack voltage at each ***Power:Sleep:Voltage Time*** measurement interval. If the PACK pin voltage is higher than the top-of-stack voltage by more than ***Power:Sleep:Sleep Charger PACK-TOS Delta*** and the top-of-stack voltage is less than ***Power:Sleep:Sleep Charger Voltage Threshold***, the device will exit SLEEP mode. The BQ76942 device also includes a hysteresis on the SLEEP mode entrance, in order to avoid the device quickly entering and exiting SLEEP mode based on a dynamic load. After transitioning to NORMAL mode, the device will not enter SLEEP mode again for a number of seconds given by the ***Power:Sleep:Sleep Hysteresis Time*** setting.

During SLEEP mode, the DSG FET can be driven either using the charge pump or in source-follower mode, as described in High-Side NFET Drivers. The CHG FET can be disabled or driven using the charge pump, based on the setting of ***Settings:FET:FET Options[SLEEPCHG]***.

#### *7.3.14.3 DEEPSLEEP Mode*

The BQ76942 device integrates a DEEPSLEEP mode, which is a low power mode that allows the REG1 and REG2 LDOs to remain powered, but disables other subsystems. In this mode, the protection FETs are all disabled, so no voltage is provided at the battery pack terminals. All protections are disabled, and all voltage, current, and temperature measurements are disabled.

DEEPSLEEP mode can be entered by sending the *0x000F DEEPSLEEP()* subcommand twice in a row within a 4-sec time window. The device will exit DEEPSLEEP mode and return to NORMAL mode if the *0x000E EXIT_DEEPSLEEP()* subcommand is sent, or if the RST_SHUT pin is asserted for < 1-sec, or if a charger is attached (which is detected by the voltage on the LD pin rising from below $V_{WAKEONLD}$ to exceed it). In addition, if the BAT pin voltage falls below $V_{PORA}$ - $V_{PORA\_HYS}$, the device transitions to SHUTDOWN mode.

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When the device is exiting DEEPSLEEP mode, it first completes a full measurement loop and evaluates conditions relative to enabled protections, to ensure that conditions are acceptable to proceed to NORMAL mode. This may take ≈250 ms plus the time for the measurement loop to complete.

The REG1 and REG2 LDOs will maintain their power state when entering DEEPSLEEP mode if the ***Settings:Configuration:Power Config[DPSLP_LDO]*** configuration bit is set. The device also provides the ability to keep the LFO running while in DEEPSLEEP mode, which allows for a faster responsiveness to communications and transition back to NORMAL mode, but will consume additional power. This is controlled by the ***Settings:Configuration:Power Config[DPSLP_LFO]*** configuration bit.

Other than the *0x000E EXIT_DEEPSLEEP()* subcommand, communications with the device over the serial interface will not cause it to exit DEEPSLEEP mode. However, since no measurements are taken while in DEEPSLEEP mode, there is no new information available for readout. To collect measurement data without powering the system the user can do the following:

1. Send the *0x0095 ALL_FETS_OFF()* subcommand to keep the FETs disabled.
2. Send the *0x000E EXIT_DEEPSLEEP()* subcommand to transition back into NORMAL mode.
3. Wait for a measurement cycle to complete by monitoring the *0x62 Alarm Status()[FULLSCAN]* bit.
4. Read the data.
5. Send the *0x000F DEEPSLEEP()* subcommand to return to DEEPSLEEP mode.
6. Send the *0x0096 ALL_FETS_ON()* subcommand to unblock the FETs from being enabled when DEEPSLEEP mode is exited in the future.

#### *7.3.14.4 SHUTDOWN Mode*

SHUTDOWN mode is the lowest power mode of the BQ76942 device, which can be used for shipping or long-term storage. In this mode, the device loses all register state information, the internal logic is powered down, the protection FETs are all disabled, so no voltage is provided at the battery pack terminals. All protections are disabled, all voltage, current, and temperature measurements are disabled, and no communications are supported. When the device exits SHUTDOWN, it will boot and read parameters stored in OTP (if that has been written). If the OTP has not been written, the device will power up with default settings, and then settings can be changed by the host writing device registers.

Entering SHUTDOWN mode involves a sequence of steps. The sequence can be initiated manually by sending the *0x0010 SHUTDOWN()* subcommand twice in a row within a 4-sec time window if the device is SEALED. If this subcommand is sent twice in a row while the device is UNSEALED, the delays associated with the sequence are skipped. The device can also be configured to enter SHUTDOWN mode automatically based on the top of stack voltage or the minimum cell voltage. If the top-of-stack voltage falls below ***Power:Shutdown:Shutdown Stack Voltage*** or if the minimum cell voltage falls below ***Power:Shutdown:Shutdown Cell Voltage***, the SHUTDOWN mode sequence is automatically initiated. The shutdown based on cell voltage does not apply to cell input pins being used to measure interconnect, based on settings in ***Settings:Configuration:Vcell mode***. Note: if this feature is enabled and cell open wire detection is also enabled, an open wire condition may result in the device entering SHUTDOWN mode before an open wire fault can be recorded. If an automatic shutdown has been started based on the cell or stack voltage, and the voltage measured on the PACK pin is equal or above a threshold given by ***Power:Shutdown:Charger Present Threshold***, the device will delay shutdown until the PACK pin voltage falls below this threshold.

While the BQ76942 device is in NORMAL mode or SLEEP mode, the device can also be configured to enter SHUTDOWN mode if the internal temperature measurement exceeds ***Power:Shutdown:Shutdown Temperature*** for ***Power:Shutdown:Shutdown Temperature Delay*** seconds.

When the SHUTDOWN mode sequence has been initiated by the *0x0010 SHUTDOWN()* subcommand or the RST_SHUT pin driven high for 1-sec, the device will wait for ***Power:Shutdown:FET Off Delay*** then disable the protection FETs. After a delay of ***Power:Shutdown:Shutdown Command Delay*** from when the sequence begins, the device will enter SHUTDOWN mode (so ***Power:Shutdown:Shutdown Command Delay*** should be set longer than ***Power:Shutdown:FET Off Delay***). However, if the voltage on the LD pin is still above the $V_{WAKEONLD}$ level, shutdown will be delayed until the voltage on LD falls below that level. Note: when SHUTDOWN mode is initiated in this manner, the device will first transition to NORMAL mode and will block entrance to SLEEP mode. If the FETs were initially off (such as if the device was in DEEPSLEEP mode) and

***Power:Shutdown:FET Off Delay*** = 0, the FETs will remain off. However, if ***Power:Shutdown:FET Off Delay*** > 0, the FETs may be enabled (if not blocked) upon entering NORMAL mode, then disabled after the ***Power:Shutdown:FET Off Delay***. If this is not preferred, the host can send the *0x0095 ALL_FETS_OFF()* before entering DEEPSLEEP mode, then can send the *0x0096 ALL_FETS_ON()* when exiting DEEPSLEEP mode.

While the device is in SHUTDOWN mode, a ≈5 V voltage is provided at the TS2 pin with high source impedance. If the TS2 pin is pulled low, such as by a switch to VSS, or if a voltage is applied at the LD pin above $V_{WAKEONLD}$ (such as when a charger is attached in series FET configuration), the device will exit SHUTDOWN mode. Note: if a thermistor is attached from the TS2 pin to VSS, this will prevent the device from ever fully entering SHUTDOWN mode.

As a countermeasure to avoid an unintentional wake from SHUTDOWN mode when putting the BQ76942 device into long-term storage, the device can be configured to automatically re-enter SHUTDOWN mode after ***Power:Shutdown:Auto Shutdown Time*** minutes. See Power:Shutdown:Auto Shutdown Time for more details.

The BQ76942 device performs periodic memory integrity checks and will force a watchdog reset if any corruption is detected. To avoid a cycle of resets in the case of a memory fault, the device will enter SHUTDOWN mode rather than resetting if a memory error is detected within ***Power:Shutdown:RAM Fail Shutdown Time*** seconds after a watchdog reset has occurred.

When the device is wakened from SHUTDOWN, it requires approximately 200-300 ms (if ***Settings:Permanent Failure:Enabled PF A[CUDEP]*** is not enabled) for the internal circuitry to power up, load settings from OTP memory, perform initial measurements, evaluate those relative to enabled protections, then to enable FETs if conditions allow. This can be much longer if ***[CUDEP]*** is enabled, depending on its associated delay setting in ***Permanent Fail:CUDEP:Delay***.

The BQ76942 device integrates a hardware overtemperature detection circuit, which determines when the die temperature passes an excessive temperature of approximately 120°C. If this detector triggers, the device will automatically begin the sequence to enter SHUTDOWN if the ***Settings:Configuration:Power Config[OTSD]*** configuration bit is set.

#### *7.3.14.5 CONFIG_UPDATE Mode*

The BQ76942 device uses a special CONFIG_UPDATE mode to make changes to the data memory settings. If changes were made to the data memory settings while the firmware was in normal operation, it could result in unexpected operation or consequences if settings used by the firmware changed in the midst of operation. When changes to the data memory settings are needed (which generally should only be done on the customer manufacturing line or in an offline condition), the host should:

Place the device into CONFIG_UPDATE mode by sending the *0x0090 ENTER_CFG_UPDATE()* subcommand. The device will then automatically disable the protection FETs if they are enabled.

Wait for the *0x12 Battery Status()[CFGUPDATE]* flag to set.

Modify settings as needed by writing updated data memory settings (for more information, see Data Memory Settings).

Send the *0x0092 EXIT_CFG_UPDATE()* command to resume firmware operation.

When in CONFIG_UPDATE mode, the device stops normal firmware operation and stops all measurements and protection monitoring. The host can then make changes to data memory settings (either writing registers directly into RAM, or instructing the device to program the RAM data into OTP). After changes are complete, the host then sends the *0x0092 EXIT_CFG_UPDATE()* command, at which point the device restarts normal firmware operation using the new data memory settings.

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### 7.3.15 Permanent Fail

The BQ76942 device integrates a suite of checks on battery operation and status that can trigger a Permanent Fail (PF) if conditions are considered so serious that the pack should be permanently disabled. The various PF checks can be enabled individually based on configuration settings, along with associated thresholds and delays for most checks. When a Permanent Fail has occurred, the BQ76942 device can be configured to either simply provide a flag (see *PF Status A–D()* subcommands), or to indefinitely disable the protection FETs (if the ***Settings:Protection:Protection Configuration[PF_FETS]*** bit is set), or to assert the FUSE pin (if the ***Settings:Protection:Protection Configuration[PF_FUSE]*** bit is set) to permanently disable the pack. The FUSE pin can be used to blow an in-line fuse and also can monitor if a separate secondary protector IC has attempted to blow the fuse.

Since the device stores Permanent Fail status in RAM, that status would be lost when the device resets. To mitigate this, the device can write Permanent Fail status to OTP when the ***Settings:Protection:Protection Configuration[PF_OTP]*** bit is set. OTP programming may be delayed in low-voltage and high-temperature conditions until OTP programming can reliably be accomplished. Note: writes to OTP during operation are only allowed if ***Settings:Manufacturing:Mfg Status Init[OTPW_EN]*** is set. If ***Settings:Protection:Protection Configuration[PF_OTP]*** is set but ***Settings:Manufacturing:Mfg Status Init[OTPW_EN]*** is clear, Permanent Fail status is saved to RAM (and will be preserved during a partial reset) but will not be programmed to OTP. If ***Settings:Protection:Protection Configuration[PF_OTP]*** is not set, Permanent Fail status will be lost on any reset, including a partial reset through the RST_SHUT pin.

Normally, a Permanent Fail causes the FETs to remain off indefinitely and the fuse may be blown. In that situation, no further action would be taken on further monitoring operations, and charging would no longer be possible. To avoid rapidly draining the battery, the device may be configured to enter DEEPSLEEP mode when a Permanent Fail occurs by setting the ***Settings:Protection:Protection Configuration[PF_DPSLP]*** configuration bit. Entrance to DEEPSLEEP mode will still be delayed until after fuse blow and OTP programming are completed, if those options are enabled.

When a Permanent Fail occurs, the device may be configured to either turn the REG1 and REG2 LDOs off (if ***Settings:Protection:Protection Configuration[PF_REGS]*** is set) or to leave them in their present state (if ***Settings:Protection:Protection Configuration[PF_REGS]*** is cleared). Once disabled, they may still be reenabled through command.

The Permanent Fail checks incorporate a programmable delay, to avoid triggering a PF fault on an intermittent condition or measurement. When the threshold is first detected as being met or exceeded by an enabled PF check, the device will set a PF Alert signal, which can be monitored using the *PF Alert A–D()* commands and can also trigger an interrupt on the ALERT pin using the *Alarm Status()[MSK_PFALERT]* register bit and its associated mask settings.

Note: the device only evaluates the conditions for Permanent Fail at one second intervals while in NORMAL and SLEEP modes, it does not continuously compare measurements to the Permanent Fail fault thresholds between intervals. Thus, it is possible for a condition to trigger a PF Alert if detected over threshold, but even if the condition drops back below threshold briefly between the one second interval checks, the PF Alert would not be cleared until it was detected below threshold at a periodic check.

#### *7.3.15.1 Copper Deposition (CUDEP) Permanent Fail*

When a cell is severely overdischarged, copper deposition can occur, resulting in very high impedance. If this occurs while the pack is in operation, the BQ76942 device will typically detect this and disable the pack before cells reach this low voltage (based on a SUV PF). However, if the device is in SHUTDOWN mode for an excessively long time period and the cells become overly discharged, the pack could still wake and enable the FETs if a charger were attached. If the FETs were turned on in this condition, the pack voltage would rise sharply due to charging current, making the cells appear healthy. The CUDEP Permanent Fail is used to identify this condition and disable the pack. When enabled, this check keeps the FETs disabled at power up from SHUTDOWN mode until each cell voltage is greater than or equal to ***Permanent Fail:CUDEP:Threshold*** for ***Permanent Fail:CUDEP:Delay*** seconds. If any cell voltage is below ***Permanent Fail:CUDEP:Threshold*** for ***Permanent Fail:CUDEP:Delay*** seconds, the CUDEP Permanent Fail is triggered. This PF check is enabled by setting the ***Settings:Permanent Failure:Enabled PF A[CUDEP]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits.

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#### 7.3.15.2 Safety Undervoltage (SUV) Permanent Fail

The BQ76942 device integrates a Safety Undervoltage (SUV) Permanent Fail, which can permanently disable the pack if any cell voltage reaches or falls below a programmable threshold for a programmable delay time. The threshold is set by ***Permanent Fail:SUV:Threshold***, and the delay is set by ***Permanent Fail:SUV:Delay***. This PF check is enabled by setting the ***Settings:Permanent Failure:Enabled PF A[SUV]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits.

#### 7.3.15.3 Safety Overvoltage (SOV) Permanent Fail

The BQ76942 device integrates a Safety Overvoltage (SOV) Permanent Fail, which can permanently disable the pack if any cell voltage reaches or exceeds a programmable threshold for a programmable delay time. The threshold is set by ***Permanent Fail:SOV:Threshold***, and the delay is set by ***Permanent Fail:SOV:Delay***. This PF check is enabled by setting the ***Settings:Permanent Failure:Enabled PF A[SOV]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits.

#### 7.3.15.4 Safety Overcurrent in Charge (SOCC) Permanent Fail

The BQ76942 device integrates a Safety Overcurrent in Charge (SOCC) Permanent Fail, which can permanently disable the pack if the charging current reaches or exceeds a programmable threshold for a programmable delay time. The threshold is set by ***Permanent Fail:SOCC:Threshold***, and the delay is set by ***Permanent Fail:SOCC:Delay***. This PF check is enabled by setting the ***Settings:Permanent Failure:Enabled PF A[SOCC]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits.

#### 7.3.15.5 Safety Overcurrent in Discharge (SOCD) Permanent Fail

The BQ76942 device integrates a Safety Overcurrent in Discharge (SOCD) Permanent Fail, which can permanently disable the pack if the discharging current reaches or exceeds a programmable threshold for a programmable delay time. The threshold is set by ***Permanent Fail:SOCD:Threshold***, and the delay is set by ***Permanent Fail:SOCD:Delay***. This PF check is enabled by setting the ***Settings:Permanent Failure:Enabled PF A[SOCD]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits.

#### 7.3.15.6 Safety Cell Overtemperature (SOT) Permanent Fail

The BQ76942 device integrates a Safety Cell Overtemperature (SOT) Permanent Fail, which can permanently disable the pack if the maximum cell temperature reaches or exceeds a programmable threshold for a programmable delay time. The threshold is set by ***Permanent Fail:SOT:Threshold***, and the delay is set by ***Permanent Fail:SOT:Delay***. This PF check is enabled by setting the ***Settings:Permanent Failure:Enabled PF A[SOT]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits.

#### 7.3.15.7 Safety FET Overtemperature (SOTF) Permanent Fail

The BQ76942 device integrates a Safety FET Overtemperature (SOT) Permanent Fail, which can permanently disable the pack if the maximum FET temperature reaches or exceeds a programmable threshold for a programmable delay time. The threshold is set by ***Permanent Fail:SOTF:Threshold***, and the delay is set by ***Permanent Fail:SOTF:Delay***. This PF check is enabled by setting the ***Settings:Permanent Failure:Enabled PF A[SOTF]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits.

#### 7.3.15.8 Charge FET (CFETF) Permanent Fail

The BQ76942 device integrates a Charge FET (CFETF) Permanent Fail, which can permanently disable the pack if a charging current is measured that reaches or exceeds a programmable threshold for a programmable delay time while the charge FET is disabled. The threshold is set by ***Permanent Fail:CFETF:OFF Threshold***, and the delay is set by ***Permanent Fail:CFETF:OFF Delay***. This PF check is enabled by setting the ***Settings:Permanent Failure:Enabled PF B[CFETF]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits.

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#### 7.3.15.9 Discharge FET (DFETF) Permanent Fail

The BQ76942 device integrates a Discharge FET (DFETF) Permanent Fail, which can permanently disable the pack if a discharge current is measured that reaches or exceeds a programmable threshold for a programmable delay time while the discharge FET is disabled. The threshold is set by ***Permanent Fail:DFETF:OFF Threshold***, and the delay is set by ***Permanent Fail:DFETF:OFF Delay***. This PF check is enabled by setting the ***Settings:Permanent Failure:Enabled PF B[DFETF]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits. The value of ***Permanent Fail:DFETF:OFF Threshold*** should typically be a negative number.

#### 7.3.15.10 Secondary Protector (2LVL) Permanent Fail

The BQ76942 device integrates a Secondary Protector (2LVL) Permanent Fail, which can permanently disable the pack if an external secondary protector has detected a fault and is attempting to blow the fuse. The BQ76942 device monitors the level of the FUSE pin each second (in NORMAL and SLEEP modes), and if it detects the pin is being asserted by the secondary protector for ***Permanent Fail:2LVL:Delay*** seconds, a 2LVL PF fault is generated. This PF check is enabled by setting the ***Settings:Permanent Failure:Enabled PF B[2LVL]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits.

#### 7.3.15.11 Voltage Imbalance in Relax (VIMR) Permanent Fail

The BQ76942 device integrates a Voltage Imbalance in Relax (VIMR) Permanent Fail, which can permanently disable the pack if an excessive level of cell imbalance is detected while the pack is in a relax state, which is determined by the absolute value of measured current being less than ***Permanent Fail:VIMR:Max Relax Current***. The VIMR PF is only checked if the maximum cell voltage is above ***Permanent Fail:VIMR:Check Voltage*** and the absolute value of measured current is less than ***Permanent Fail:VIMR:Max Relax Current*** for a time duration of at least ***Permanent Fail:VIMR:Relax Min Duration***. This check will generate a PF fault when a cell imbalance (that is, the difference in the maximum and minimum cell voltages) is detected that meets or exceeds ***Permanent Fail:VIMR:Threshold*** for a time duration of ***Permanent Fail:VIMR:Delay***. This PF check is enabled by setting the ***Settings:Permanent Failure:Enabled PF B[VIMR]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits.

#### 7.3.15.12 Voltage Imbalance in Active (VIMA) Permanent Fail

The BQ76942 device integrates a Voltage Imbalance in Active (VIMA) Permanent Fail, which can permanently disable the pack if an excessive level of cell imbalance is detected while the pack is in a charging state, which is determined by the measured current meeting or exceeding ***Permanent Fail:VIMA:Min Active Current***. The VIMA PF is only checked if the maximum cell voltage is above ***Permanent Fail:VIMA:Check Voltage*** and the measured current is not less than ***Permanent Fail:VIMA:Min Active Current***. This check will generate a PF fault when a cell imbalance (that is, the difference in the maximum and minimum cell voltages) is detected that meets or exceeds ***Permanent Fail:VIMA:Threshold*** for a time duration of ***Permanent Fail:VIMA:Delay***. This PF check is enabled by setting the ***Settings:Permanent Failure:Enabled PF B[VIMA]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits.

#### 7.3.15.13 Short Circuit in Discharge Latched Permanent Fail

The BQ76942 device integrates a Latched Short Circuit in Discharge (SCDL) Permanent Fail, which can permanently disable the pack if an SCDL protection fault occurs (which indicates multiple Short Circuit in Discharge (SCD) protection faults have detected within a programmable time window). The settings that control the SCDL fault are explained in Short Circuit in Discharge Protection. The SCDL Permanent Fail should only be enabled if the SCDL protection fault is configured to not allow recovery. This PF check is enabled by setting the ***Settings:Permanent Failure:Enabled PF B[SCDL]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits.

#### 7.3.15.14 OTP Memory Signature Permanent Fail

The BQ76942 device integrates a signature check on the OTP memory that will be checked when the device boots and loads data from OTP, but only if the OTP memory is not entirely empty (which is the default configuration). If the OTP memory signature check fails, the device will not load any settings from OTP, it will instead boot and load the default configuration, which keeps the FETs turned off (but it will not blow the fuse) and the REG1 LDO disabled.

The OTP PF (OTPF) is enabled by default. It can be disabled by clearing the ***Settings:Permanent Failure:Enabled PF C[OTPF]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits.

Note: the device also includes a check on the trim information stored within the device during factory test. If an error is detected in this information during boot, the device will directly begin the SHUTDOWN sequence.

#### 7.3.15.15 Data ROM Memory Signature Permanent Fail

The BQ76942 device integrates a signature check on the Data ROM, which contains default values for the Data Memory settings. This PF will be checked when the device loads data from the Data ROM, which occurs at initial powerup or device reset. The Data ROM PF (DRMF) can be enabled by setting the ***Settings:Permanent Failure:Enabled PF C[DRMF]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits.

#### 7.3.15.16 Instruction ROM Memory Signature Permanent Fail

The BQ76942 device integrates a signature check on the Instruction ROM, which contains internal controller program code. This PF will be checked at initial powerup or device reset. The Instruction ROM PF (IRMF) can be enabled by setting the ***Settings:Permanent Failure:Enabled PF C[IRMF]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits.

#### 7.3.15.17 LFO Oscillator Permanent Fail

The BQ76942 device includes a separate hardware monitor circuit which determines if the LFO oscillator frequency deviates excessively from its expected value. If such a deviation is detected, the device can trigger an LFO Oscillator PF (LFOF) and disable the battery pack. This PF can be enabled by setting the ***Settings:Permanent Failure:Enabled PF C[LFOF]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits.

#### 7.3.15.18 VREF Permanent Fail

The BQ76942 device integrates a diagnostic check on the voltage references used by the device. VREF2, which is used by the coulomb counter and LDOs, is periodically measured using the voltage ADC (which uses VREF1) and can be read back in bytes 0-1 of the *0x0075 DASTATUS5()* subcommand. This command should normally report a value of approximately 19660. If it differs significantly from this, it may indicate that one reference has changed in value significantly relative to the other, meaning reported measurements may no longer be accurate. This ratio is monitored periodically and, if it deviates by more than 10% for four seconds, the device can trigger a VREF PF (VREF) and disable the battery pack. This PF can be enabled by setting the ***Settings:Permanent Failure:Enabled PF C[VREF]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits.

#### 7.3.15.19 VSS Permanent Fail

The BQ76942 device integrates a diagnostic check on the ADC input mux by periodically measuring the VSS voltage level using the voltage ADC. This measurement is reported in bytes 2-3 of the *0x0075 DASTATUS5()* subcommand and should normally report a value that is near zero. If it differs significantly from this, it may indicate the ADC input mux has experienced an error, meaning reported measurements may no longer be accurate. This measurement is monitored by the device and, if not as expected, can trigger a VSS PF (VSSF) and disable the battery pack. This PF can be enabled by setting the ***Settings:Permanent Failure:Enabled PF C[VSSF]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits, and the fail threshold and delay are set by ***Permanent Fail:VSSF:Fail Threshold*** and ***Permanent Fail:VSSF:Delay***.

#### 7.3.15.20 Protection Comparator MUX Permanent Fail

The BQ76942 device implements a periodic check on the input mux for the hardware protection comparator subsystem used for the OV, UV, OCC, OCD1, and OCD2 primary protections. If this check fails, it can trigger a Protection Comparator MUX Permanent Fail (HWMX) and disable the battery pack. This PF can be enabled by setting the ***Settings:Permanent Failure:Enabled PF C[HWMX]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]***configuration bits.

#### 7.3.15.21 Commanded Permanent Fail

The BQ76942 device includes the capability for the host to force a Permanent Fail by sending the *0x2857 PF_FORCE_A()* subcommand followed by the *0x29A3 PF_FORCE_B()* subcommand within 4 seconds. This PF is only allowed if the ***Settings:Permanent Failure:Enabled PF C[CMDF]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]***configuration bits are set.

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#### 7.3.15.22 Top of Stack Measurement Check

The voltage ADC regularly measures the top of stack voltage through an internal divider and reports this in *0x34 Stack Voltage()*. It also compares this measurement to the sum of the individual cell voltage measurements and can trigger a Top of Stack PF (TOSF) and disable the battery pack if they differ excessively. This PF can be enabled by setting the ***Settings:Permanent Failure:Enabled PF D[TOSF]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]***configuration bits, and the fail threshold and delay are set by ***Permanent Fail:TOS:Threshold*** and ***Permanent Fail:TOSF:Delay***. This check is not performed if the current is beyond ***Power:Sleep:Sleep Current***, in order to avoid false triggers due to a dynamic load.

#### 7.3.15.23 Cell Open Wire

The BQ76942 device supports detection of a broken connection between a cell in the pack and the cell attachment to the PCB containing BQ76942. Without this check, the voltage at the cell input pin of the BQ76942 device may persist for some time on the board-level capacitor, leading to incorrect voltage readings. The Cell Open Wire detection in the BQ76942 device operates by enabling a small current source from each cell to VSS at programmable intervals. If a cell input pin is floating due to an open wire condition, this current will discharge the capacitance, causing the voltage at the pin to slowly drop. This drop in voltage will eventually trigger a Cell Undervoltage protection fault on that particular cell, as well as a Cell Overvoltage protection fault on the cell above it. Eventually, the voltage will drop low enough to trigger a Safety Undervoltage PF on the particular cell, or a Safety Overvoltage PF on the cell above it. It is important that the undervoltage and overvoltage protections and PFs be enabled with appropriate threshold settings for the open wire condition to be detected and the desired reaction initiated.

The Cell Open Wire current will be enabled at a periodic interval set by the ***Settings:Cell Open-Wire:Check Time*** configuration register, with a setting of 0 disabling this check entirely. The current source is enabled once every interval for a duration of the ADC measurement time (which is 3 ms by default). This provides programmability in the average current drawn from ≈0.65 nA to ≈165 nA, based on the typical current level of 55 µA. Note: the Cell Open Wire check can create cell imbalance, so the settings should be selected appropriately.

### 7.3.16 Cell Balancing

The BQ76942 device supports passive cell balancing by bypassing the current of a selected cell during charging or at rest, using either integrated bypass switches between cells, or external bypass FET switches. The device incorporates a voltage-based balancing algorithm which can optionally autonomously balance cells without requiring any interaction with a host processor. Or if preferred, balancing can be entirely controlled manually from a host processor. For autonomous balancing, the device will only balance non-adjacent cells in use (it does not consider inputs used to measure interconnect as cells in use). In order to avoid excessive power dissipation within the BQ76942 device, the maximum number of cells allowed to balance simultaneously can be limited by setting ***Settings:Cell Balancing Config:Balancing Configuration:Cell Balance Max Cells***. For host-controlled balancing, adjacent as well as non-adjacent cells can be balanced.

Host-controlled balancing can be controlled using specific subcommands sent by the host, these subcommands are also accessible in SEALED mode, to avoid the need for the pack to be unsealed in operation in order to initiate balancing. If host-controlled balancing will not be used, access to these subcommands can be disabled by clearing the ***Settings:Cell Balancing Config:Balancing Configuration[CB_NO_CMD]*** configuration bit.

The subcommands used by the host to control cell balancing are described below.

**Table 32. Host-controlled Cell Balancing Subcommands**

| Subcommand | Description |
|---|---|
| 0x0083 CB_ACTIVE_CELLS() | When read, reports a bit mask of which cells are being actively balanced. When written, starts balancing on the specified cells. Write 0x0000 to turn balancing off. |
| 0x0084 CB_SET_LVL() | When written with a 16-bit cell voltage threshold in mV, the device begins balancing one or more of the highest voltage cells if above the written threshold. When read, returns the threshold. |

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The device also returns status information regarding how long cells have been balanced through the subcommands described below.

**Table 33. Cell Balancing Status Subcommands**

| Subcommand | Description |
|---|---|
| 0x0085 CBSTATUS1() | When read, returns the 16-bit time in seconds that balancing has been active. |
| 0x0086 CBSTATUS2() | When read, returns a block containing the 32-bit cumulative balancing times in seconds for each of cells 1 - 8. These values will reset if a device reset occurs, or the device enters CONFIG_UPDATE mode. |
| 0x0087 CBSTATUS3() | When read, returns a block containing the 32-bit cumulative balancing times in seconds for each of cells 9 - 10. These values will reset if a device reset occurs, or the device enters CONFIG_UPDATE mode. |

When host-controlled balancing is initiated using the subcommands above, the device starts a timer and will continue balancing until the timer reaches a value of ***Settings:Cell Balancing Config:Cell Balance Interval***, or a new balancing subcommand is issued (which resets the timer). This is included as a precaution, in case the host processor initiated balancing but then stopped communication with the BQ76942 device, so that balancing would not continue indefinitely.

The BQ76942 device can automatically balance cells using a voltage-based algorithm based on environmental and system conditions. Several settings are provided to control when balancing is allowed, as described below.

**Temperature** - the device will disable balancing (both autonomous and host-controlled) if the cell temperature is below *Settings:Cell Balancing Config:Min Cell Temp* or above *Settings:Cell Balancing Config:Max Cell Temp* or the internal die temperature of the device is above *Settings:Cell Balancing Config:Max Internal Temp*.

**Charge versus Relax** - autonomous balancing can be allowed during charging by setting *Settings:Cell Balancing Config:Balancing Configuration[CB_CHG]*, or in a relaxed condition by setting *Settings:Cell Balancing Config:Balancing Configuration[CB_RLX]*, or both. If *Settings:Cell Balancing Config:Balancing Configuration[CB_CHG]* is set, autonomous balancing is allowed while the CC1 Current is above *Settings:Current Thresholds:Chg Current Threshold*. If *Settings:Cell Balancing Config:Balancing Configuration[CB_RLX]* is set, autonomous balancing is allowed while the current is below *Settings:Current Thresholds:Chg Current Threshold* and above the negative of *Settings:Current Thresholds:Dsg Current Threshold*. The device evaluates the conditions for continuing balancing every *Settings:Cell Balancing Config:Cell Balance Interval*. For example, if the device is configured to avoid balancing during charge, and while balancing the pack begins charging, balancing will continue until the interval timer expires before it is disabled.

**Cell Voltage** - if autonomous balancing during charge is enabled, the device will allow balancing if the minimum cell voltage is above *Settings:Cell Balancing Config:Cell Balance Min Cell V (Charge)* and the difference between the maximum and minimum cell voltages is greater than *Settings:Cell Balancing Config:Cell Balance Min Delta (Charge)*. Similarly, if autonomous balancing during relax is enabled, the device will allow balancing if the minimum cell voltage is above *Settings:Cell Balancing Config:Cell Balance Min Cell V (Relax)* and the difference between the maximum and minimum cell voltages is greater than *Settings:Cell Balancing Config:Cell Balance Min Delta (Relax)*.

While balancing during relax, when the device re-evaluates the cell status at the end of each timer interval, it will cease balancing if all cell voltages are within *Settings:Cell Balancing Config:Cell Balance Stop Delta (Relax)* of the minimum cell voltage. This **Cell Balance Stop Delta** reduces the risk of over-balancing a higher voltage cell to slightly below the minimum voltage cell, and thereby slowly draining the pack. Operation while balancing during charge is similar, instead using the *Settings:Cell Balancing Config:Cell Balance Stop Delta (Charge)* configuration value. The **Cell Balance Stop Delta** parameters should be set to a lower level than the **Cell Balance Min Delta** parameters, then the device will have a hysteresis that delays restarting balancing until the level of imbalance again exceeds the higher **Cell Balance Min Delta** level.

**NORMAL versus SLEEP Mode** - the BQ76942 device can also be configured to avoid autonomous balancing while in SLEEP mode by clearing the *Settings:Cell Balancing Config:Balancing Configuration[CB_SLEEP]* configuration bit. The device can also be prevented from entering SLEEP mode while balancing if the *Settings:Cell Balancing Config:Balancing Configuration[CB_NOSLEEP]* bit is set.

Note: balancing is disabled immediately (without waiting for the interval timer to expire) if any of the following events occur:

- The device enters CONFIG_UPDATE mode.
- An enabled protection alert occurs.
- An enabled protection fault occurs.

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- The device enters DEEPSLEEP mode, which may occur due to a Permanent Fail event.
- The device enters SHUTDOWN mode.

Due to the current that flows into the cell input pins on the BQ76942 device while balancing is active, the measurement of cell voltages and evaluation of cell voltage protections by the device is modified during balancing. Balancing is temporarily disabled during the regular measurement loop while the actively balanced cell is being measured by the ADC, as well as when the cells immediately adjacent to the active cell are being measured. Similarly, balancing on the top cell is disabled while the stack voltage measurement is underway. This occurs on every measurement loop, and so can result in significant reduction in the average balancing current that flows. In order to help alleviate this, the ***Settings:Configuration:Power Config[CB_LOOP_SLOW_1:0]*** configuration bits cause the device to slow the measurement loop speed when cell balancing is active, as shown below. The BQ76942 device will insert current-only measurements after each voltage and temperature scan loop to slow down voltage measurements and thereby increase the average balancing current.

**Table 34. Cell Balancing Loop Slow-down Setting**

| CB_LOOP_SLOW_1 | CB_LOOP_SLOW_1 | Pin Function |
|---|---|---|
| 0 | 0 | Measurement loop runs at full speed during balancing |
| 0 | 1 | Measurement loop runs at half speed during balancing |
| 1 | 0 | Measurement loop runs at quarter speed during balancing |
| 1 | 1 | Measurement loop runs at eighth speed during balancing |

In order to avoid the balancing current causing a protection alert or fault, the device modifies the timing on the CUV check on an actively balanced cell and the COV checks on adjacent cells, disabling balancing briefly every 1-sec to allow these checks to occur. If a CUV or COV alert is detected at the 1-sec check, balancing is immediately disabled. Note: the device will therefore have a different delay (≈ 1-sec) in triggering a CUV or COV alert or fault on these cells while balancing is active. Timing for CUV and COV on other cells besides these being actively balanced or adjacent are not modified.

The device includes an internal die temperature check, to disable balancing if the die temperature exceeds a programmable threshold. However, the customer should still carefully analyze the thermal effect of the balancing on the device in system. Based on the planned ambient temperature of the device during operation and the thermal properties of the package, the maximum power should be calculated that can be dissipated within the device and still ensure operation remains within the recommended operating temperature range. The cell balancing configuration can then be determined such that the device power remains below this level by limiting the maximum number of cells that can be balanced simultaneously, or by reducing the balancing current of each cell by appropriate selection of the external resistance in series with each cell.

### 7.3.17 Low Frequency Oscillator

The low frequency oscillator (LFO) in the BQ76942 device operates continuously while in NORMAL and SLEEP modes, and can be configured to remain powered or shutdown (except when needed) during DEEPSLEEP mode. The LFO runs at ≈262.144 kHz during NORMAL mode, and reduces to ≈32.768 kHz in SLEEP or DEEPSLEEP modes. The LFO is trimmed during manufacturing to meet the specified accuracy across temperature.

### 7.3.18 High Frequency Oscillator

The high frequency oscillator (HFO) in the BQ76942 device operates at 16.78 MHz and is frequency locked to the LFO. The HFO powers up as needed for internal logic functions.

### 7.3.19 Device Security

The BQ76942 device includes three security modes: SEALED, UNSEALED, and FULL ACCESS, which can be used to limit the ability to view or change settings.

In SEALED mode, most data and status can be read using commands and subcommands, but only selected settings can be changed. Data memory settings cannot be changed directly.

UNSEALED mode includes SEALED functionality, and also adds the ability to execute additional subcommands, and read and write data memory.

FULL ACCESS mode allows capability to read and modify all device settings, including writing OTP memory.

Selected settings in the device can be modified while the device is in operation through supported commands and subcommands, but in order to modify all settings, the device must enter CONFIG_UPDATE mode (see CONFIG_UPDATE Mode), which stops device operation while settings are being updated. After the update is completed, operation is restarted using the new settings. CONFIG_UPDATE mode is only available in FULL ACCESS mode.

The BQ76942 device implements a key-access scheme to transition among SEALED, UNSEALED, and FULL ACCESS modes. Each transition requires that a unique set of keys be sent to the device through the subcommand address (0x3E and 0x3F). The keys must be sent consecutively to 0x3E and 0x3F, with no other data written between the keys. Do not set the two keys to identical values. When in the SEALED mode, the *0x12 Battery Status()[SEC1, SEC0]* bits are set to [1, 1]. When the UNSEAL keys are correctly received by the device, the bits will be set to [1, 0]. When the FULL ACCESS keys are correctly received, then the bits will change to [0, 1]. The state [0, 0] is not valid, and only indicates that the state has not yet been loaded.

The unseal keys are stored in data memory in ***Security:Keys:Unseal Key Step 1*** and ***Security:Keys:Unseal Key Step 2***. The FULL ACCESS keys are stored in ***Security:Keys:Full Access Key Step 1*** and ***Security:Keys:Full Access Key Step 2***. The access keys are changed during operation using the *0x0035 SECURITY_KEYS()* subcommand. This subcommand enables a R/W of the 4 key words (8 bytes). Each word is sent in big endian order using this subcommand, with the first two words being the unseal code and the remaining two words being the full access codes.

When using the codes by writing them to 0x3E and 0x3F, they must be sent in little endian order; therefore, if 0x1234 and 0x5678 are written as the unseal codes to *0x0035 SECURITY_KEYS()*, then to unseal requires writing 0x34 and 0x12 to 0x3E and 0x3F, followed by writing 0x78 and 0x56 to 0x3E and 0x3F. The two codes must be written within 4 s of each other to succeed.

To read the keys:

1. Write 0x35 and 0x00 to 0x3E and 0x3F
2. Read back 8 bytes from the transfer buffer at 0x40–0x47.

To write the keys:

1. Write 0x35 and 0x00 to 0x3E and 0x3F.
2. Write the data in big endian format to the transfer buffer at 0x40–0x47.
3. Write the checksum to 0x60. The checksum is the complement of the sum of the data and command bytes.
4. Write the length of 0x0A to 0x61. The length includes the command, data, checksum, and length bytes.

To set the device into SEALED mode when initially powering up, the ***Security:Settings:Security Settings[SEAL]*** configuration bit can be set. During operation, the device can be put into SEALED mode by sending the *0x0030 SEAL()* subcommand.

The BQ76942 device includes additional means to limit further modification of device settings. If the ***Security:Settings:Security Settings[LOCK_CFG]*** configuration bit is set, the data memory settings can no longer be modified when the device is in CONFIG_UPDATE mode. If the ***Security:Settings:Security Settings[PERM_SEAL]*** bit is set, the device cannot be unsealed after it has been sealed.

The device provides additional checks which can be used to optimize system robustness:

The *0x0004 IROM_SIG()* subcommand calculates a digital signature of the integrated instruction ROM, and the *0x0009 DROM_SIG()* subcommand calculates a similar signature of the integrated data ROM (which contains the default values for the device). These signatures should never change for a particular product. If these were to change, it would indicate an error, either that the ROM had been corrupted, or the readback of the ROM or calculation of the signature experienced an error.

The *0x0005 STATIC_CFG_SIG()* subcommand calculates a digital signature for the static configuration data (which excludes calibration values) and compares it to a stored value. If the result does not match the stored signature, the MSB returned is set.

### 7.3.20 *0x00 Control Status()* and *0x12 Battery Status()* Commands

The BQ76942 device includes *0x00 Control Status()* and *0x12 Battery Status()* commands, which report various status information on the pack. The *0x00 Control Status()* command behaves similarly to 0x3E and 0x3F when written, this functionality is included for legacy auto-detection and is not recommended for customer usage. When this command is read back immediately after it has been written, it will return 0xFFA5 once. Subsequent reads will return the *0x00 Control Status()* data, which is described below with the *0x12 Battery Status()* details.

**Table 35. *0x00 Control Status()* Bit Definitions**

| Bit | Name | Description |
|---|---|---|
| 15 - 3 | RSVD | Reserved |
| 2 | DEEPSLEEP | This bit indicates whether or not the device is in DEEPSLEEP mode.<br>DEEPSLEEP = 0: Device is in DEEPSLEEP mode.<br>DEEPSLEEP = 1: Device is not in DEEPSLEEP mode. |
| 1 | LD_TIMEOUT | This bit is set when the Load Detect function has timed out and checking has stopped.<br>LD_TIMEOUT = 0: Load Detect function has not timed out or is inactive.<br>LD_TIMEOUT = 1: Load Detection function timed out and was deactivated. |
| 0 | LD_ON | This bit indicates whether or not the Load Detect pullup was active during the previous LD pin voltage measurement.<br>LD_ON = 0: LD pullup was not active during the previous LD pin measurement.<br>LD_ON = 1: LD pullup was active during the previous LD pin measurement. |

**Table 36. *0x12 Battery Status()* Bit Definitions**

| Bit | Name | Description |
|---|---|---|
| 15 | SLEEP | This bit indicates whether or not the device is presently in SLEEP mode.<br>SLEEP = 0: Device is not in SLEEP mode.<br>SLEEP = 1: Device is in SLEEP mode. |
| 14 | RSVD | Reserved |
| 13 | SDM | SHUTDOWN mode is pending because the Shutdown() subcommand was received, or the RST_SHUT pin was asserted for > 1-sec.<br>SDM = 0: Shutdown due to command or pin is not pending.<br>SDM = 1: Shutdown due to command or pin is pending. |
| 12 | PF | Indicates whether a Permanent Fail fault has triggered.<br>PF = 0: No Permanent Fail fault has triggered.<br>PF = 1: At least one Permanent Fail fault has triggered. |
| 11 | SS | Indicates whether an enabled safety fault has triggered<br>SS = 0: No safety fault is triggered.<br>SS = 1: At least one enabled safety fault is triggered. |
| 10 | FUSE | Reports the most recently observed state of the FUSE pin, is updated every second in NORMAL mode.<br>FUSE = 0: FUSE pin was not asserted by device or secondary protector at last sample.<br>FUSE = 1: FUSE pin was asserted by device or secondary protector at last sample. |
| 9 | SEC1 | SEC1:0 indicate the present security state of the device.<br>SEC1:0 = 0: Device has not initialized yet.<br>SEC1:0 = 1: Device is in FULLACCESS mode.<br>SEC1:0 = 2: Device is in UNSEALED mode.<br>SEC1:0 = 3: Device is in SEALED mode.<br>When in SEALED mode, device configuration may not be read or written and some commands are restricted.<br>When in UNSEALED mode, device configuration may normally be read and may be written while in CONFIG_UPDATE mode.<br>When in FULLACCESS mode, unrestricted read and write access is allowed and all commands are accepted. |
| 8 | SEC0 | |
| 7 | OTPB | This bit indicates whether or not voltage and temperature conditions are valid for OTP programming. During normal operation, this bit will always be set if [[Manufacturing Status()[OTPW]]] is clear. When entering CONFIG_UPDATE mode, conditions will be checked and this bit will reflect whether or not programming is allowed ([[Manufacturing Status()[OTPW]]] does not apply in CONFIG_UPDATE mode). Once in CONFIG_UPDATE mode, this bit will not change state since no new measurements are being taken.<br>OTPB = 0: OTP writes are allowed.<br>OTPB = 1: Writes to OTP are blocked. |
| 6 | OTPW | This bit indicates whether or not some data is waiting to be written to OTP during normal operation. This can occur when, for example, configured to Permanent Fail information to OTP. This bit may remain set until conditions for OTP programming are met and all data is programmed. This bit is not set during OTP programming from CONFIG_UPDATE mode.<br>OTPW = 0: No writes to OTP are pending.<br>OTPW = 1: Writes to OTP are pending. |

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**Table 36. *0x12 Battery Status()* Bit Definitions (continued)**

| Bit | Name | Description |
|---|---|---|
| 5 | COW_CHK | This bit indicates while cell open-wire checks are occurring. When the feature is disabled, this bit will not set. When the feature is enabled, this bit will set periodically as the checks are performed.<br>COW_CHK = 0: Device is not actively performing a cell open-wire check.<br>COW_CHK = 1: Device is actively performing a cell open-wire check. |
| 4 | WD | This bit indicates whether or not the previous device reset was caused by the internal watchdog timer. This is not related to the Host Watchdog protection.<br>WD = 0: Previous reset was normal.<br>WD = 1: Previous reset was caused by the watchdog timer. |
| 3 | POR | This bit is set when the device fully resets. It is cleared upon exit of CONFIG_UPDATE mode. It can be used by the host to determine if any RAM configuration changes were lost due to a reset.<br>POR = 0: Full reset has not occurred since last exit of CONFIG_UPDATE mode.<br>POR = 1: Full reset has occurred since last exit of CONFIG_UPDATE and reconfiguration of any RAM settings is required. |
| 2 | SLEEP_EN | This bit indicates whether or not SLEEP mode is allowed based on configuration and commands. The [[Power Config[SLEEP_EN]]] bit sets the default state of this bit. The host may send commands to enable or disable SLEEP mode based on system requirements. When this bit is set, the device may transition to SLEEP mode when other SLEEP criteria are met.<br>SLEEP_EN = 0: SLEEP mode is disabled by the host.<br>SLEEP_EN = 1: SLEEP mode is allowed when other SLEEP conditions are met. |
| 1 | PCHG_MODE | This bit indicates whether or not the device is in precharge mode. In precharge mode, the PCHG FET is turned on instead of the CHG FET.<br>PCHG_MODE = 0: Device is not in precharge mode.<br>PCHG_MODE = 1: Device is in precharge mode. |
| 0 | CFGUPDATE | This bit indicates whether or not the device is in CONFIG_UPDATE mode. It will be set after the *0x0090 ENTER_CFG_UPDATE()* subcommand is received and fully processed. Configuration settings may be changed only while this bit is set.<br>CFGUPDATE = 0: Device is not in CONFIG_UPDATE mode.<br>CFGUPDATE = 1: Device is in CONFIG_UPDATE mode. |

### 7.3.21 Fuse Drive

The FUSE pin on the BQ76942 device can be used to blow a chemical fuse in the presence of a Permanent Fail (PF), as well as to detect if an external secondary protector in the system has detected a fault and is attempting to blow the fuse itself. The pin is intended to drive the gate of an NFET, which can be combined with the drive from an external secondary protector, as shown in Figure 9. When the FUSE pin is not being asserted by the BQ76942 device, it remains in a high-impedance state and will detect a voltage applied at the pin by a secondary protector. If the Second Level Protector PF is enabled (using the ***Settings:Permanent Failure:Enabled PF B[2LVL]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits), a PF will be generated if the device detects a high signal at the FUSE pin.

The device can be configured to blow the fuse when a PF occurs by setting the ***Settings:Protection:Protection Configuration[PF_FUSE]*** configuration bit. If this is set, the device will only attempt to blow the fuse if the stack voltage is above a threshold given by ***Settings:Fuse:Min Blow Fuse Voltage***, based on a system configuration with the fuse placed between the top of stack and the high-side protection FETs. If instead the fuse is placed between the FETs and the PACK+ connector, then the ***Settings:Protection:Protection Configuration[PACK_FUSE]*** bit should be set, and the device will instead base its decision on the PACK Pin Voltage. This voltage threshold check will be disregarded if a FET Failure PF (CFETF or DFETF) has occurred and the ***Settings:Protection:Protection Configuration[FETF_FUSE]*** bit is set.

When the FUSE pin is asserted to blow the external fuse, it will only stay asserted for a length of time set by the ***Settings:Fuse:Fuse Blow Timeout*** configuration register.

The status of the FUSE pin is provided in the *0x12 Battery Status[FUSE]* bit.

The *0x001D FUSE_TOGGLE()* subcommand can be used to toggle the state of the FUSE pin drive. The *0x0026 FUSE_ENABLE()* subcommand will toggle the state of the ***Settings:Protection:Protection Configuration[PF_FUSE]*** bit.

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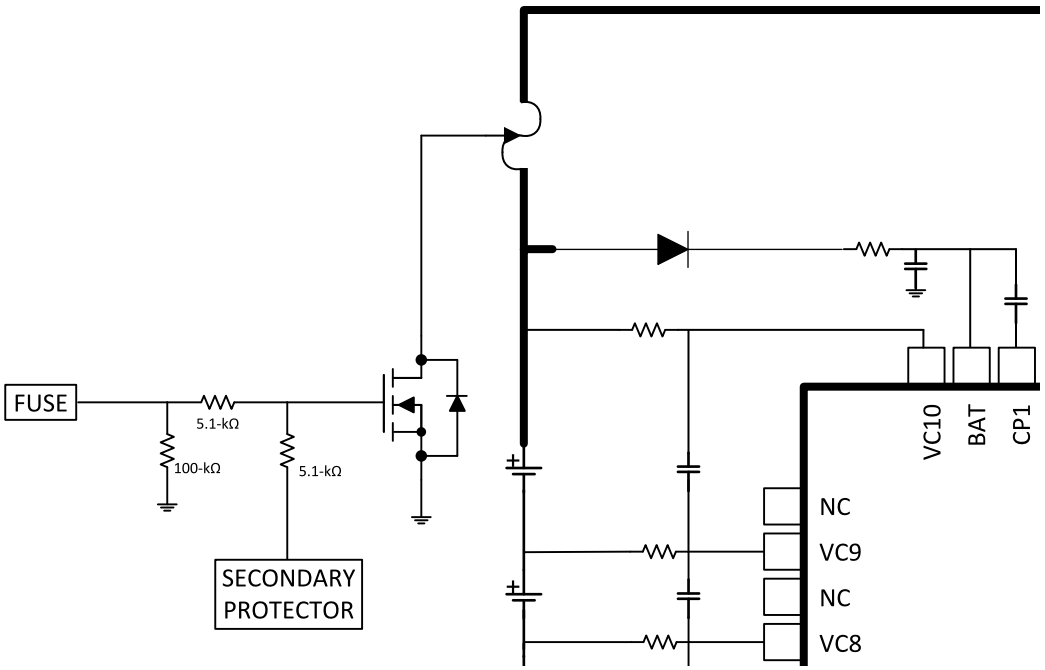


**Figure 9. FUSE pin operation**

### 7.3.22 *0x0070 MANU_DATA()* Subcommand

The BQ76942 device integrates a 32-byte scratchpad memory which can be used by the customer for storing manufacturing data, such as serial numbers, production or test dates, and so forth, which can be written into OTP memory on the customer production line. This data can only be written while in FULLACCESS mode, although it can be read in all modes. The data is read or written using the *0x0070 MANU_DATA()* subcommand.

### 7.3.23 Diagnostics

The BQ76942 device includes a suite of diagnostic tests which can be utilized by the system to improve robustness of operation.

#### *7.3.23.1 VREF2 Versus VREF1 Measurement*

The VREF2, which is used by the coulomb counter and LDOs, is measured using the voltage ADC (which uses VREF1) and can be read back in bytes 0-1 of the *0x0075 DASTATUS5()* subcommand. This command should normally report a value of approximately 19660. If it differs significantly from this, it may indicate that one reference has changed in value significantly relative to the other, meaning reported measurements may no longer be accurate. This ratio is monitored periodically and, if it deviates by more than 10% for four seconds, the device can trigger a Permanent Fail (PF) and disable the battery pack. This PF can be enabled by setting the ***Settings:Permanent Failure:Enabled PF C[VREF]*** configuration bit.

#### *7.3.23.2 VSS Measurement*

The voltage ADC regularly measures the VSS signal and reports the result in bytes 2-3 of the *0x0075 DASTATUS5()* subcommand. This command should normally report a value that is near zero. If it differs significantly from this, it may indicate the ADC input mux has experienced an error, meaning reported measurements may no longer be accurate. This measurement is monitored by the device and, if not as expected, can trigger a Permanent Fail (PF) and disable the battery pack. This PF can be enabled by setting the ***Settings:Permanent Failure:Enabled PF C[VSSF]*** configuration bit, and the fail threshold and delay are set by ***Permanent Fail:VSSF:Fail Threshold*** and ***Permanent Fail:VSSF:Delay***.

#### 7.3.23.3 Top of Stack Measurement Check

The voltage ADC regularly measures the top of stack voltage through an internal divider and reports this in *0x34 Stack Voltage()*. It also compares this measurement to the sum of the individual cell voltage measurements and can trigger a Permanent Fail (PF) and disable the battery pack. This PF can be enabled by setting the ***Settings:Permanent Failure:Enabled PF D[TOSF]*** configuration bit, and the fail threshold and delay are set by ***Permanent Fail:TOS:Threshold*** and ***Permanent Fail:TOSF:Delay***. This check is not performed if the current is beyond ***Power:Sleep:Sleep Current***, in order to avoid false triggers due to a dynamic load.

#### 7.3.23.4 LFO Oscillator Monitor

The BQ76942 device includes a separate hardware monitor circuit which determines if the LFO oscillator frequency deviates excessively from its expected value. If such a deviation is detected, the device can trigger a Permanent Fail (PF) and disable the battery pack. This PF can be enabled by setting the ***Settings:Permanent Failure:Enabled PF C[LFOF]*** configuration bit.

#### 7.3.23.5 Protection Comparator Mux Check

The BQ76942 device implements a periodic check on the input mux for the hardware protection comparator subsystem used for the OV, UV, OCC, OCD1, and OCD2 primary protections. If this check fails, it can trigger a Permanent Fail (PF) and disable the battery pack. This PF can be enabled by setting the ***Settings:Permanent Failure:Enabled PF C[HWMX]*** configuration bit.

#### 7.3.23.6 Internal Watchdog Reset

The BQ76942 device integrates an internal watchdog circuit for the internal processor, which will trigger a watchdog fault if it is not serviced by the processor at regular intervals. A watchdog fault may occur if the internal processor is unexpectedly halted or overloaded with tasks, such as servicing excessive serial communications. When a watchdog fault occurs, the internal processor is reset, and the *0x12 Battery Status()[WD]* bit will be set after the reset is complete.

There are additional checks performed by the device which can also trigger a watchdog reset. The BQ76942 device incorporates an ADC measurement watchdog, which monitors whether the ADC and coulomb counter measurements are completing as expected, and if not will trigger a watchdog fault. A RAM integrity check is also performed periodically and forces a watchdog reset if corruption is detected. If the device detects a RAM error within a programmable time (set by ***Power:Shutdown:RAM Fail Shutdown Time***) after a watchdog reset, the device will enter SHUTDOWN mode instead of resetting, in order to avoid unwanted reset loops in the case of a RAM failure.

#### 7.3.23.7 Internal Memory Checks

The BQ76942 device implements a signature check on the instruction ROM for the internal processor at initial power up or upon reset. If this fails, the device can trigger a Permanent Fail (PF) and disable the battery pack. This PF can be enabled by setting the ***Settings:Permanent Failure:Enabled PF C[IRMF]*** configuration bit.

The device also implements a signature check at initial power up or after reset on the internal processor data ROM, which holds default values for the device configuration. If this fails, the device can trigger a Permanent Fail (PF) and disable the battery pack. This PF can be enabled by setting the ***Settings:Permanent Failure:Enabled PF C[DRMF]*** configuration bit.

The device also implements a signature check at initial power up or after reset on the internal OTP memories, one of which may contain customer configuration data, while another contains factory trim information. If this check fails, the device can trigger a Permanent Fail (PF) and disable the battery pack. This PF can be enabled by setting the ***Settings:Permanent Failure:Enabled PF C[OTPF]*** configuration bit.

### 7.3.24 Serial Communications Interfaces

The BQ76942 device integrates three serial communication interfaces - an $I^2C$ bus, which supports 100 kHz and 400 kHz modes with an optional CRC check, an SPI bus with an optional CRC check, which supports a clock rate up to 2 MHz, and a single-wire HDQ interface. The device is configured default in $I^2C$ mode, and can be changed to SPI or HDQ mode by programming either the register or OTP configuration accordingly. The customer can program the device's integrated OTP on the manufacturing line to set the desired communications speed and protocol to be used at power up in operation.

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The ***Settings:Configuration:Comm Type*** configuration register controls the active communication mode of the BQ76942 device. These settings are shown below.

**Table 37. Comm Type Data Memory Settings**

| Comm Type Setting | Description |
|---|---|
| 0x00 | Default ( $I^2C$ Fast (for use above 100 kHz bus speed) |
| 0x03 | HDQ using the ALERT pin |
| 0x04 | HDQ using the HDQ pin |
| 0x07 | $I^2C$ (for use up to 100 kHz bus speed) |
| 0x08 | $I^2C$ Fast (for use above 100 kHz bus speed) |
| 0x09 | $I^2C$ Fast with timeouts (for use above 100 kHz bus speed) |
| 0x0F | SPI |
| 0x10 | SPI with CRC |
| 0x11 | $I^2C$ with CRC (for use up to 100 kHz bus speed) |
| 0x12 | $I^2C$ Fast with CRC (for use above 100 kHz bus speed) |
| 0x1E | $I^2C$ with timeouts (for use with 100 kHz bus speed) |
| 0xFF | $I^2C$ Fast (for use above 100 kHz bus speed) |
| All other values | Reserved. Do not use. |

#### *7.3.24.1 $I^2C$ Communications Subsystem*

The $I^2C$ serial communications interface in the BQ76942 device acts as a slave device and supports rates up to 400 kHz with an optional CRC check. If the OTP has not been programmed, the device will initially power up by default in 400 kHz $I^2C$ mode. The OTP setting can be programmed on the manufacturing line, then when the device powers up, it will automatically enter the selected mode per OTP setting. The host can also change the $I^2C$ speed setting while in CONFIG_UPDATE mode, then the new speed setting will take effect upon exit of CONFIG_UPDATE mode. Alternatively, the host can write the *0x29e7 SWAP_TO_I2C()* subcommand to change the communications interface to $I^2C$ immediately. The *0x29BC SWAP_COMM_MODE()* subcommand can be sent to transition the device to the communications mode selected by the setting in ***Settings:Configuration:Comm Type***.

The $I^2C$ device address is set by default as 0x10 (write), 0x11 (read), which can be changed by programming ***Settings:Configuration:I2C Address*** with the desired write address.

The communications interface includes optional timeout capability which can be enabled based on the ***Comm Type*** setting. The ***Comm Type*** settings with timeouts should only be used if the bus will be operating at 100 kHz or 400 kHz. If ***Comm Type***= 0x1E (100 kHz mode with timeouts enabled), then the device will reset the communications interface logic if a clock is detected low longer than a $t_{TIMEOUT}$ of 25 ms to 35 ms, or if the cumulative clock low slave extend time exceeds ≈25 ms, or if the cumulative clock low master extend time exceeds 10 ms. If ***Comm Type***= 0x09 (400 kHz mode with timeouts enabled), then the device will reset the communications interface logic if a clock is detected low longer than $t_{TIMEOUT}$ of 5 ms to 20 ms. The bus also includes a long-term timeout if the SCL pin is detected low for more than 2 seconds, which applies whether the ***Comm Type*** setting includes timeouts or not.

An $I^2C$ write transaction is shown in Figure 10. Block writes are allowed by sending additional data bytes before the Stop. The $I^2C$ logic will auto-increment the register address after each data byte.

When enabled, the CRC is calculated as follows:

- In a single-byte write transaction, the CRC is calculated over the slave address, register address, and data.
- In a block write transaction, the CRC for the first data byte is calculated over the slave address, register address, and data. The CRC for subsequent data bytes is calculated over the data byte only.

The CRC polynomial is $x^8 + x^2 + x + 1$, and the initial value is 0.

When the slave detects a bad CRC, the $I^2C$ slave will NACK the CRC, which causes the $I^2C$ slave to go to an idle state.

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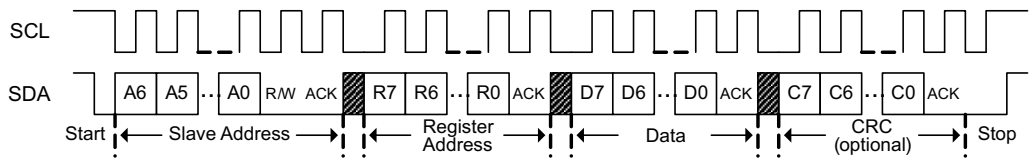


**Figure 10. I²C Write**

Figure 11 shows a read transaction using a Repeated Start.

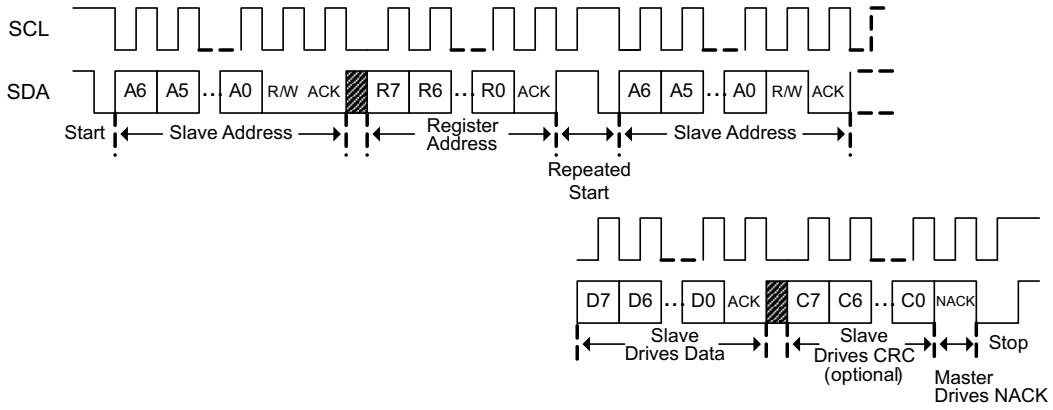


**Figure 11. I²C Read with Repeated Start**

Figure 12 shows a read transaction where a Repeated Start is not used, for example if not available in hardware. For a block read, the master ACK's each data byte except the last and continues to clock the interface. The I²C block will auto-increment the register address after each data byte.

When enabled, the CRC for a read transaction is calculated as follows:

- In a single-byte read transaction, the CRC is calculated beginning at the first start, so will include the slave address, the register address, then the slave address with read bit set, then the data byte.
- In a block read transaction, the CRC for the first data byte is calculated beginning at the first start and will include the slave address, the register address, then the slave address with read bit set, then the data byte. The CRC resets after each data byte and after each stop. The CRC for subsequent data bytes is calculated over the data byte only.

The CRC polynomial is $x^8 + x^2 + x + 1$, and the initial value is 0.

When the master detects a bad CRC, the I²C master will NACK the CRC, which causes the I²C slave to go to an idle state.

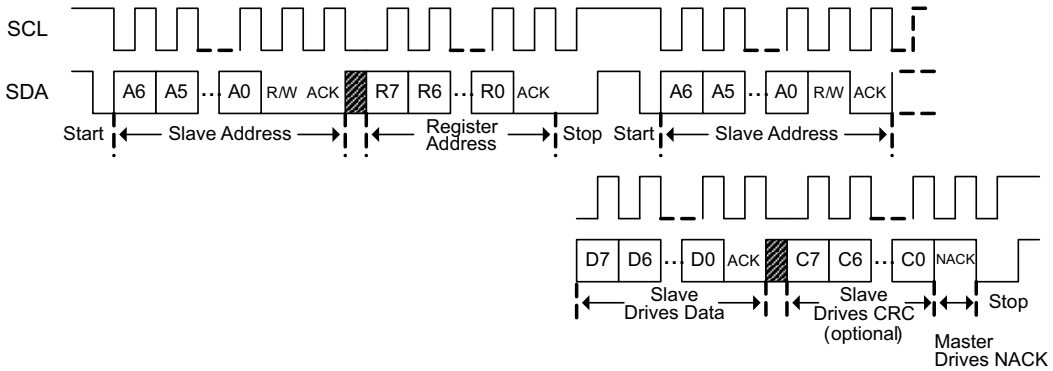


**Figure 12. I²C Read Without Repeated Start**

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#### 7.3.24.2 SPI Communications Interface

The SPI interface in the BQ76942 device operates as a slave-only interface and supports rates up to 2 MHz with an optional CRC check. If the OTP has not been programmed, the device will initially power up by default in 400 kHz $I^2C$ mode. The OTP setting to select SPI mode (set by ***Settings:Configuration:Comm Type***) can be programmed on the manufacturing line to select SPI mode, then when the device powers up, it will automatically enter SPI mode. The host can also change the serial communication setting while in CONFIG_UPDATE mode, although the device will not immediately change communication mode upon exit of CONFIG_UPDATE mode, in order to avoid losing communications during evaluation or production. The host can reset the device or write the *0x7C35 SWAP_TO_SPI()* subcommand to change the communications interface to SPI immediately. Alternatively, the *0x29BC SWAP_COMM_MODE()* subcommand can be sent to transition the device to the communications mode selected by the setting in ***Settings:Configuration:Comm Type***.

The SPI interface logic operates with clock polarity (CPOL) = 0 and clock phase (CPHA) = 0, as shown in the figure below.

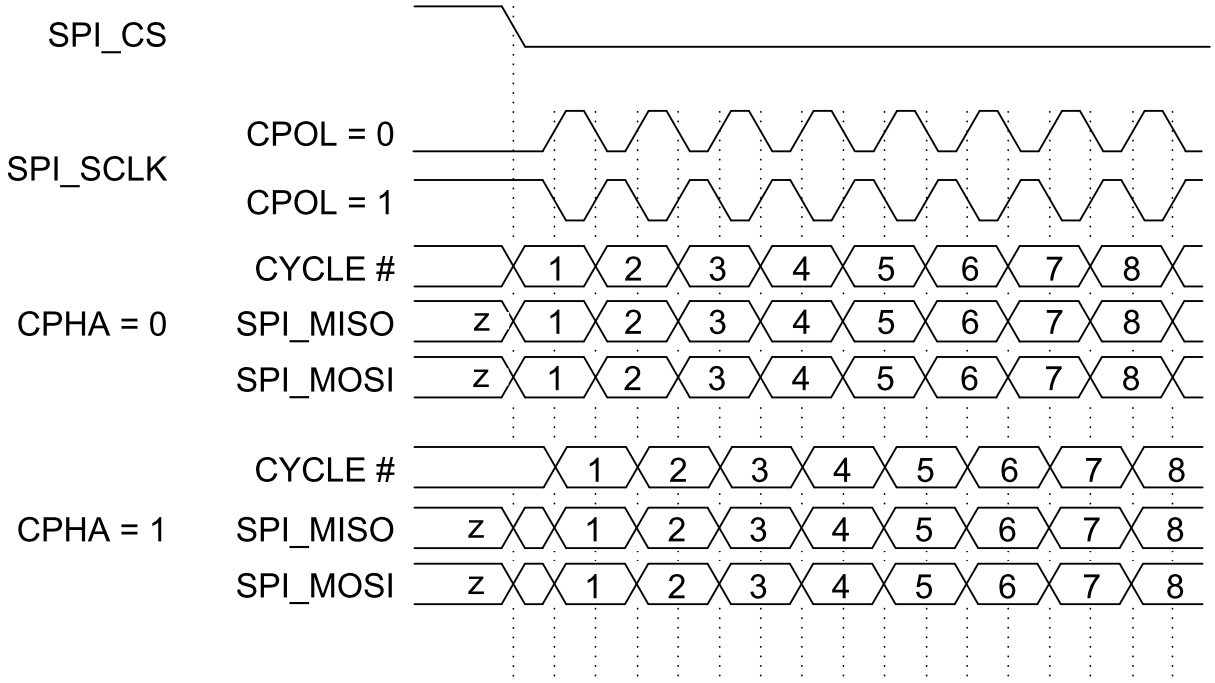


**Figure 13. SPI with CPOL = 0 and CPHA = 0**

The device also includes an optional 8-bit CRC using polynomial $x^8+x^2+x+1$. The interface must use 16-bit transactions if CRC is not enabled, and must use 24-bit transactions when CRC is enabled. CRC mode is enabled or disabled based on the setting of ***Settings:Configuration:Comm Type***. Based on control settings, the logic will:

(a) only work with CRC, will not accept data without valid CRC, or

(b) will only accept transactions without CRC (so the host must only clock 16-bits per transaction, the device will detect an error if more or less clocks are sent).

If the host performs a write with CRC and the CRC is not correct, then the incoming data is not transferred to the incoming buffer, and the outgoing buffer (used for the next transaction) is also reset to 0xFFFF. This transaction is considered invalid. On the next transaction, the CRC (if clocked out) will be 0xAA, so the 0xFFFFAA will indicate to the master that a CRC error was detected.

The internal oscillator in the BQ76942 device may not be running when the host initiates a transaction (for example, this can occur if the device is in SLEEP mode). If this occurs, the interface will drive out 0xFFFF on SPI_MISO for the first 16-bits clocked out. It will also drive out 0xFF for the third (CRC) byte as well, if CRC is enabled. So the 0xFFFFFF will indicate to the master that the internal oscillator is not ready yet.

The device will automatically wake the internal oscillator at a falling edge of SPI_CS, but it may take up to 50µs to stabilize and be available for use to the SPI interface logic. The address 0x7F used in the device is defined in such a manner that there should be no valid transaction to write 0xFF into this address. Thus the two-byte pattern 0xFFFF should never occur as a valid sequence in the first two bytes of a transaction (that is, it is only used as a flag that something is wrong, similar to an $I^2C$ NACK).

The device includes ability to detect a frozen or disconnected SPI bus condition, and it will then reset the bus logic. This condition is recognized when the SPI_CS is low and the SPI_SCLK is static and not changing for a two second timeout.

#### 7.3.24.2.1 SPI Protocol

The first byte of a SPI transaction consists of an R/W bit (R=0, W=1), followed by a 7-bit address, MSB-first. If the master (host) is writing, then the second byte will be the data to be written. If the master is reading, then the second byte sent on SPI_MOSI is ignored (except for CRC calculation).

If CRC is enabled, then the master must send as the third byte the 8-bit CRC code, which is calculated over first two bytes. If the CRC is correct, then the values clocked in will be put into the incoming buffer. If the CRC is not correct, then the outgoing buffer will be set to 0xFFFF, and the outgoing CRC will be set to 0xAA (these are clocked out on the next transaction).

During this transaction, the logic will clock out the contents of the outgoing buffer. If the outgoing buffer has not been updated since the last transaction, then the logic will clock out 0xFFFF, and if the CRC is clocked, it will clock out 0x00 for the CRC (if enabled). Thus the 0xFFFF00 will indicate to the master that the outgoing buffer was not updated by the internal logic before the transaction occurred. This can occur when the device did not have sufficient time to update the buffer between consecutive transactions.

When the internal logic takes the write-data from the interface logic and processes it, it also causes the R/W bit, address, and data to be copied into the outgoing buffer. On the next transaction, this data is clocked back to the master.

When the master is initiating a read, the internal logic will put the R/W bit and address into the outgoing buffer, along with the data requested. The interface will compute the CRC on the two bytes in the outgoing buffer and clock that back to the master if CRC is enabled (with the exceptions associated with 0xFFFF as noted above). A diagram of three transaction sequences with and without CRC are shown below, assuming CPOL=0.

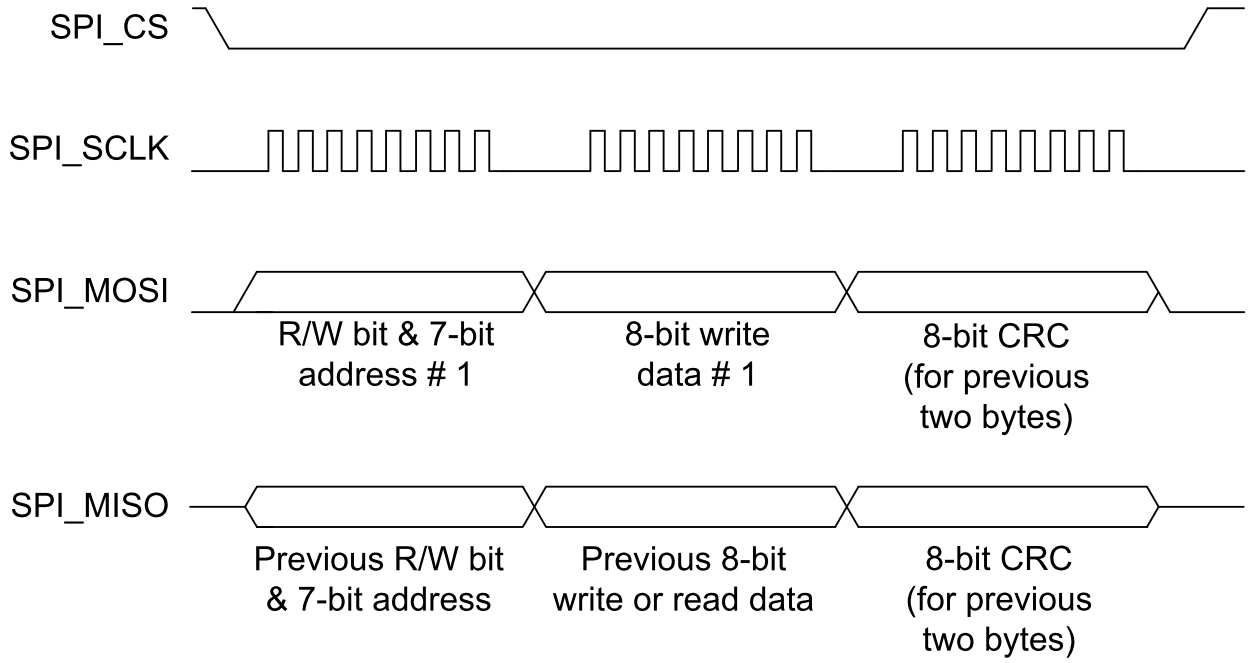


**Figure 14. SPI Transaction #1 using CRC**

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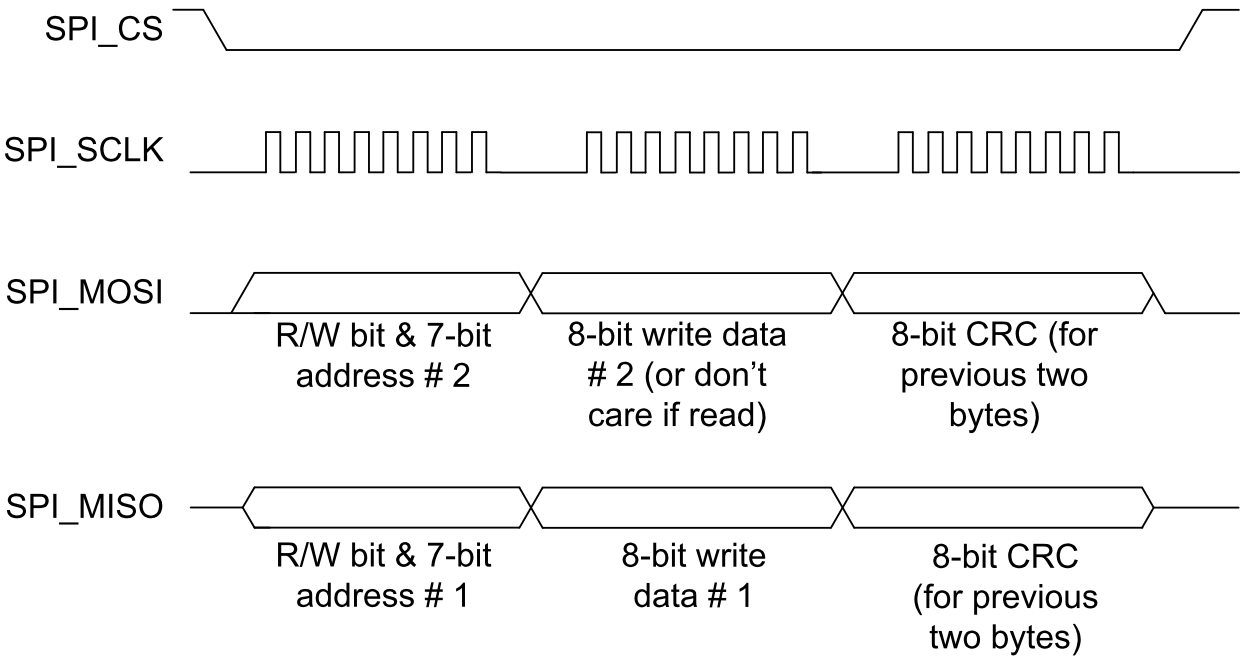


**Figure 15. SPI Transaction #2 using CRC**

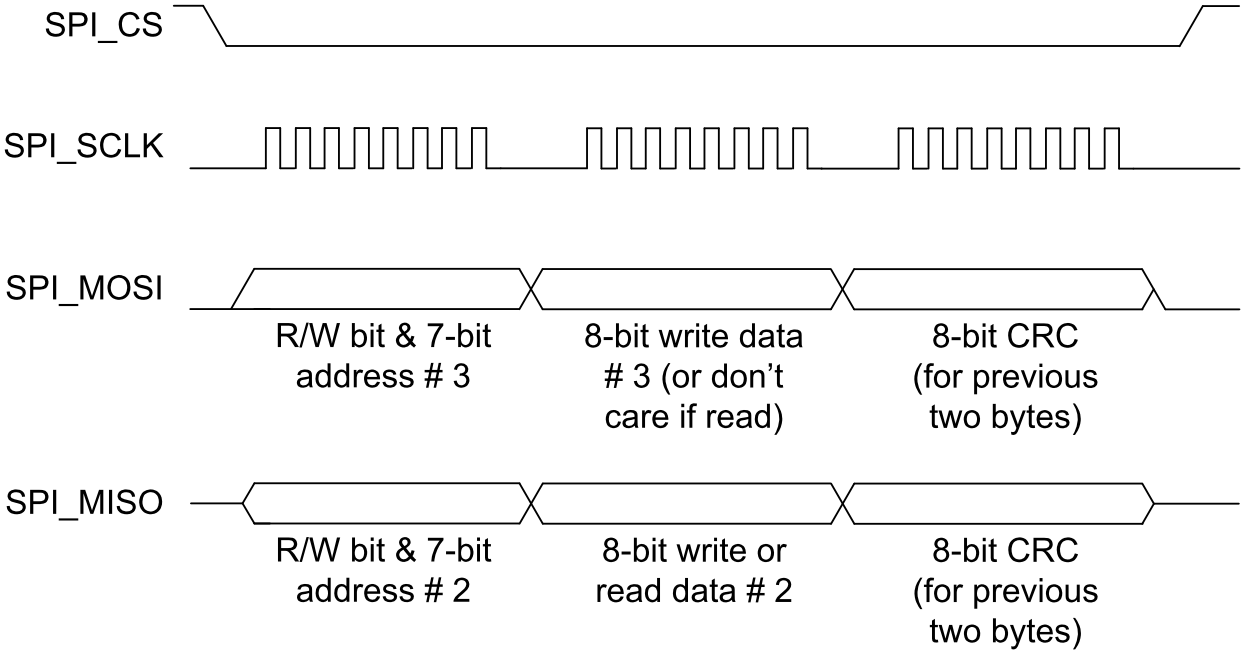


**Figure 16. SPI Transaction #3 using CRC**

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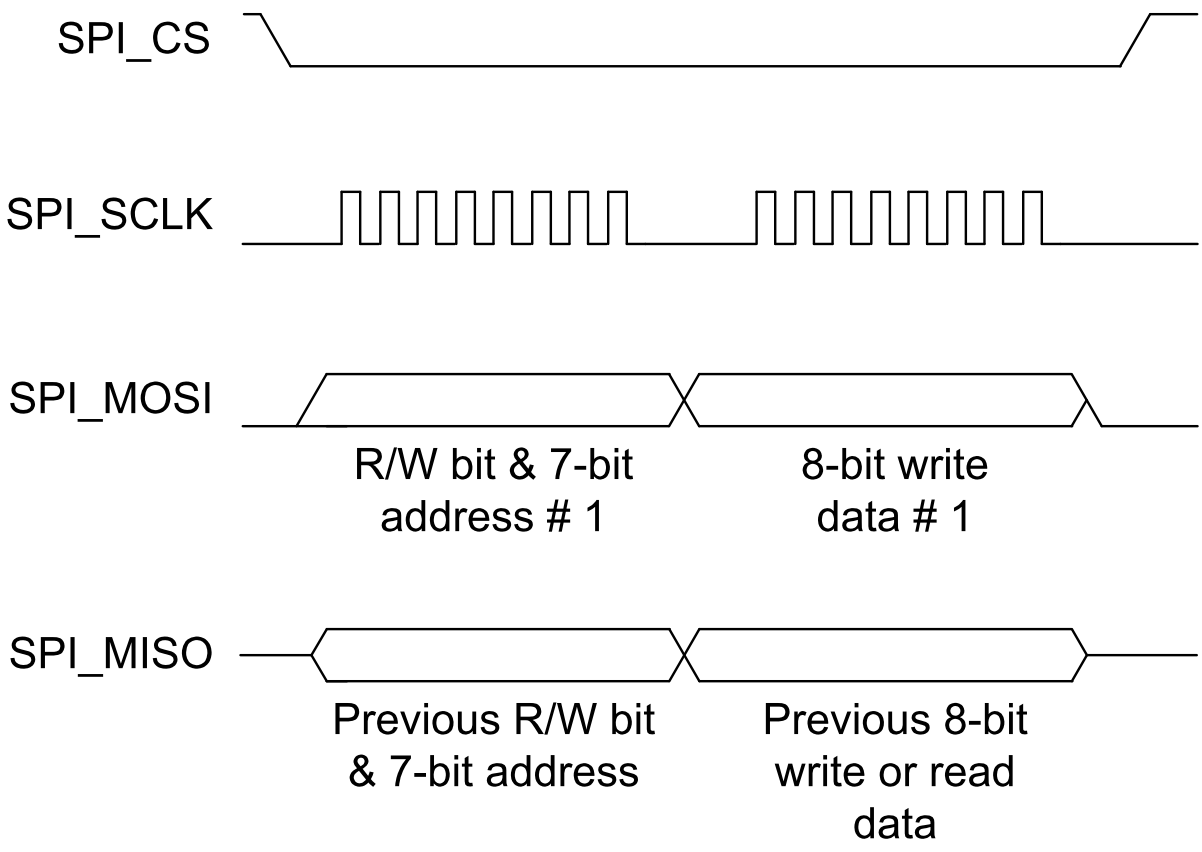


**Figure 17. SPI Transaction #1 without CRC**

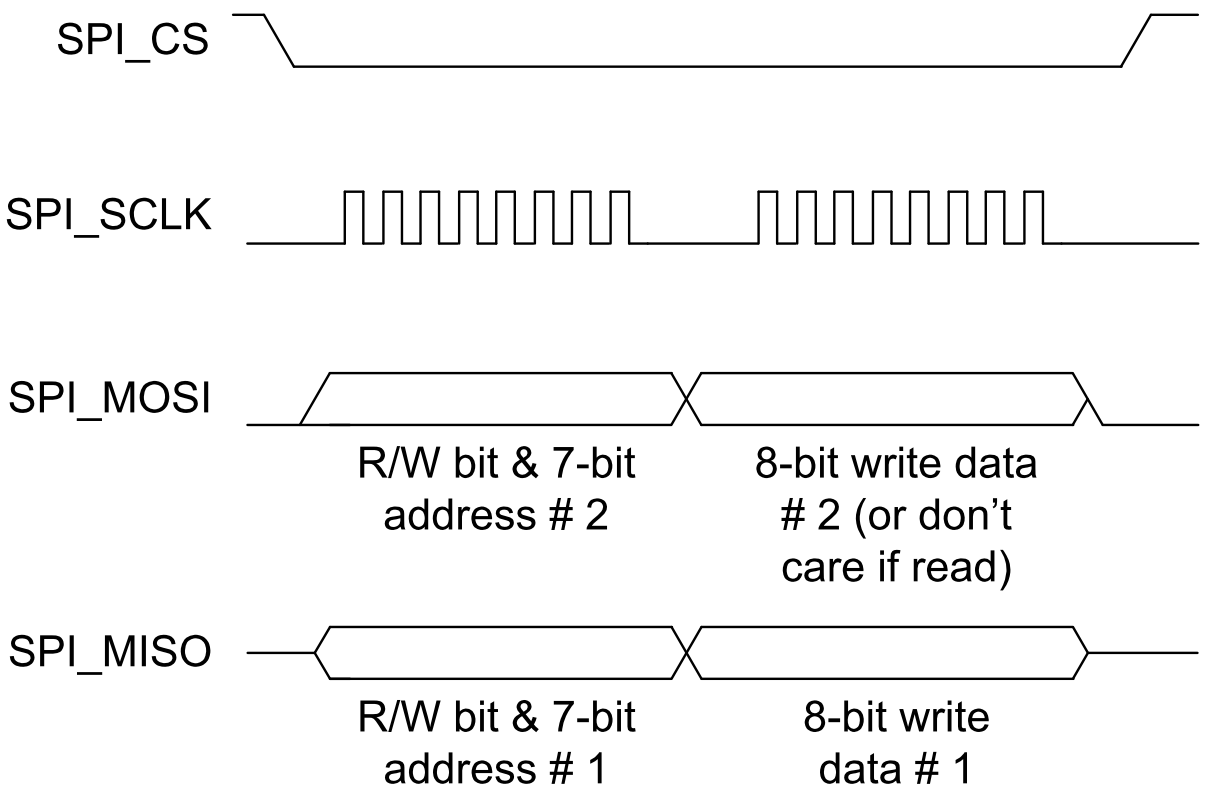


**Figure 18. SPI Transaction #2 without CRC**

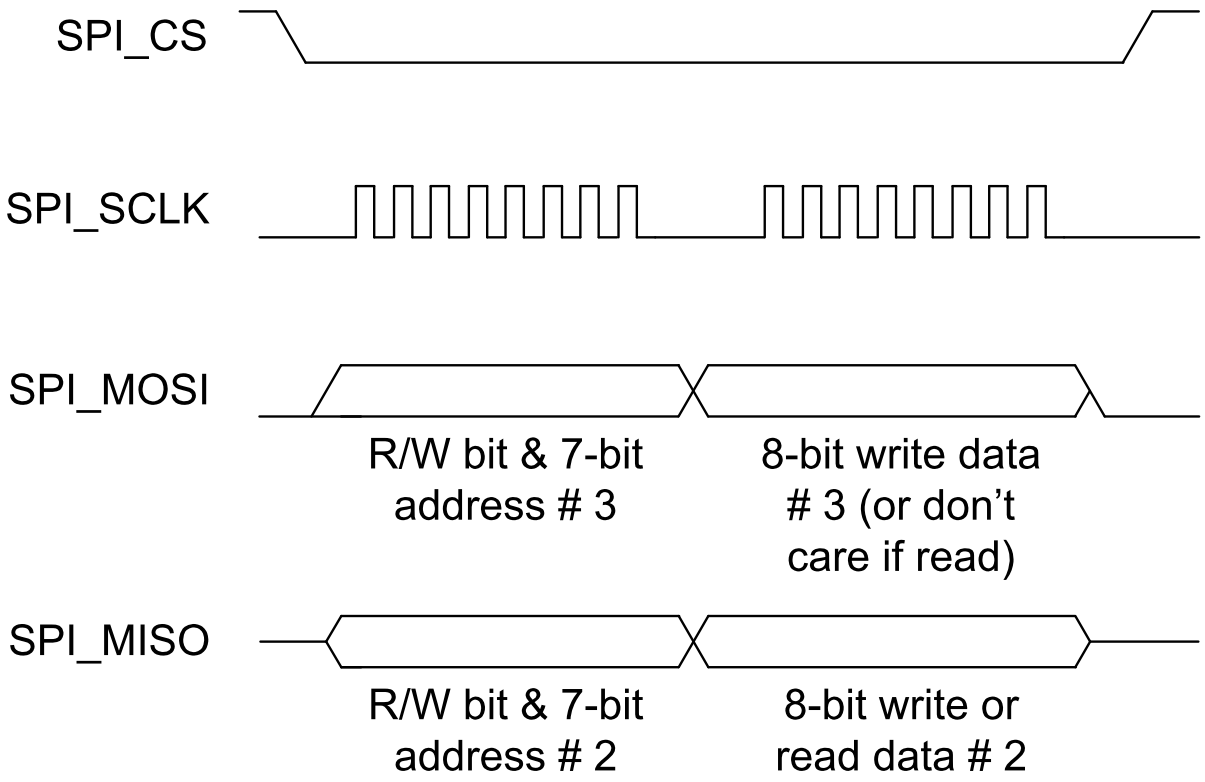


**Figure 19. SPI Transaction #3 without CRC**

Due to the delay in the HFO powering up if powered off, it is recommended to set the ***Settings:Configuration:Comm Idle Time*** to a level of 1 second or higher, which causes the HFO to stay powered for a programmable number of seconds after it is wakened by a falling edge on SPI_CS. The host can set this to a longer time (up to 255 seconds) and maintain regular communications within this window, causing the HFO to stay powered, so the device can respond quickly to SPI transactions. However, keeping the HFO running continuously will cause the device to consume additional supply current (≈30µA) beyond what it would consume if the HFO were only powered when needed. In order to avoid this extra supply current, the host can send an initial, unnecessary SPI transaction (such as reading command *CONTROL_STATUS()*) to cause the HFO to waken, and continue this until a valid response is returned on SPI_MISO. At this point, the host can begin sending the intended SPI transactions. Afterward, the host can send 0xAA to the *0x7F FET_OPTIONS()* command, which will cause the HFO to turn off.

#### *7.3.24.3 HDQ Communications Interface*

The HDQ interface is an asynchronous return-to-one protocol where a processor communicates with the BQ76942 device using a single-wire connection to the ALERT pin (which must be configured for use as the HDQ interface). Both the master (host device) and slave (BQ76942) drive the HDQ interface using an open-drain driver, with a pull-up resistor from the HDQ interface to a supply voltage required on the circuit board. The BQ76942 device can be changed from the default $I^2C$ communication mode to HDQ communication mode by setting the ***Settings:Configuration:Comm Type*** configuration register, or sending the *0x7C40 SWAP_TO_HDQ()* subcommand (at which point the device switches to HDQ mode immediately).

With HDQ, the least significant bit (LSB) of a data byte (command) or word (data) is transmitted first.

The 8-bit command code consists of two fields: the 7-bit HDQ command code (bits 0–6) and the 1-bit R/W field (MSB Bit 7). The R/W field directs the device to do one of the following:

- Accept the next 8 bits as data from the host to the device, or

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- Output 8 bits of data from the device to the host in response to the 7-bit command.

The HDQ peripheral on the BQ76952 device can transmit and receive data as an HDQ slave only.

The return-to-one data bit frame of HDQ consists of the following sections:

1. The first section is used to start the transmission by the host sending a Break (the host drives the HDQ interface to a logic-low state for a time $t_{(B)}$) followed by a Break Recovery (the host releases the HDQ interface for a time $t_{(BR)}$).
2. The next section is for host command transmission, where the host transmits 8 bits by driving the HDQ interface for 8 $T_{(CYCH)}$ time slots. For each time slot, the HDQ line is driven low for a time $T_{(HW0)}$ (host writing a "0") or $T_{(HW1)}$ (host writing a "1"). The HDQ pin is then released and remains high to complete each $T_{(CYCH)}$ time slot.
3. The next section is for data transmission where the host (if a write was initiated) or device (if a read was initiated) transmits 8 bits by driving the HDQ interface for 8 $T_{(CYCH)}$ (if host is driving) or $T_{(CYCD)}$ (if device is driving) time slots. The HDQ line is driven low for a time $T_{(HW0)}$ (host writing a "0"), $T_{(HW1)}$ (host writing a "1"), $T_{(DW0)}$ (device writing a "0"), or $T_{(DW1)}$ (device writing a "1"). The HDQ pin is then released and remains high to complete the time slot. The HDQ interface does not auto-increment, so a separate transaction must be sent for each byte to be transferred.

## 7.4 Data Formats

### 7.4.1 Unsigned Integer

Unsigned integers are stored without changes as 1-byte, 2-byte, or 4-byte values in little endian byte order.

| 0 |
|---|
| U1<br>MSB |

| 0 | 1 |
|---|---|
| U2<br>LSB | U2<br>MSB |

| 0 | 1 | 2 | 3 |
|---|---|---|---|
| U4 L<br>LSB | U4 L<br>MSB | U4 H<br>LSB | U4 H<br>MSB |

### 7.4.2 Integer

Integer values are stored in 2's-complement format in 1-byte, 2-byte, or 4-byte values in little endian byte order.

| 0 |
|---|
| I1<br>MSB |

| 0 | 1 |
|---|---|
| I2<br>LSB | I2<br>MSB |

| 0 | 1 | 2 | 3 |
|---|---|---|---|
| I4 L<br>LSB | I4 L<br>MSB | I4 H<br>LSB | I4 H<br>MSB |

### 7.4.3 Floating Point

Floating point values are stored using the IEEE754 Single Precision 4-byte format in little endian byte order.

| 0 | 1 | 2 | 3 |
|---|---|---|---|
| Fract [0–7] | Fract [8–15] | Exp[0] +<br>Fract[16–22] | Sign + Exp[1–7] |

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Where:

Exp: 8-bit exponent stored with an offset bias of 127. The values 00 and FF have unique meanings.

Fract: 23-bit fraction. If the exponent is > 0, then the mantissa is 1.fract. If the exponent is zero, then the mantissa is 0.fract.

The floating point value depends on the unique cases of the exponent:

- If the exponent is FF and the fraction is zero, this represents ± infinity.
- If the exponent is FF and the fraction is non-zero this represents "not a number" (NaN).
- If the exponent is 00 then the value is a subnormal number represented by $(–1)^{sign} \times 2^{–126} \times 0.fraction$.
- Otherwise, the value is a normalized number represented by $(–1)^{sign} \times 2^{(exponent – 127)} \times 1.fraction$.

### 7.4.4 Hex

Bit register definitions are stored in unsigned integer format.

## 7.5 Commands and Subcommands

The commands and subcommands supported by the BQ76942 device are described below, with direct commands listed in Table 38, subcommands that involve data listed in Table 39, and command-only subcommands listed in Table 40.

**Table 38. Direct Commands Table**

| Command | Name | Units | Type | Access | Description |
|---|---|---|---|---|---|
| 0x00 | Control Status | Hex | H2 | Sealed: R/W<br>Unsealed: R/W<br>Full Access: R/W | When read, this command provides device status bits. This command behaves similarly to 0x3E and 0x3F when written. When read back immediately after word write, it will return 0xFFA5 once. Subsequent reads will return Control Status. Writing this command is used for legacy auto-detection, and it is not recommended for customers to write to it.<br>Bit descriptions can be found in *Control Status(): 0x00* . |
| 0x02 | Safety Alert A | Hex | H1 | Sealed: R<br>Unsealed: R<br>Full Access: R | Provides individual alert signals when enabled safety alerts have triggered.<br>Bit descriptions can be found in *Safety Alert A(): 0x02* . |
| 0x03 | Safety Status A | Hex | H1 | Sealed: R<br>Unsealed: R<br>Full Access: R | Provides individual fault signals when enabled safety faults have triggered.<br>Bit descriptions can be found in *Safety Status A(): 0x03* . |
| 0x04 | Safety Alert B | Hex | H1 | Sealed: R<br>Unsealed: R<br>Full Access: R | Provides individual alert signals when enabled safety alerts have triggered.<br>Bit descriptions can be found in *Safety Alert B(): 0x04* . |
| 0x05 | Safety Status B | Hex | H1 | Sealed: R<br>Unsealed: R<br>Full Access: R | Provides individual fault signals when enabled safety faults have triggered.<br>Bit descriptions can be found in *Safety Status B(): 0x05* . |
| 0x06 | Safety Alert C | Hex | H1 | Sealed: R<br>Unsealed: R<br>Full Access: R | Provides individual alert signals when enabled safety alerts have triggered.<br>Bit descriptions can be found in *Safety Alert C(): 0x06* . |
| 0x07 | Safety Status C | Hex | H1 | Sealed: R<br>Unsealed: R<br>Full Access: R | Provides individual fault signals when enabled safety faults have triggered.<br>Bit descriptions can be found in *Safety Status C(): 0x07* . |
| 0x0A | PF Alert A | Hex | H1 | Sealed: R<br>Unsealed: R<br>Full Access: R | Provides individual alert signals when enabled Permanent Fail alerts have triggered.<br>Bit descriptions can be found in *PF Alert A(): 0x0A* . |
| 0x0B | PF Status A | Hex | H1 | Sealed: R<br>Unsealed: R<br>Full Access: R | Provides individual fault signals when enabled Permanent Fail faults have triggered.<br>Bit descriptions can be found in *PF Status A(): 0x0B* . |
| 0x0C | PF Alert B | Hex | H1 | Sealed: R<br>Unsealed: R<br>Full Access: R | Provides individual alert signals when enabled Permanent Fail alerts have triggered.<br>Bit descriptions can be found in *PF Alert B(): 0x0C* . |
| 0x0D | PF Status B | Hex | H1 | Sealed: R<br>Unsealed: R<br>Full Access: R | Provides individual fault signals when enabled Permanent Fail faults have triggered.<br>Bit descriptions can be found in *PF Status B(): 0x0D* . |
| 0x0E | PF Alert C | Hex | H1 | Sealed: R<br>Unsealed: R<br>Full Access: R | Provides individual alert signals when enabled Permanent Fail alerts have triggered.<br>Bit descriptions can be found in *PF Alert C(): 0x0E* . |

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## Commands and Subcommands (continued)

### Table 38. Direct Commands Table (continued)

| Command | Name | Units | Type | Access | Description |
|---|---|---|---|---|---|
| 0x0F | PF Status C | Hex | H1 | Sealed: R<br>Unsealed: R<br>Full Access: R | Provides individual fault signals when enabled Permanent Fail faults have triggered.<br>Bit descriptions can be found in *PF Status C(): 0x0F* . |
| 0x10 | PF Alert D | Hex | H1 | Sealed: R<br>Unsealed: R<br>Full Access: R | Provides individual alert signals when enabled Permanent Fail alerts have triggered.<br>Bit descriptions can be found in *PF Alert D(): 0x10* . |
| 0x11 | PF Status D | Hex | H1 | Sealed: R<br>Unsealed: R<br>Full Access: R | Provides individual fault signals when enabled Permanent Fail faults have triggered.<br>Bit descriptions can be found in *PF Status D(): 0x11* . |
| 0x12 | Battery Status | Hex | H2 | Sealed: R<br>Unsealed: R<br>Full Access: R | Flags related to battery status<br>Bit descriptions can be found in *Battery Status(): 0x12* . |
| 0x14 | Cell 1 Voltage | mV | I2 | Sealed: R<br>Unsealed: R<br>Full Access: R | 16-bit voltage on cell 1 |
| 0x16 | Cell 2 Voltage | mV | I2 | Sealed: R<br>Unsealed: R<br>Full Access: R | 16-bit voltage on cell 2 |
| 0x18 | Cell 3 Voltage | mV | I2 | Sealed: R<br>Unsealed: R<br>Full Access: R | 16-bit voltage on cell 3 |
| 0x1A | Cell 4 Voltage | mV | I2 | Sealed: R<br>Unsealed: R<br>Full Access: R | 16-bit voltage on cell 4 |
| 0x1C | Cell 5 Voltage | mV | I2 | Sealed: R<br>Unsealed: R<br>Full Access: R | 16-bit voltage on cell 5 |
| 0x1E | Cell 6 Voltage | mV | I2 | Sealed: R<br>Unsealed: R<br>Full Access: R | 16-bit voltage on cell 6 |
| 0x20 | Cell 7 Voltage | mV | I2 | Sealed: R<br>Unsealed: R<br>Full Access: R | 16-bit voltage on cell 7 |
| 0x22 | Cell 8 Voltage | mV | I2 | Sealed: R<br>Unsealed: R<br>Full Access: R | 16-bit voltage on cell 8 |
| 0x24 | Cell 9 Voltage | mV | I2 | Sealed: R<br>Unsealed: R<br>Full Access: R | 16-bit voltage on cell 9 |
| 0x26 | Cell 10 Voltage | mV | I2 | Sealed: R<br>Unsealed: R<br>Full Access: R | 16-bit voltage on cell 10 |
| 0x34 | Stack Voltage | userV | I2 | Sealed: R<br>Unsealed: R<br>Full Access: R | 16-bit voltage on top of stack |
| 0x36 | PACK Pin Voltage | userV | I2 | Sealed: R<br>Unsealed: R<br>Full Access: R | 16-bit voltage on PACK pin |
| 0x38 | LD Pin Voltage | userV | I2 | Sealed: R<br>Unsealed: R<br>Full Access: R | 16-bit voltage on LD pin |
| 0x3A | CC2 Current | userA | I2 | Sealed: R<br>Unsealed: R<br>Full Access: R | 16-bit CC2 current |
| 0x62 | Alarm Status | Hex | H2 | Sealed: R/W<br>Unsealed: R/W<br>Full Access: R/W | Latched signal used to assert the ALERT pin. Write a bit high to clear the latch.<br>Bit descriptions can be found in *Alarm Status(): 0x62* . |
| 0x64 | Alarm Raw Status | Hex | H2 | Sealed: R<br>Unsealed: R<br>Full Access: R | Unlatched value of flags which can be selected to be latched (using *Alarm Enable()*) and used to assert the ALERT pin.<br>Bit descriptions can be found in *Alarm Raw Status(): 0x64* . |

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## Commands and Subcommands (continued)

### Table 38. Direct Commands Table (continued)

| Command | Name | Units | Type | Access | Description |
|---|---|---|---|---|---|
| 0x66 | Alarm Enable | Hex | H2 | Sealed: R/W<br>Unsealed: R/W<br>Full Access: R/W | Mask for *Alarm Status()*. Can be written to change during operation to change which alarm sources are enabled. The default value of this parameter is set by ***Settings:Alarm:Default Alarm Mask***.<br>Bit descriptions can be found in *Alarm Enable(): 0x66* . |
| 0x68 | Int Temperature | dK | I2 | Sealed: R<br>Unsealed: R<br>Full Access: R | This is the most recent measured internal die temperature. |
| 0x6A | CFETOFF Temperature | dK | I2 | Sealed: R<br>Unsealed: R<br>Full Access: R | When the CFETOFF pin is configured as a thermistor input, this reports its most recent temperature measurement. When configured as ADCIN, this instead reports the measured voltage at the CFETOFF pin in millivolts. |
| 0x6C | DFETOFF Temperature | dK | I2 | Sealed: R<br>Unsealed: R<br>Full Access: R | When the DFETOFF pin is configured as a thermistor input, this reports its most recent temperature measurement. When configured as ADCIN, this instead reports the measured voltage at the DFETOFF pin in millivolts. |
| 0x6E | ALERT Temperature | dK | I2 | Sealed: R<br>Unsealed: R<br>Full Access: R | When the ALERT pin is configured as a thermistor input, this reports its most recent temperature measurement. When configured as ADCIN, this instead reports the measured voltage at the ALERT pin in millivolts. |
| 0x70 | TS1 Temperature | dK | I2 | Sealed: R<br>Unsealed: R<br>Full Access: R | When the TS1 pin is configured as a thermistor input, this reports its most recent temperature measurement. When configured as ADCIN, this instead reports the measured voltage at the TS1 pin in millivolts. |
| 0x72 | TS2 Temperature | dK | I2 | Sealed: R<br>Unsealed: R<br>Full Access: R | When the TS2 pin is configured as a thermistor input, this reports its most recent temperature measurement. When configured as ADCIN, this instead reports the measured voltage at the TS2 pin in millivolts. |
| 0x74 | TS3 Temperature | dK | I2 | Sealed: R<br>Unsealed: R<br>Full Access: R | When the TS3 pin is configured as a thermistor input, this reports its most recent temperature measurement. When configured as ADCIN, this instead reports the measured voltage at the TS3 pin in millivolts. |
| 0x76 | HDQ Temperature | dK | I2 | Sealed: R<br>Unsealed: R<br>Full Access: R | When the HDQ pin is configured as a thermistor input, this reports its most recent temperature measurement. When configured as ADCIN, this instead reports the measured voltage at the HDQ pin in millivolts. |
| 0x78 | DCHG Temperature | dK | I2 | Sealed: R<br>Unsealed: R<br>Full Access: R | When the DCHG pin is configured as a thermistor input, this reports its most recent temperature measurement. When configured as ADCIN, this instead reports the measured voltage at the DCHG pin in millivolts. |
| 0x7A | DDSG Temperature | dK | I2 | Sealed: R<br>Unsealed: R<br>Full Access: R | When the DDSG pin is configured as a thermistor input, this reports its most recent temperature measurement. When configured as ADCIN, this instead reports the measured voltage at the DDSG pin in millivolts. |
| 0x7F | FET Status | Hex | H1 | Sealed: R<br>Unsealed: R<br>Full Access: R | Provides flags showing status of FETs and ALERT pin.<br>Bit descriptions can be found in *FET Status(): 0x7F* . |

The subcommands supported in the device are listed below.

### Table 39. Subcommands Table

| Command | Name | Access | Offset | Data | Units | Type | Description |
|---|---|---|---|---|---|---|---|
| 0x0001 | DEVICE_NUMBER | Sealed: R<br>Unsealed: R<br>Full Access: R | 0 | Device Number | Hex | U2 | Reports the device number that identifies the product. The data is returned in little-endian format. |
| 0x0002 | FW_VERSION | Sealed: R<br>Unsealed: R<br>Full Access: R | 0 | Device Number (Big-Endian) | Hex | U2 | Device number in big-endian format for compatibility with legacy products |
| | | | 2 | Firmware Version (Big-Endian) | Hex | U2 | Device firmware major and minor version number (Big-Endian) |
| | | | 4 | Build Number (Big-Endian) | Hex | U2 | Firmware build number in big-endian, binary-coded decimal format for compatibility with legacy products |
| 0x0003 | HW_VERSION | Sealed: R<br>Unsealed: R<br>Full Access: R | 0 | Hardware Version | Hex | U2 | Reports the device hardware version number. |
| 0x0004 | IROM_SIG | Sealed: R<br>Unsealed: R<br>Full Access: R | 0 | Instruction ROM Signature | Hex | U2 | Calculates and reports the device instruction ROM signature. |
| 0x0005 | STATIC_CFG_SIG | Sealed: R<br>Unsealed: R<br>Full Access: R | 0 | Static Configuration Signature | Hex | U2 | The lower 15-bits report the signature of static (non-calibration) configuration data memory. If this does not match the stored ***System Data:Integrity:Config RAM Signature***, the MSBit is set. |

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**Table 39. Subcommands Table (continued)**

| Command | Name | Access | Offset | Data | Units | Type | Description |
|---|---|---|---|---|---|---|---|
| 0x0007 | PREV_MACWRITE | Sealed: R<br>Unsealed: R<br>Full Access: R | 0 | Previous Mac Write | Hex | U2 | Reports the previously written MAC command. This is primarily for use by TI software tools to restore any data after performing background operations. |
| 0x0009 | DROM_SIG | Sealed: R<br>Unsealed: R<br>Full Access: R | 0 | Data ROM Signature | Hex | U2 | Calculates and reports the device data ROM signature. |
| 0x0035 | SECURITY_KEYS | Sealed: —<br>Unsealed: —<br>Full Access: R/W | 0 | Unseal Key Step 1 | Hex | U2 | This is the first word of the security key that must be sent to transition from SEALED to UNSEALED mode. |
| | | | 2 | Unseal Key Step 2 | Hex | U2 | This is the second word of the security key that must be sent to transition from SEALED to UNSEALED mode. It must be sent within 5 seconds of the first word of the key and with no other commands in between. |
| | | | 4 | Full Access Key Step 1 | Hex | U2 | This is the second word of the security key that must be sent to transition from UNSEALED to FULLACCESS mode. |
| | | | 6 | Full Access Key Step 2 | Hex | U2 | This is the second word of the security key that must be sent to transition from UNSEALED to FULLACCESS mode. It must be sent within 5 seconds of the first word of the key and with no other commands in between. |
| 0x0053 | PF_STATUS | Sealed: R<br>Unsealed: R<br>Full Access: R | 0 | PF Status A | Hex | U1 | Saved Permanent Failure Status A<br>Bit descriptions can be found in *0x0053 PF_STATUS[0]: PF Status A()* . |
| | | | 1 | PF Status B | Hex | U1 | Saved Permanent Failure Status B<br>Bit descriptions can be found in *0x0053 PF_STATUS[1]: PF Status B()* . |
| | | | 2 | PF Status C | Hex | U1 | Saved Permanent Failure Status D<br>Bit descriptions can be found in *0x0053 PF_STATUS[2]: PF Status C()* . |
| | | | 3 | PF Status D | Hex | U1 | Saved Permanent Failure Status D<br>Bit descriptions can be found in *0x0053 PF_STATUS[3]: PF Status D()* . |
| | | | 4 | Fuse Flag | Hex | U1 | This is used to track whether or not the fuse has already been blown. This byte is normally zero but is set to 0x72 after the fuse is blown. |
| 0x0057 | MANUFACTURING STATUS | Sealed: R<br>Unsealed: R<br>Full Access: R | 0 | Manufacturing Status | Hex | H2 | Provides flags for use during manufacturing.<br>Bit descriptions can be found in *0x0057 MANUFACTURINGSTATUS[0–1]: Manufacturing Status()* . |

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**Table 39. Subcommands Table (continued)**

| Command | Name | Access | Offset | Data | Units | Type | Description |
|---|---|---|---|---|---|---|---|
| 0x0070 | MANU_DATA | Sealed: R<br>Unsealed: R<br>Full Access: R/W | 0 | Manufacturer Data 0 | Hex | U1 | Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write. |
| | | | 1 | Manufacturer Data 1 | Hex | U1 | Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write. |
| | | | 2 | Manufacturer Data 2 | Hex | U1 | Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write. |
| | | | 3 | Manufacturer Data 3 | Hex | U1 | Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write. |
| | | | 4 | Manufacturer Data 4 | Hex | U1 | Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write. |
| | | | 5 | Manufacturer Data 5 | Hex | U1 | Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write. |
| | | | 6 | Manufacturer Data 6 | Hex | U1 | Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write. |
| | | | 7 | Manufacturer Data 7 | Hex | U1 | Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write. |
| | | | 8 | Manufacturer Data 8 | Hex | U1 | Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write. |
| | | | 9 | Manufacturer Data 9 | Hex | U1 | Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write. |
| | | | 10 | Manufacturer Data 10 | Hex | U1 | Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write. |
| | | | 11 | Manufacturer Data 11 | Hex | U1 | Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write. |
| | | | 12 | Manufacturer Data 12 | Hex | U1 | Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write. |
| | | | 13 | Manufacturer Data 13 | Hex | U1 | Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write. |
| | | | 14 | Manufacturer Data 14 | Hex | U1 | Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write. |
| | | | 15 | Manufacturer Data 15 | Hex | U1 | Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write. |

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**Table 39. Subcommands Table (continued)**

| Command | Name | Access | Offset | Data | Units | Type | Description |
|---|---|---|---|---|---|---|---|
| 0x0070 | MANU_DATA | Sealed: R<br>Unsealed: R<br>Full Access: R/W | 16 | Manufacturer Data 16 | Hex | U1 | Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write. |
| | | | 17 | Manufacturer Data 17 | Hex | U1 | Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write. |
| | | | 18 | Manufacturer Data 18 | Hex | U1 | Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write. |
| | | | 19 | Manufacturer Data 19 | Hex | U1 | Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write. |
| | | | 20 | Manufacturer Data 20 | Hex | U1 | Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write. |
| | | | 21 | Manufacturer Data 21 | Hex | U1 | Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write. |
| | | | 22 | Manufacturer Data 22 | Hex | U1 | Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write. |
| | | | 23 | Manufacturer Data 23 | Hex | U1 | Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write. |
| | | | 24 | Manufacturer Data 24 | Hex | U1 | Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write. |
| | | | 25 | Manufacturer Data 25 | Hex | U1 | Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write. |
| | | | 26 | Manufacturer Data 26 | Hex | U1 | Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write. |
| | | | 27 | Manufacturer Data 27 | Hex | U1 | Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write. |
| | | | 28 | Manufacturer Data 28 | Hex | U1 | Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write. |
| | | | 29 | Manufacturer Data 29 | Hex | U1 | Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write. |
| | | | 30 | Manufacturer Data 30 | Hex | U1 | Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write. |
| | | | 31 | Manufacturer Data 31 | Hex | U1 | Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write. |
| 0x0071 | DASTATUS1 | Sealed: R<br>Unsealed: R<br>Full Access: R | 0 | Cell 1 Voltage Counts | — | I4 | 32-bit ADC counts for cell voltage measurement. |
| | | | 4 | Cell 1 Current Counts | — | I4 | 32-bit ADC counts for current measurement taken during the cell voltage measurement. |
| | | | 8 | Cell 2 Voltage Counts | — | I4 | 32-bit ADC counts for cell voltage measurement. |
| | | | 12 | Cell 2 Current Counts | — | I4 | 32-bit ADC counts for current measurement taken during the cell voltage measurement. |
| | | | 16 | Cell 3 Voltage Counts | — | I4 | 32-bit ADC counts for cell voltage measurement. |
| | | | 20 | Cell 3 Current Counts | — | I4 | 32-bit ADC counts for current measurement taken during the cell voltage measurement. |
| | | | 24 | Cell 4 Voltage Counts | — | I4 | 32-bit ADC counts for cell voltage measurement. |
| | | | 28 | Cell 4 Current Counts | — | I4 | 32-bit ADC counts for current measurement taken during the cell voltage measurement. |

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**Table 39. Subcommands Table (continued)**

| Command | Name | Access | Offset | Data | Units | Type | Description |
|---|---|---|---|---|---|---|---|
| 0x0072 | DASTATUS2 | Sealed: R<br>Unsealed: R<br>Full Access: R | 0 | Cell 5 Voltage Counts | — | I4 | 32-bit ADC counts for cell voltage measurement. |
| | | | 4 | Cell 5 Current Counts | — | I4 | 32-bit ADC counts for current measurement taken during the cell voltage measurement. |
| | | | 8 | Cell 6 Voltage Counts | — | I4 | 32-bit ADC counts for cell voltage measurement. |
| | | | 12 | Cell 6 Current Counts | — | I4 | 32-bit ADC counts for current measurement taken during the cell voltage measurement. |
| | | | 16 | Cell 7 Voltage Counts | — | I4 | 32-bit ADC counts for cell voltage measurement. |
| | | | 20 | Cell 7 Current Counts | — | I4 | 32-bit ADC counts for current measurement taken during the cell voltage measurement. |
| | | | 24 | Cell 8 Voltage Counts | — | I4 | 32-bit ADC counts for cell voltage measurement. |
| | | | 28 | Cell 8 Current Counts | — | I4 | 32-bit ADC counts for current measurement taken during the cell voltage measurement. |
| 0x0073 | DASTATUS3 | Sealed: R<br>Unsealed: R<br>Full Access: R | 0 | Cell 9 Voltage Counts | — | I4 | 32-bit ADC counts for cell voltage measurement. |
| | | | 4 | Cell 9 Current Counts | — | I4 | 32-bit ADC counts for current measurement taken during the cell voltage measurement. |
| | | | 8 | Cell 10 Voltage Counts | — | I4 | 32-bit ADC counts for cell voltage measurement. |
| | | | 12 | Cell 10 Current Counts | — | I4 | 32-bit ADC counts for current measurement taken during the cell voltage measurement. |
| 0x0075 | DASTATUS5 | Sealed: R<br>Unsealed: R<br>Full Access: R | 0 | Vref | — | I2 | 16-bit ADC count of the voltage reference used by the coulomb counter (VREF2). This is measured for diagnostic purposes. |
| | | | 2 | VSS | — | I2 | 16-bit ADC count of the VSS pin. This is measured for diagnostic purposes to ensure the ADC input mux is working properly. |
| | | | 4 | Max Cell Voltage | mV | I2 | Maximum Cell Voltage |
| | | | 6 | Min Cell Voltage | mV | I2 | Minimum Cell Voltage |
| | | | 8 | Battery Voltage Sum | userV | I2 | Sum of cell voltages (including interconnects). This can be compared to the *Stack Voltage()* for diagnostic purposes. Note, however, that these measurements are taken at different times which may cause variation. |
| | | | 10 | Cell Temperature | dK | I2 | Reports the cell temperature being used for features depending on a single temperature threshold. Note: features (such as protections) use minimum or maximum cell temperature instead. |
| | | | 12 | FET Temperature | dK | I2 | Reports the FET temperature given by the maximum of all measured FET temperatures. |
| | | | 14 | Max Cell Temperature | dK | I2 | Reports the maximum of all measured cell temperatures. |
| | | | 16 | Min Cell Temperature | dK | I2 | Reports the minimum of all measured cell temperatures. |
| | | | 18 | Avg Cell Temperature | dK | I2 | Reports the average of all measured cell temperatures. |
| | | | 20 | CC3 Current | userA | I2 | Reports the CC3 Current, which is obtained by averaging a configurable number of CC2 current measurements. |
| | | | 22 | CC1 Current | userA | I2 | Reports the CC1 current, which is updated every 250 ms in NORMAL mode. In SLEEP mode, this is updated every 4 seconds beginning one second after voltage measurements end. See the documentation on power modes for further details. |
| | | | 24 | CC2 Counts | — | I4 | Raw 32-bit count value for the latest CC2 measurement. |
| | | | 28 | CC3 Counts | — | I4 | Raw 32-bit count value for the latest CC3 measurement. |

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**Table 39. Subcommands Table (continued)**

| Command | Name | Access | Offset | Data | Units | Type | Description |
|---|---|---|---|---|---|---|---|
| 0x0076 | DASTATUS6 | Sealed: R<br>Unsealed: R<br>Full Access: R | 0 | Accum Charge | userAh | I4 | Reports the integer portion of accumulated passed charge in userAmp-hours. |
| | | | 4 | Accum Charge Fraction | — | U4 | Reports the fractional portion of accumulated passed charge. This is initialized to 0.5 userAh to facilitate appropriate rounding of the integer portion. |
| | | | 8 | Accum Time | s | U4 | Reports the number of seconds over which passed charge has been integrated. |
| | | | 12 | TS1 Counts | — | I4 | Reports the 32-bit ADC counts for the most recent measurement on the TS1 pin. |
| 0x0080 | CUV_SNAPSHOT | Sealed: R<br>Unsealed: R<br>Full Access: R | 0 | Cell 1 Voltage at CUV Event | mV | I2 | Records the cell voltage measurement made just after the latest CUV event. |
| | | | 2 | Cell 2 Voltage at CUV Event | mV | I2 | Records the cell voltage measurement made just after the latest CUV event. |
| | | | 4 | Cell 3 Voltage at CUV Event | mV | I2 | Records the cell voltage measurement made just after the latest CUV event. |
| | | | 6 | Cell 4 Voltage at CUV Event | mV | I2 | Records the cell voltage measurement made just after the latest CUV event. |
| | | | 8 | Cell 5 Voltage at CUV Event | mV | I2 | Records the cell voltage measurement made just after the latest CUV event. |
| | | | 10 | Cell 6 Voltage at CUV Event | mV | I2 | Records the cell voltage measurement made just after the latest CUV event. |
| | | | 12 | Cell 7 Voltage at CUV Event | mV | I2 | Records the cell voltage measurement made just after the latest CUV event. |
| | | | 14 | Cell 8 Voltage at CUV Event | mV | I2 | Records the cell voltage measurement made just after the latest CUV event. |
| | | | 16 | Cell 9 Voltage at CUV Event | mV | I2 | Records the cell voltage measurement made just after the latest CUV event. |
| | | | 18 | Cell 10 Voltage at CUV Event | mV | I2 | Records the cell voltage measurement made just after the latest CUV event. |
| 0x0081 | COV_SNAPSHOT | Sealed: R<br>Unsealed: R<br>Full Access: R | 0 | Cell 1 Voltage at COV Event | mV | I2 | Records the cell voltage measurement made just after the latest COV event. |
| | | | 2 | Cell 2 Voltage at COV Event | mV | I2 | Records the cell voltage measurement made just after the latest COV event. |
| | | | 4 | Cell 3 Voltage at COV Event | mV | I2 | Records the cell voltage measurement made just after the latest COV event. |
| | | | 6 | Cell 4 Voltage at COV Event | mV | I2 | Records the cell voltage measurement made just after the latest COV event. |
| | | | 8 | Cell 5 Voltage at COV Event | mV | I2 | Records the cell voltage measurement made just after the latest COV event. |
| | | | 10 | Cell 6 Voltage at COV Event | mV | I2 | Records the cell voltage measurement made just after the latest COV event. |
| | | | 12 | Cell 7 Voltage at COV Event | mV | I2 | Records the cell voltage measurement made just after the latest COV event. |
| | | | 14 | Cell 8 Voltage at COV Event | mV | I2 | Records the cell voltage measurement made just after the latest COV event. |
| | | | 16 | Cell 9 Voltage at COV Event | mV | I2 | Records the cell voltage measurement made just after the latest COV event. |
| | | | 18 | Cell 10 Voltage at COV Event | mV | I2 | Records the cell voltage measurement made just after the latest COV event. |
| 0x0083 | CB_ACTIVE_CELL | Sealed: R/W<br>Unsealed: R/W<br>Full Access: R/W | 0 | Cell Balancing Active Cell | — | U1 | When read, reports the actively balanced cell or 0xFF if balancing is disabled. When written, starts balancing on the specified cell. Write 0xFF to turn balancing off. |
| 0x0084 | CB_SET_LVL | Sealed: W<br>Unsealed: W<br>Full Access: W | 0 | Cell Balancing Set Level | mV | I2 | Start balancing the maximum-voltage cell if it is above the written voltage threshold. |
| 0x0085 | CBSTATUS1 | Sealed: R<br>Unsealed: R<br>Full Access: R | 0 | Cell Balancing Present Time | s | U2 | Reports the number of seconds that balancing has been continuously active. |

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**Table 39. Subcommands Table (continued)**

| Command | Name | Access | Offset | Data | Units | Type | Description |
|---|---|---|---|---|---|---|---|
| 0x0086 | CBSTATUS2 | Sealed: R<br>Unsealed: R<br>Full Access: R | 0 | Cell 1 Total Balancing Time | s | U4 | Reports the cumulative number of seconds that balancing has been active on this cell since the last device reset. |
| | | | 4 | Cell 2 Total Balancing Time | s | U4 | Reports the cumulative number of seconds that balancing has been active on this cell since the last device reset. |
| | | | 8 | Cell 3 Total Balancing Time | s | U4 | Reports the cumulative number of seconds that balancing has been active on this cell since the last device reset. |
| | | | 12 | Cell 4 Total Balancing Time | s | U4 | Reports the cumulative number of seconds that balancing has been active on this cell since the last device reset. |
| | | | 16 | Cell 5 Total Balancing Time | s | U4 | Reports the cumulative number of seconds that balancing has been active on this cell since the last device reset. |
| | | | 20 | Cell 6 Total Balancing Time | s | U4 | Reports the cumulative number of seconds that balancing has been active on this cell since the last device reset. |
| | | | 24 | Cell 7 Total Balancing Time | s | U4 | Reports the cumulative number of seconds that balancing has been active on this cell since the last device reset. |
| | | | 28 | Cell 8 Total Balancing Time | s | U4 | Reports the cumulative number of seconds that balancing has been active on this cell since the last device reset. |
| 0x0087 | CBSTATUS3 | Sealed: R<br>Unsealed: R<br>Full Access: R | 0 | Cell 9 Total Balancing Time | s | U4 | Reports the cumulative number of seconds that balancing has been active on this cell since the last device reset. |
| | | | 4 | Cell 10 Total Balancing Time | s | U4 | Reports the cumulative number of seconds that balancing has been active on this cell since the last device reset. |
| 0x0097 | FET_CONTROL | Sealed: W<br>Unsealed: W<br>Full Access: W | 0 | FET Control | Hex | H1 | Allows host control of individual FET drivers.<br>Bit descriptions can be found in *0x0097 FET_CONTROL[0]: FET Control()* . |
| 0x0098 | REG12_CONTROL | Sealed: W<br>Unsealed: W<br>Full Access: W | 0 | REG12 Control | Hex | H1 | Changes voltage regulator settings<br>Bit descriptions can be found in *0x0098 REG12_CONTROL[0]: REG12 Control()* . |
| 0x00a0 | OTP_WR_CHECK | Sealed: —<br>Unsealed: R<br>Full Access: R | 0 | OTP Write Check Result | Hex | H1 | Reports whether or not OTP programming is allowed.<br>Bit descriptions can be found in *0x00A0 OTP_WR_CHECK[0]: OTP Write Check Result()* . |
| | | | 1 | OTP Write Check Data Fail Addr | Hex | U2 | When data cannot be programmed to OTP because no XOR bits remain, this will contain the address of the first data value which could not be programmed. |
| 0x00a1 | OTP_WRITE | Sealed: —<br>Unsealed: R<br>Full Access: R | 0 | OTP Write Result | Hex | H1 | Reports whether or not OTP programming is allowed.<br>Bit descriptions can be found in *0x00A1 OTP_WRITE[0]: OTP Write Result()* . |
| | | | 1 | OTP Write Data Fail Addr | Hex | U2 | When data cannot be programmed to OTP because no XOR bits remain, this will contain the address of the first data value which could not be programmed. |
| 0xf081 | READ_CAL1 | Sealed: —<br>Unsealed: R<br>Full Access: R | 0 | Calibration Data Counter | — | I2 | Sample counter that is incremented when buffer is updated. Used to ensure unique measurement samples are taken when averaging is required. |
| | | | 2 | CC2 Counts | — | I4 | 32-bit CC2 Counts from the most recent current measurement. |
| | | | 6 | PACK pin ADC Counts | — | I2 | 16-bit ADC counts from previous PACK pin voltage measurement. |
| | | | 8 | Top of Stack ADC Counts | — | I2 | 16-bit ADC counts from previous Top of Stack voltage measurement. |
| | | | 10 | LD pin ADC Counts | — | I2 | 16-bit ADC counts from previous Top of Stack voltage measurement. |

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**Table 40. Command-only Subcommands Table**

| Command | Name | Access | Description |
|---|---|---|---|
| 0x000E | EXIT_DEEPSLEEP | Sealed: W<br>Unsealed: W<br>Full Access: W | Exit DEEPSLEEP mode. |
| 0x000F | DEEPSLEEP | Sealed: W<br>Unsealed: W<br>Full Access: W | Enter DEEPSLEEP mode. Must be sent twice in a row within 4s to take effect. |
| 0x0010 | SHUTDOWN | Sealed: W<br>Unsealed: W<br>Full Access: W | Start SHUTDOWN sequence. Must be sent twice in a row within 4s to take effect if sealed. If sent twice while unsealed, the shutdown delays are skipped. |
| 0x0012 | RESET | Sealed: —<br>Unsealed: W<br>Full Access: W | Resets the device. |
| 0x001C | PDSGTEST | Sealed: —<br>Unsealed: W<br>Full Access: W | In FET Test mode, toggle the PCHG FET enable. |
| 0x001D | FUSE_TOGGLE | Sealed: —<br>Unsealed: W<br>Full Access: W | Toggle FUSE state. |
| 0x001E | PCHGTEST | Sealed: —<br>Unsealed: W<br>Full Access: W | In FET Test mode, toggle the PCHG FET enable. |
| 0x001F | CHGTEST | Sealed: —<br>Unsealed: W<br>Full Access: W | In FET Test mode, toggle the CHG FET enable. |
| 0x0020 | DSGTEST | Sealed: —<br>Unsealed: W<br>Full Access: W | In FET Test mode, toggle the DSG FET enable. |
| 0x0022 | FET_ENABLE | Sealed: —<br>Unsealed: W<br>Full Access: W | Toggle FET_EN in Manufacturing Status. FET_EN = 0 means FET Test mode. FET_EN = 1 means Firmware FET Control. |
| 0x0024 | PF_ENABLE | Sealed: —<br>Unsealed: W<br>Full Access: W | Toggle PF_EN in Manufacturing Status. |
| 0x0029 | PF_RESET | Sealed: —<br>Unsealed: W<br>Full Access: W | Clear PF status. |
| 0x0030 | SEAL | Sealed: —<br>Unsealed: W<br>Full Access: W | Places the device in SEALED mode. |
| 0x0082 | RESET_PASSQ | Sealed: W<br>Unsealed: W<br>Full Access: W | Resets the integrated charge and timer. Charge resets to 0.5 userAh so that the integer portion is rounded. |
| 0x0090 | SET_CFGUPDATE | Sealed: —<br>Unsealed: W<br>Full Access: W | Enters CONFIG_UPDATE mode. |
| 0x0092 | EXIT_CFGUPDATE | Sealed: W<br>Unsealed: W<br>Full Access: W | Exits CONFIG_UPDATE mode. This also clears the *Battery Status()[POR]* and *Battery Status()[WD]* bits. |
| 0x0093 | DSG_PDSG_OFF | Sealed: W<br>Unsealed: W<br>Full Access: W | Disables DSG and PDSG FET drivers. |
| 0x0094 | CHG_PCHG_OFF | Sealed: W<br>Unsealed: W<br>Full Access: W | Disables CHG and PCHG FET drivers. |
| 0x0095 | ALL_FETS_OFF | Sealed: W<br>Unsealed: W<br>Full Access: W | Disables CHG, DSG, PCHG, and PDSG FET drivers. |
| 0x0096 | ALL_FETS_ON | Sealed: W<br>Unsealed: W<br>Full Access: W | Allows all four FETs to be on if other safety conditions are met. This clears the states set by the DSG_PDSG_OFF, CHG_PCHG_OFF, and ALL_FETS_OFF commands. |
| 0x0099 | SLEEP_ENABLE | Sealed: W<br>Unsealed: W<br>Full Access: W | Enable SLEEP mode. The default is loaded from data memory, after which this command can change the setting. |
| 0x009A | SLEEP_DISABLE | Sealed: W<br>Unsealed: W<br>Full Access: W | Disable SLEEP mode. The default is loaded from data memory, after which this command can change the setting. |

**Table 40. Command-only Subcommands Table (continued)**

| Command | Name | Access | Description |
|---|---|---|---|
| 0x009B | OCDL_RECOVER | Sealed: W<br>Unsealed: W<br>Full Access: W | Recovers Overcurrent in Discharge Latch (OCDL) in the next execution of the safety engine (≈1 second). |
| 0x009C | SCDL_RECOVER | Sealed: W<br>Unsealed: W<br>Full Access: W | Recovers Short Circuit in Discharge Latch (SCDL) in the next execution of the safety engine (≈1 second). |
| 0x009D | LOAD_DETECT_RESTART | Sealed: W<br>Unsealed: W<br>Full Access: W | Restarts the timeout on the Load Detect (LD) pin current source if it has already triggered. |
| 0x009E | LOAD_DETECT_ON | Sealed: W<br>Unsealed: W<br>Full Access: W | Force the Load Detect (LD) pin current source to be ON. This command has no effect when the device is configured for autonomous control of the current source (***Protections:Load Detect:Active Time*** > 0). |
| 0x009F | LOAD_DETECT_OFF | Sealed: W<br>Unsealed: W<br>Full Access: W | Force the Load Detect (LD) pin current source to be OFF. This command has no effect when the device is configured for autonomous control of the current source (***Protections:Load Detect:Active Time*** > 0). |
| 0x2800 | CFETOFF_LO | Sealed: W<br>Unsealed: W<br>Full Access: W | Drive the CFETOFF pin to a low state if it is configured as a GPO. |
| 0x2801 | DFETOFF_LO | Sealed: W<br>Unsealed: W<br>Full Access: W | Drive the DFETOFF pin to a low state if it is configured as a GPO. |
| 0x2802 | ALERT_LO | Sealed: W<br>Unsealed: W<br>Full Access: W | Drive the ALERT pin to a low state if it is configured as a GPO. |
| 0x2806 | HDQ_LO | Sealed: W<br>Unsealed: W<br>Full Access: W | Drive the HDQ pin to a low state if it is configured as a GPO. |
| 0x2807 | DCHG_LO | Sealed: W<br>Unsealed: W<br>Full Access: W | Drive the DCHG pin to a low state if it is configured as a GPO. |
| 0x2808 | DDSG_LO | Sealed: W<br>Unsealed: W<br>Full Access: W | Drive the DDSG pin to a low state if it is configured as a GPO. |
| 0x2810 | CFETOFF_HI | Sealed: W<br>Unsealed: W<br>Full Access: W | Drive the CFETOFF pin to a high state if it is configured as a GPO. |
| 0x2811 | DFETOFF_HI | Sealed: W<br>Unsealed: W<br>Full Access: W | Drive the DFETOFF pin to a high state if it is configured as a GPO. |
| 0x2812 | ALERT_HI | Sealed: W<br>Unsealed: W<br>Full Access: W | Drive the ALERT pin to a high state if it is configured as a GPO. |
| 0x2816 | HDQ_HI | Sealed: W<br>Unsealed: W<br>Full Access: W | Drive the HDQ pin to a high state if it is configured as a GPO. |
| 0x2817 | DCHG_HI | Sealed: W<br>Unsealed: W<br>Full Access: W | Drive the DCHG pin to a high state if it is configured as a GPO. |
| 0x2818 | DDSG_HI | Sealed: W<br>Unsealed: W<br>Full Access: W | Drive the DDSG pin to a high state if it is configured as a GPO. |
| 0x2857 | PF_FORCE_A | Sealed: W<br>Unsealed: W<br>Full Access: W | First part of two-word command to force the command-based PF. Must be followed by PF_FORCE_B within 4s with no writes in between. |
| 0x29A3 | PF_FORCE_B | Sealed: W<br>Unsealed: W<br>Full Access: W | Second part of two-word command to force the command-based PF. Must be preceded by PF_FORCE_A within 4s with no writes in between. |
| 0x29BC | SWAP_COMM_MODE | Sealed: —<br>Unsealed: W<br>Full Access: W | Change to the communications mode previously configured in CONFIG_UPDATE_MODE. |
| 0x29E7 | SWAP_TO_I2C | Sealed: —<br>Unsealed: W<br>Full Access: W | Select $I^2C$ mode in data memory and immediately start using $I^2C$. |
| 0x7C35 | SWAP_TO_SPI | Sealed: —<br>Unsealed: W<br>Full Access: W | Select SPI mode in data memory and immediately start using SPI. |

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**Table 40. Command-only Subcommands Table (continued)**

| Command | Name | Access | Description |
|---|---|---|---|
| 0x7C40 | SWAP_TO_HDQ | Sealed: —<br>Unsealed: W<br>Full Access: W | Select HDQ mode in data memory and immediately start using HDQ. |

### 7.5.1 Bitfield Definitions for Direct Commands

#### *7.5.1.1 Control Status(): 0x00*

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | DEEPSLEEP | LD_TIMEOUT | LD_ON |

**Description**: When read, this command provides device status bits. This command behaves similarly to 0x3E and 0x3F when written. When read back immediately after word write, it will return 0xFFA5 once. Subsequent reads will return Control Status. Writing this command is used for legacy auto-detection, and it is not recommended for customers to write to it.

**Table 41. Control Status Register Field Descriptions**

| Bit | Field | Description |
|---|---|---|
| 2 | DEEPSLEEP | This bit indicates whether or not the device is in DEEPSLEEP mode.<br>0 = Device is in DEEPSLEEP mode.<br>1 = Device is not in DEEPSLEEP mode. |
| 1 | LD_TIMEOUT | This bit is set when the Load Detect function has timed out and checking has stopped.<br>0 = Load Detect function has not timed out or is inactive.<br>1 = Load Detection function timed out and was deactivated. |
| 0 | LD_ON | This bit indicates whether or not the Load Detect pullup was active during the previous LD pin voltage measurement.<br>0 = LD pullup was not active during the previous LD pin measurement.<br>1 = LD pullup was active during the previous LD pin measurement. |

#### *7.5.1.2 Safety Alert A(): 0x02*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SCD | OCD2 | OCD1 | OCC | COV | CUV | RSVD_0 | RSVD_0 |

**Description**: Provides individual alert signals when enabled safety alerts have triggered.

**Table 42. Safety Alert A Register Field Descriptions**

| Bit | Field | Description |
|---|---|---|
| 7 | SCD | Short Circuit in Discharge Protection<br>0 = Alert is not triggered.<br>1 = Alert is triggered. |
| 6 | OCD2 | Overcurrent in Discharge 2nd Tier Protection<br>0 = Alert is not triggered.<br>1 = Alert is triggered. |
| 5 | OCD1 | Overcurrent in Discharge 1st Tier Protection<br>0 = Alert is not triggered.<br>1 = Alert is triggered. |
| 4 | OCC | Overcurrent in Charge Protection<br>0 = Alert is not triggered.<br>1 = Alert is triggered. |

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**Table 42. Safety Alert A Register Field Descriptions (continued)**

| Bit | Field | Description |
|---|---|---|
| 3 | COV | Cell Overvoltage Protection<br>0 = Alert is not triggered.<br>1 = Alert is triggered. |
| 2 | CUV | Cell Undervoltage Protection<br>0 = Alert is not triggered.<br>1 = Alert is triggered. |

### *7.5.1.3 Safety Status A(): 0x03*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SCD | OCD2 | OCD1 | OCC | COV | CUV | RSVD_0 | RSVD_0 |

**Description**: Provides individual fault signals when enabled safety faults have triggered.

**Table 43. Safety Status A Register Field Descriptions**

| Bit | Field | Description |
|---|---|---|
| 7 | SCD | Short Circuit in Discharge Protection<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |
| 6 | OCD2 | Overcurrent in Discharge 2nd Tier Protection<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |
| 5 | OCD1 | Overcurrent in Discharge 1st Tier Protection<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |
| 4 | OCC | Overcurrent in Charge Protection<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |
| 3 | COV | Cell Overvoltage Protection<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |
| 2 | CUV | Cell Undervoltage Protection<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |

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### *7.5.1.4 Safety Alert B(): 0x04*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OTF | OTINT | OTD | OTC | RSVD_0 | UTINT | UTD | UTC |

**Description**: Provides individual alert signals when enabled safety alerts have triggered.

**Table 44. Safety Alert B Register Field Descriptions**

| Bit | Field | Description |
|---|---|---|
| 7 | OTF | FET Overtemperature<br>0 = Alert is not triggered.<br>1 = Alert is triggered. |
| 6 | OTINT | Internal Overtemperature<br>0 = Alert is not triggered.<br>1 = Alert is triggered. |

**Table 44. Safety Alert B Register Field Descriptions (continued)**

| Bit | Field | Description |
|---|---|---|
| 5 | OTD | Overtemperature in Discharge<br>0 = Alert is not triggered.<br>1 = Alert is triggered. |
| 4 | OTC | Overtemperature in Charge<br>0 = Alert is not triggered.<br>1 = Alert is triggered. |
| 2 | UTINT | Internal Undertemperature<br>0 = Alert is not triggered.<br>1 = Alert is triggered. |
| 1 | UTD | Undertemperature in Discharge<br>0 = Alert is not triggered.<br>1 = Alert is triggered. |
| 0 | UTC | Undertemperature in Charge<br>0 = Alert is not triggered.<br>1 = Alert is triggered. |

### 7.5.1.5 Safety Status B(): 0x05

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OTF | OTINT | OTD | OTC | RSVD_0 | UTINT | UTD | UTC |

**Description**: Provides individual fault signals when enabled safety faults have triggered.

**Table 45. Safety Status B Register Field Descriptions**

| Bit | Field | Description |
|---|---|---|
| 7 | OTF | FET Overtemperature<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |
| 6 | OTINT | Internal Overtemperature<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |
| 5 | OTD | Overtemperature in Discharge<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |
| 4 | OTC | Overtemperature in Charge<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |
| 2 | UTINT | Internal Undertemperature<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |
| 1 | UTD | Undertemperature in Discharge<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |
| 0 | UTC | Undertemperature in Charge<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |

### 7.5.1.6 Safety Alert C(): 0x06

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OCD3 | SCDL | OCDL | COVL | PTOS | RSVD_0 | RSVD_0 | RSVD_0 |

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**Description**: Provides individual alert signals when enabled safety alerts have triggered.

**Table 46. Safety Alert C Register Field Descriptions**

| Bit | Field | Description |
|---|---|---|
| 7 | OCD3 | Overcurrent in Discharge 3rd Tier Protection<br>0 = Alert is not triggered.<br>1 = Alert is triggered. |
| 6 | SCDL | Short Circuit in Discharge Latch<br>0 = Alert is not triggered.<br>1 = Alert is triggered. |
| 5 | OCDL | Overcurrent in Discharge Latch<br>0 = Alert is not triggered.<br>1 = Alert is triggered. |
| 4 | COVL | Cell Overvoltage Latch<br>0 = Alert is not triggered.<br>1 = Alert is triggered. |
| 3 | PTOS | Precharge Timeout Suspend<br>0 = Precharge timeout protection is not suspended.<br>1 = Precharge timeout protection is suspended. |

### 7.5.1.7 Safety Status C(): 0x07

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OCD3 | SCDL | OCDL | COVL | RSVD_0 | PTO | HWDF | RSVD_0 |

**Description**: Provides individual fault signals when enabled safety faults have triggered.

**Table 47. Safety Status C Register Field Descriptions**

| Bit | Field | Description |
|---|---|---|
| 7 | OCD3 | Overcurrent in Discharge 3rd Tier Protection<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |
| 6 | SCDL | Short Circuit in Discharge Latch<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |
| 5 | OCDL | Overcurrent in Discharge Latch<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |
| 4 | COVL | Cell Overvoltage Latch<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |
| 2 | PTO | Precharge Timeout<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |
| 1 | HWDF | Host Watchdog Fault<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |

### 7.5.1.8 PF Alert A(): 0x0A

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CUDEP | SOTF | RSVD_0 | SOT | SOCD | SOCC | SOV | SUV |

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**Description**: Provides individual alert signals when enabled Permanent Fail alerts have triggered.

**Table 48. PF Alert A Register Field Descriptions**

| Bit | Field | Description |
|---|---|---|
| 7 | CUDEP | Copper Deposition Permanent Fail<br>0 = Alert is not triggered.<br>1 = Alert is triggered. |
| 6 | SOTF | Safety Overtemperature FET Permanent Fail<br>0 = Alert is not triggered.<br>1 = Alert is triggered. |
| 4 | SOT | Safety Overtemperature Permanent Fail<br>0 = Alert is not triggered.<br>1 = Alert is triggered. |
| 3 | SOCD | Safety Overcurrent in Discharge Permanent Fail<br>0 = Alert is not triggered.<br>1 = Alert is triggered. |
| 2 | SOCC | Safety Overcurrent in Charge Permanent Fail<br>0 = Alert is not triggered.<br>1 = Alert is triggered. |
| 1 | SOV | Safety Cell Overvoltage Permanent Fail<br>0 = Alert is not triggered.<br>1 = Alert is triggered. |
| 0 | SUV | Safety Cell Undervoltage Permanent Fail<br>0 = Alert is not triggered.<br>1 = Alert is triggered. |

### *7.5.1.9 PF Status A(): 0x0B*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CUDEP | SOTF | RSVD_0 | SOT | SOCD | SOCC | SOV | SUV |

**Description**: Provides individual fault signals when enabled Permanent Fail faults have triggered.

**Table 49. PF Status A Register Field Descriptions**

| Bit | Field | Description |
|---|---|---|
| 7 | CUDEP | Copper Deposition Permanent Fail<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |
| 6 | SOTF | Safety Overtemperature FET Permanent Fail<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |
| 4 | SOT | Safety Overtemperature Permanent Fail<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |
| 3 | SOCD | Safety Overcurrent in Discharge Permanent Fail<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |
| 2 | SOCC | Safety Overcurrent in Charge Permanent Fail<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |
| 1 | SOV | Safety Cell Overvoltage Permanent Fail<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |

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**Table 49. PF Status A Register Field Descriptions (continued)**

| Bit | Field | Description |
|---|---|---|
| 0 | SUV | Safety Cell Undervoltage Permanent Fail<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |

### *7.5.1.10 PF Alert B(): 0x0C*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SCDL | RSVD_0 | RSVD_0 | VIMA | VIMR | 2LVL | DFETF | CFETF |

**Description**: Provides individual alert signals when enabled Permanent Fail alerts have triggered.

**Table 50. PF Alert B Register Field Descriptions**

| Bit | Field | Description |
|---|---|---|
| 7 | SCDL | Short Circuit in Discharge Latch Permanent Fail<br>0 = Alert is not triggered.<br>1 = Alert is triggered. |
| 4 | VIMA | Voltage Imbalance Active Permanent Fail<br>0 = Alert is not triggered.<br>1 = Alert is triggered. |
| 3 | VIMR | Voltage Imbalance at Rest Permanent Fail<br>0 = Alert is not triggered.<br>1 = Alert is triggered. |
| 2 | 2LVL | Second Level Protector Permanent Fail<br>0 = Alert is not triggered.<br>1 = Alert is triggered. |
| 1 | DFETF | Discharge FET Permanent Fail<br>0 = Alert is not triggered.<br>1 = Alert is triggered. |
| 0 | CFETF | Charge FET Permanent Fail<br>0 = Alert is not triggered.<br>1 = Alert is triggered. |

### *7.5.1.11 PF Status B(): 0x0D*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SCDL | RSVD_0 | RSVD_0 | VIMA | VIMR | 2LVL | DFETF | CFETF |

**Description**: Provides individual fault signals when enabled Permanent Fail faults have triggered.

**Table 51. PF Status B Register Field Descriptions**

| Bit | Field | Description |
|---|---|---|
| 7 | SCDL | Short Circuit in Discharge Latch Permanent Fail<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |
| 4 | VIMA | Voltage Imbalance Active Permanent Fail<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |
| 3 | VIMR | Voltage Imbalance at Rest Permanent Fail<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |

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**Table 51. PF Status B Register Field Descriptions (continued)**

| Bit | Field | Description |
|---|---|---|
| 2 | 2LVL | Second Level Protector Permanent Fail<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |
| 1 | DFETF | Discharge FET Permanent Fail<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |
| 0 | CFETF | Charge FET Permanent Fail<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |

### *7.5.1.12 PF Alert C(): 0x0E*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RSVD_0 | HWMX | VSSF | VREF | LFOF | RSVD_0 | RSVD_0 | RSVD_0 |

**Description**: Provides individual alert signals when enabled Permanent Fail alerts have triggered.

**Table 52. PF Alert C Register Field Descriptions**

| Bit | Field | Description |
|---|---|---|
| 6 | HWMX | Hardware Mux Permanent Fail<br>0 = Alert is not triggered.<br>1 = Alert is triggered. |
| 5 | VSSF | Internal VSS Measurement Permanent Fail<br>0 = Alert is not triggered.<br>1 = Alert is triggered. |
| 4 | VREF | Internal Voltage Reference Permanent Fail<br>0 = Alert is not triggered.<br>1 = Alert is triggered. |
| 3 | LFOF | Internal LFO Permanent Fail<br>0 = Alert is not triggered.<br>1 = Alert is triggered. |

### *7.5.1.13 PF Status C(): 0x0F*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CMDF | HWMX | VSSF | VREF | LFOF | IRMF | DRMF | OTPF |

**Description**: Provides individual fault signals when enabled Permanent Fail faults have triggered.

**Table 53. PF Status C Register Field Descriptions**

| Bit | Field | Description |
|---|---|---|
| 7 | CMDF | Commanded Permanent Fail<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |
| 6 | HWMX | Hardware Mux Permanent Fail<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |
| 5 | VSSF | Internal VSS Measurement Permanent Fail<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |

**Table 53. PF Status C Register Field Descriptions (continued)**

| Bit | Field | Description |
|---|---|---|
| 4 | VREF | Internal Voltage Reference Permanent Fail<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |
| 3 | LFOF | Internal LFO Permanent Fail<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |
| 2 | IRMF | Instruction ROM Permanent Fail<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |
| 1 | DRMF | Data ROM Permanent Fail<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |
| 0 | OTPF | OTP Memory Permanent Fail<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |

### 7.5.1.14 PF Alert D(): 0x10

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | TOSF |

**Description**: Provides individual alert signals when enabled Permanent Fail alerts have triggered.

**Table 54. PF Alert D Register Field Descriptions**

| Bit | Field | Description |
|---|---|---|
| 0 | TOSF | Top of Stack versus Cell Sum Permanent Fail<br>0 = Alert is not triggered.<br>1 = Alert is triggered. |

### 7.5.1.15 PF Status D(): 0x11

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | TOSF |

**Description**: Provides individual fault signals when enabled Permanent Fail faults have triggered.

**Table 55. PF Status D Register Field Descriptions**

| Bit | Field | Description |
|---|---|---|
| 0 | TOSF | Top of Stack versus Cell Sum Permanent Fail<br>0 = Fault is not triggered.<br>1 = Fault is triggered. |

### 7.5.1.16 Battery Status(): 0x12

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| SLEEP | RSVD_0 | SD_CMD | PF | SS | FUSE | SEC1 | SEC0 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OTPB | OTPW | COW_CHK | WD | POR | SLEEP_EN | PCHG_MODE | CFGUPDATE |

ADVANCE INFORMATION

**Description**: Flags related to battery status

**Table 56. Battery Status Register Field Descriptions**

| Bit | Field | Description |
|---|---|---|
| 15 | SLEEP | This bit indicates whether or not the device is presently in SLEEP mode.<br>0 = Device is not in SLEEP mode.<br>1 = Device is in SLEEP mode. |
| 13 | SD_CMD | This bit is set when shutdown is pending because the command was received or the RST_SHUT pin was asserted for at least one second.<br>0 = Shutdown due to command or pin is not pending.<br>1 = Shutdown due to command or pin is pending. |
| 12 | PF | This bit indicates whether or not an enabled Permanent Fail fault has triggered.<br>0 = No Permanent Fail fault has triggered.<br>1 = At least one Permanent Fail fault has triggered. |
| 11 | SS | This bit indicates whether or not an enabled safety fault is triggered.<br>0 = No safety fault is triggered.<br>1 = At least one enabled safety fault is triggered. |
| 10 | FUSE | This bit reports the most recently observed state of the FUSE pin and is updated every second.<br>0 = FUSE pin was not asserted by device or secondary protector at last sample.<br>1 = FUSE pin was asserted by device or secondary protector at last sample. |
| 9–8 | SEC1–SEC0 | These bits indicate the present security state of the device. When in SEALED mode, device configuration may not be read or written and some commands are restricted. When in UNSEALED mode, device configuration may normally be read and may be written while in CONFIG_UPDATE mode. When in FULLACCESS mode, unrestricted read and write access is allowed and all commands are accepted. Even in FULLACCESS mode, changes to device configuration should only be changed while also in CONFIG_UPDATE mode.<br>0 = Device has not initialized yet.<br>1 = Device is in FULLACCESS mode.<br>2 = Device is in UNSEALED mode.<br>3 = Device is in SEALED mode. |
| 7 | OTPB | This bit indicates whether or not voltage and temperature conditions are valid for OTP programming. During normal operation, this bit will always be set if *Manufacturing Status()[OTPW]* is clear. When entering CONFIG_UPDATE mode, conditions will be checked and this bit will reflect whether or not programming is allowed (*Manufacturing Status()[OTPW]* does not apply in CONFIG_UPDATE mode). Once in CONFIG_UPDATE mode, this bit will not change state since no new measurements are being taken.<br>0 = OTP writes are allowed.<br>1 = Writes to OTP are blocked. |
| 6 | OTPW | This bit indicates whether or not some data is waiting to be written to OTP during normal operation. This can occur when, for example, configured to Permanent Fail information to OTP. This bit may remain set until conditions for OTP programming are met and all data is programmed. This bit is not set during OTP programming from CONFIG_UPDATE mode.<br>0 = No writes to OTP are pending.<br>1 = Writes to OTP are pending. |
| 5 | COW_CHK | This bit indicates while cell open-wire checks are occurring. When the feature is disabled, this bit will not set. When the feature is enabled, this bit will set periodically as the checks are performed.<br>0 = Device is not actively performing a cell open-wire check.<br>1 = Device is actively performing a cell open-wire check. |
| 4 | WD | This bit indicates whether or not the previous device reset was caused by the internal watchdog timer. This is not related to the Host Watchdog protection.<br>0 = Previous reset was normal.<br>1 = Previous reset was caused by the watchdog timer. |
| 3 | POR | This bit is set when the device fully resets. It is cleared upon exit of CONFIG_UPDATE mode. It can be used by the host to determine if any RAM configuration changes were lost due to a reset.<br>0 = Full reset has not occurred since last exit of CONFIG_UPDATE mode.<br>1 = Full reset has occurred since last exit of CONFIG_UPDATE and reconfiguration of any RAM settings is required. |

ADVANCE INFORMATION

**Table 56. Battery Status Register Field Descriptions (continued)**

| Bit | Field | Description |
|---|---|---|
| 2 | SLEEP_EN | This bit indicates whether or not SLEEP mode is allowed based on configuration and commands. The ***Settings:Configuration:Power Config[SLEEP]*** bit sets the default state of this bit. The host may send commands to enable or disable SLEEP mode based on system requirements. When this bit is set, the device may transition to SLEEP mode when other SLEEP criteria are met.<br>0 = SLEEP mode is disabled by the host.<br>1 = SLEEP mode is allowed when other SLEEP conditions are met. |
| 1 | PCHG_MODE | This bit indicates whether or not the device is in precharge mode. In precharge mode, the PCHG FET is turned on instead of the CHG FET.<br>0 = Device is not in precharge mode.<br>1 = Device is in precharge mode. |
| 0 | CFGUPDATE | This bit indicates whether or not the device is in CONFIG_UPDATE mode. It will be set after the SET_CFGUPDATE command is received and fully processed. Configuration settings may be changed only while this bit is set.<br>0 = Device is not in CONFIG_UPDATE mode.<br>1 = Device is in CONFIG_UPDATE mode. |

### *7.5.1.17 Alarm Status(): 0x62*

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| SSBC | SSA | PF | MSK_SFALERT | MSK_PFALERT | INITSTART | INITCOMP | RSVD_0 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FULLSCAN | XCHG | XDSG | SHUTV | FUSE | CB | ADSCAN | WAKE |

**Description**: Latched signal used to assert the ALERT pin. Write a bit high to clear the latch.

**Table 57. Alarm Status Register Field Descriptions**

| Bit | Field | Description |
|---|---|---|
| 15 | SSBC | This bit is set when a bit is set in *Safety Status B()* or *Safety Status C()*. |
| 14 | SSA | This bit is set when a bit is set in *Safety Status A()*. |
| 13 | PF | This bit is set when an enabled Permanent Fail fault triggers. |
| 12 | MSK_SFALERT | This bit is set when a safety alert is triggered that is also enabled in the corresponding ***Settings:Alarm:SF Alert Mask A***, ***Settings:Alarm:SF Alert Mask B***, or ***Settings:Alarm:SF Alert Mask C*** register. |
| 11 | MSK_PFALERT | This bit is set when a Permanent Fail alert is triggered that is also enabled in the corresponding ***Settings:Alarm:PF Alert Mask A***, ***Settings:Alarm:PF Alert Mask B***, ***Settings:Alarm:PF Alert Mask C***, or ***Settings:Alarm:PF Alert Mask D*** register. |
| 10 | INITSTART | Initialization started (sets quickly after device powers up). |
| 9 | INITCOMP | Initialization completed (sets after the device has powered and completed one measurement scan). |
| 7 | FULLSCAN | Full Voltage Scan Complete. The necessary multiple ADC scans have been completed to collect the full voltag emeasurement loop data (including cell voltages, pin or thermistor voltages, etc). This bit sets each time a full scan completes (when enabled). |
| 6 | XCHG | This bit is set when the CHG FET is off. |
| 5 | XDSG | This bit is set when the DSG FET is off. |
| 4 | SHUTV | Stack voltage is below ***Power:Shutdown:Shutdown Stack Voltage***. |
| 3 | FUSE | FUSE Pin Driven. FUSE pin is being driven by either the device or the secondary protector. |
| 2 | CB | This bit is set when cell balancing is active. |
| 1 | ADSCAN | Voltage ADC Scan Complete. A single ADC scan is complete (cell voltages are measured on each scan). This bit sets each time a scan completes (when enabled). |
| 0 | WAKE | This bit is set when the device is wakened from SLEEP mode. |

ADVANCE INFORMATION

### 7.5.1.18 Alarm Raw Status(): 0x64

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| SSBC | SSA | PF | MSK_SFALERT | MSK_PFALERT | INITSTART | INITCOMP | RSVD_0 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FULLSCAN | XCHG | XDSG | SHUTV | FUSE | CB | ADSCAN | WAKE |

**Description**: Unlatched value of flags which can be selected to be latched (using *Alarm Enable()*) and used to assert the ALERT pin.

**Table 58. Alarm Raw Status Register Field Descriptions**

| Bit | Field | Description |
|---|---|---|
| 15 | SSBC | This bit is set when a bit is set in *Safety Status B()* or *Safety Status C()*. |
| 14 | SSA | This bit is set when a bit is set in *Safety Status A()*. |
| 13 | PF | This bit is set when an enabled Permanent Fail fault triggers. |
| 12 | MSK_SFALERT | This bit is set when a safety alert is triggered that is also enabled in the corresponding ***Settings:Alarm:SF Alert Mask A***, ***Settings:Alarm:SF Alert Mask B***, or ***Settings:Alarm:SF Alert Mask C*** register. |
| 11 | MSK_PFALERT | This bit is set when a Permanent Fail alert is triggered that is also enabled in the corresponding ***Settings:Alarm:PF Alert Mask A***, ***Settings:Alarm:PF Alert Mask B***, ***Settings:Alarm:PF Alert Mask C***, or ***Settings:Alarm:PF Alert Mask D*** register. |
| 10 | INITSTART | Initialization started (sets quickly after device powers up). |
| 9 | INITCOMP | Initialization completed (sets after the device has powered and completed one measurement scan). |
| 7 | FULLSCAN | Full Voltage Scan Complete. The necessary multiple ADC scans have been completed to collect the full voltage measurement loop data (including cell voltages, pin or thermistor voltages, etc). This bit sets after the first full scan completes, then remains set. |
| 6 | XCHG | This bit is set when the CHG FET is off. |
| 5 | XDSG | This bit is set when the DSG FET is off. |
| 4 | SHUTV | Stack voltage is below ***Power:Shutdown:Shutdown Stack Voltage***. |
| 3 | FUSE | FUSE Pin Driven. FUSE pin is being driven by either the device or the secondary protector. |
| 2 | CB | This bit is set when cell balancing is active. |
| 1 | ADSCAN | Voltage ADC Scan Complete. A single ADC scan is complete (cell voltages are measured on each scan). This bit sets after the first ADC scan completes, then remains set. |
| 0 | WAKE | This bit is set when the device is wakened from SLEEP mode. |

### 7.5.1.19 Alarm Enable(): 0x66

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| SSBC | SSA | PF | MSK_SFALERT | MSK_PFALERT | INITSTART | INITCOMP | RSVD_0 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FULLSCAN | XCHG | XDSG | SHUTV | FUSE | CB | ADSCAN | WAKE |

**Description**: Mask for *Alarm Status()*. Can be written to change during operation to change which alarm sources are enabled. The default value of this parameter is set by ***Settings:Alarm:Default Alarm Mask***.

**Table 59. Alarm Enable Register Field Descriptions**

| Bit | Field | Description |
|---|---|---|
| 15 | SSBC | This bit is set when a bit is set in *Safety Status B()* or *Safety Status C()*. |
| 14 | SSA | This bit is set when a bit is set in *Safety Status A()*. |
| 13 | PF | This bit is set when an enabled Permanent Fail fault triggers. |
| 12 | MSK_SFALERT | This bit is set when a safety alert is triggered that is also enabled in the corresponding ***Settings:Alarm:SF Alert Mask A***, ***Settings:Alarm:SF Alert Mask B***, or ***Settings:Alarm:SF Alert Mask C*** register. |
| 11 | MSK_PFALERT | This bit is set when a Permanent Fail alert is triggered that is also enabled in the corresponding ***Settings:Alarm:PF Alert Mask A***, ***Settings:Alarm:PF Alert Mask B***, ***Settings:Alarm:PF Alert Mask C***, or ***Settings:Alarm:PF Alert Mask D*** register. |
| 10 | INITSTART | Initialization started (sets quickly after device powers up). |

**Table 59. Alarm Enable Register Field Descriptions (continued)**

| Bit | Field | Description |
|---|---|---|
| 9 | INITCOMP | Initialization completed (sets after the device has powered and completed one measurement scan). |
| 7 | FULLSCAN | Full Voltage Scan Complete. The necessary multiple ADC scans have been completed to collect the full voltage measurement loop data (including cell voltages, pin or thermistor voltages, etc). This bit sets each time a full scan completes (when enabled). |
| 6 | XCHG | This bit is set when the CHG FET is off. |
| 5 | XDSG | This bit is set when the DSG FET is off. |
| 4 | SHUTV | Stack voltage is below ***Power:Shutdown:Shutdown Stack Voltage***. |
| 3 | FUSE | FUSE Pin Driven. FUSE pin is being driven by either the device or the secondary protector. |
| 2 | CB | This bit is set when cell balancing is active. |
| 1 | ADSCAN | Voltage ADC Scan Complete. A single ADC scan is complete (cell voltages are measured on each scan). This bit sets each time a scan completes (when enabled). |
| 0 | WAKE | This bit is set when the device is wakened from SLEEP mode. |

#### *7.5.1.20 FET Status(): 0x7F*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RSVD_0 | ALRT_PIN | DDSG_PIN | DCHG_PIN | PDSG_FET | DSG_FET | PCHG_FET | CHG_FET |

**Description**: Provides flags showing status of FETs and ALERT pin.

**Table 60. FET Status Register Field Descriptions**

| Bit | Field | Description |
|---|---|---|
| 6 | ALRT_PIN | Indicates the status of the ALERT pin.<br>0 = The ALERT pin is not asserted.<br>1 = The ALERT pin is asserted. |
| 5 | DDSG_PIN | Indicates the status of the DDSG pin.<br>0 = The DDSG pin is not asserted.<br>1 = The DDSG pin is asserted. |
| 4 | DCHG_PIN | Indicates the status of the DCHG pin.<br>0 = The DCHG pin is not asserted.<br>1 = The DCHG pin is asserted. |
| 3 | PDSG_FET | Indicates the status of the PDSG FET.<br>0 = The PDSG FET is off.<br>1 = The PDSG FET is on. |
| 2 | DSG_FET | Indicates the status of the DSG FET.<br>0 = The DSG FET is off.<br>1 = The DSG FET is on. |
| 1 | PCHG_FET | Indicates the status of the PCHG FET.<br>0 = The PCHG FET is off.<br>1 = The PCHG FET is on. |
| 0 | CHG_FET | Indicates the status of the CHG FET.<br>0 = The CHG FET is off.<br>1 = The CHG FET is on. |

### 7.5.2 Bitfield Definitions for Subcommands

#### *7.5.2.1 0x0053 PF_STATUS[0]: PF Status A()*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CUDEP | SOTF | RSVD_0 | SOT | SOCD | SOCC | SOV | SUV |

ADVANCE INFORMATION

**Description**: Saved Permanent Failure Status A

**Table 61. PF Status A Register Field Descriptions**

| Bit | Field | Description |
|---|---|---|
| 7 | CUDEP | 0 = Copper Deposition Permanent Fail did not occur<br>1 = Copper Deposition Permanent Fail occurred |
| 6 | SOTF | 0 = Safety FET Overtemperature Permanent Fail did not occur<br>1 = Safety FET Overtemperature Permanent Fail occurred |
| 4 | SOT | 0 = Safety Cell Overtemperature Permanent Fail did not occur<br>1 = Safety Cell Overtemperature Permanent Fail occurred |
| 3 | SOCD | 0 = Safety Overcurrent in Discharge Permanent Fail did not occur<br>1 = Safety Overcurrent in Discharge Permanent Fail occurred |
| 2 | SOCC | 0 = Safety Overcurrent in Charge Permanent Fail did not occur<br>1 = Safety Overcurrent in Charge Permanent Fail occurred |
| 1 | SOV | 0 = Safety Cell Overvoltage Permanent Fail did not occur<br>1 = Safety Cell Overvoltage Permanent Fail occurred |
| 0 | SUV | 0 = Safety Cell Undervoltage Permanent Fail did not occur<br>1 = Safety Cell Undervoltage Permanent Fail occurred |

### *7.5.2.2 0x0053 PF_STATUS[1]: PF Status B()*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SCDL | RSVD_0 | RSVD_0 | VIMA | VIMR | 2LVL | DFETF | CFETF |

**Description**: Saved Permanent Failure Status B

**Table 62. PF Status B Register Field Descriptions**

| Bit | Field | Description |
|---|---|---|
| 7 | SCDL | 0 = Latched Short Circuit in Discharge Permanent Fail did not occur<br>1 = Latched Short Circuit in Discharge Permanent Fail occurred |
| 4 | VIMA | 0 = Voltage Imbalance in Active Permanent Fail did not occur<br>1 = Voltage Imbalance in Active Permanent Fail occurred |
| 3 | VIMR | 0 = Voltage Imbalance in Relax Permanent Fail did not occur<br>1 = Voltage Imbalance in Relax Permanent Fail occurred |
| 2 | 2LVL | 0 = Secondary Protector Permanent Fail did not occur<br>1 = Secondary Protector Permanent Fail occurred |
| 1 | DFETF | 0 = DSG FET Fail Permanent Fail did not occur<br>1 = DSG FET Fail Permanent Fail occurred |
| 0 | CFETF | 0 = CHG FET Fail Permanent Fail did not occur<br>1 = CHG FET Fail Permanent Fail occurred |

### *7.5.2.3 0x0053 PF_STATUS[2]: PF Status C()*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CMDF | HWMX | VSSF | VREF | LFOF | IRMF | DRMF | OTPF |

ADVANCE INFORMATION

**Description**: Saved Permanent Failure Status D

**Table 63. PF Status C Register Field Descriptions**

| Bit | Field | Description |
|---|---|---|
| 7 | CMDF | 0 = Commanded Permanent Fail did not occur<br>1 = Commanded Permanent Fail occurred |
| 6 | HWMX | 0 = Protection Comparator MUX Permanent Fail did not occur<br>1 = Protection Comparator MUX Permanent Fail occurred |
| 5 | VSSF | 0 = VSS Permanent Fail did not occur<br>1 = VSS Permanent Fail occurred |
| 4 | VREF | 0 = VREF Permanent Fail did not occur<br>1 = VREF Permanent Fail occurred |
| 3 | LFOF | 0 = Low Frequency Oscillator Monitor Permanent Fail did not occur<br>1 = Low Frequency Oscillator Monitor Permanent Fail occurred |
| 2 | IRMF | 0 = Instruction ROM Permanent Fail did not occur<br>1 = Instruction ROM Permanent Fail occurred |
| 1 | DRMF | 0 = Data ROM Permanent Fail did not occur<br>1 = Data ROM Permanent Fail occurred |
| 0 | OTPF | 0 = OTP Memory Permanent Fail did not occur<br>1 = OTP Memory Permanent Fail occurred |

### *7.5.2.4 0x0053 PF_STATUS[3]: PF Status D()*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | TOSF |

**Description**: Saved Permanent Failure Status D

**Table 64. PF Status D Register Field Descriptions**

| Bit | Field | Description |
|---|---|---|
| 0 | TOSF | 0 = Top-of-Stack Permanent Fail did not occur<br>1 = Top-of-Stack Permanent Fail occurred |

### *7.5.2.5 0x0057 MANUFACTURINGSTATUS[0–1]: Manufacturing Status()*

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OTPW_EN | PF_EN | PDSG_TEST | FET_EN | RSVD_0 | DSG_TEST | CHG_TEST | PCHG_TEST |

**Description**: Provides flags for use during manufacturing.

**Table 65. Manufacturing Status Register Field Descriptions**

| Bit | Field | Description |
|---|---|---|
| 7 | OTPW_EN | This bit enables or disables writes to OTP during normal operation. The device can program bits in OTP when a PF occurs or when the fuse is blown to retain state after a full reset. It also can program MANU_DATA upon request (if in FULLACCESS mode). This bit enables the device to program this runtime data to OTP. Programming will only occur when the stack voltage and temperature are within allowed limits. If this bit is not set, programming may still be done in CONFIG_UPDATE mode.<br>0 = Device will not program OTP during normal operation<br>1 = Device may program OTP during normal operation |

ADVANCE INFORMATION

**Table 65. Manufacturing Status Register Field Descriptions (continued)**

| Bit | Field | Description |
|---|---|---|
| 6 | PF_EN | This bit enables or disables Permanent Failure checks. Clearing this bit prevents Permanent Failure from triggering which is useful during manufacturing.<br>0 = Permanent Failure checks are disabled<br>1 = Permanent Failure checks are enabled |
| 5 | PDSG_TEST | This bit indicates whether the PDSG FET is enabled in FET Test mode. This bit is controlled using the PDSGTEST() subcommand.<br>0 = PDSG FET is not enabled in FET Test mode<br>1 = PDSG FET is enabled in FET Test mode |
| 4 | FET_EN | This bit enables or disables FET Test mode. In FET Test mode, the FET states are controlled by the FET Test subcommands. This is typically used during manufacturing to test FET circuitry. Note: safety checks still may force FETs off (or for body diode protection, on) in FET Test mode.<br>0 = Normal FET control is disabled. FET Test mode is enabled. Device will not turn on FETs unless FET Test subcommands instruct it to do so<br>1 = Normal FET control is enabled. FET Test mode is disabled. Device will ignore FET Test subcommands |
| 2 | DSG_TEST | This bit indicates whether the DSG FET is enabled in FET Test mode. This bit is controlled using the DSGTEST() subcommand.<br>0 = DSG FET is not enabled in FET Test mode<br>1 = DSG FET is enabled in FET Test mode |
| 1 | CHG_TEST | This bit indicates whether the CHG FET is enabled in FET Test mode. This bit is controlled using the CHGTEST() subcommand.<br>0 = CHG FET is not enabled in FET Test mode<br>1 = CHG FET is enabled in FET Test mode |
| 0 | PCHG_TEST | This bit indicates whether the PCHG FET is enabled in FET Test mode. This bit is controlled using the PCHGTEST() subcommand.<br>0 = PCHG FET is not enabled in FET Test mode<br>1 = PCHG FET is enabled in FET Test mode |

### 7.5.2.6 0x0097 FET_CONTROL[0]: FET Control()

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | PCHG_OFF | CHG_OFF | PDSG_OFF | DSG_OFF |

**Description**: Allows host control of individual FET drivers.

**Table 66. FET Control Register Field Descriptions**

| Bit | Field | Description |
|---|---|---|
| 3 | PCHG_OFF | 0 = PCHG FET is allowed to turn on if other conditions are met<br>1 = PCHG FET driver is forced off |
| 2 | CHG_OFF | 0 = CHG FET is allowed to turn on if other conditions are met<br>1 = CHG FET driver is forced off |
| 1 | PDSG_OFF | 0 = PDSG FET is allowed to turn on if other conditions are met<br>1 = PDSG FET driver is forced off |
| 0 | DSG_OFF | 0 = DSG FET is allowed to turn on if other conditions are met<br>1 = DSG FET driver is forced off |

### 7.5.2.7 0x0098 REG12_CONTROL[0]: REG12 Control()

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| REG2V_2 | REG2V_1 | REG2V_0 | REG2_EN | REG1V_2 | REG1V_1 | REG1V_0 | REG1_EN |

ADVANCE INFORMATION

**Description**: Changes voltage regulator settings

**Table 67. REG12 Control Register Field Descriptions**

| Bit | Field | Description |
|---|---|---|
| 7–5 | REG2V_2–REG2V_0 | Selects voltage level for REG2<br>0–3 = 1.8 V<br>4 = 2.5 V<br>5 = 3 V<br>6 = 3.3 V<br>7 = 5 V |
| 4 | REG2_EN | Enables or disables REG2<br>0 = REG2 Disabled<br>1 = REG2 Enabled |
| 3–1 | REG1V_2–REG1V_0 | Selects voltage level for REG1<br>0–3 = 1.8 V<br>4 = 2.5 V<br>5 = 3 V<br>6 = 3.3 V<br>7 = 5 V |
| 0 | REG1_EN | Enables or disables REG1<br>0 = REG1 Disabled<br>1 = REG1 Enabled |

### *7.5.2.8 0x00A0 OTP_WR_CHECK[0]: OTP Write Check Result()*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OK | RSVD_0 | LOCK | NOSIG | NODATA | HT | LV | HV |

**Description**: Reports whether or not OTP programming is allowed.

**Table 68. OTP Write Check Result Register Field Descriptions**

| Bit | Field | Description |
|---|---|---|
| 7 | OK | This bit is set whenever programming conditions are met. None of the other bits will be set when this bit is set.<br>0 = OTP programming is not allowed.<br>1 = OTP programming is okay. |
| 5 | LOCK | The device is not in FULLACCESS and CONFIG_UPDATE mode, or the OTP Lock bit has been set to prevent further modification.<br>0 = OTP is not locked.<br>1 = OTP is locked. |
| 4 | NOSIG | OTP signature cannot be written (indicating that the signature has already been written too many times).<br>0 = OTP signature can be programmed.<br>1 = OTP signature could not be programmed. |
| 3 | NODATA | Could not program data into OTP (indicating data has been programmed too many times, no XOR bits left). When this bit is set, the following bytes will indicate the address of the first failing parameter.<br>0 = Data can be programmed into OTP.<br>1 = Data could not be programmed into OTP. |
| 2 | HT | The measured internal temperature is above the allowed OTP programming temperature range.<br>0 = Temperature is within the allowed range.<br>1 = Temperature is too high to program OTP. |
| 1 | LV | The measured stack voltage is below the allowed OTP programming voltage.<br>0 = The measured stack voltage is above the minimum OTP programming voltage.<br>1 = The measured stack voltage is below the minimum OTP programming voltage. |

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**Table 68. OTP Write Check Result Register Field Descriptions (continued)**

| Bit | Field | Description |
|---|---|---|
| 0 | HV | The measured stack voltage is above the allowed OTP programming voltage.<br>0 = The measured stack voltage is below the maximum OTP programming voltage.<br>1 = The measured stack voltage is above the maximum OTP programming voltage. |

### *7.5.2.9 0x00A1 OTP_WRITE[0]: OTP Write Result()*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OK | RSVD_0 | LOCK | NOSIG | NODATA | HT | LV | HV |

**Description**: Reports whether or not OTP programming is allowed.

**Table 69. OTP Write Result Register Field Descriptions**

| Bit | Field | Description |
|---|---|---|
| 7 | OK | This bit is set whenever programming conditions are met. None of the other bits will be set when this one is.<br>0 = OTP programming is not allowed.<br>1 = OTP programming is okay. |
| 5 | LOCK | The device is not in FULLACCESS and CONFIG_UPDATE mode, or the OTP Lock bit has been set to prevent further modification.<br>0 = OTP is not locked.<br>1 = OTP is locked. |
| 4 | NOSIG | Signature cannot be written (indicating that the signature has already been written too many times).<br>0 = OTP signature can be programmed<br>1 = OTP signature could not be programmed |
| 3 | NODATA | Could not program OTP data (indicating data has been programmed too many times, no XOR bits left). When this bit is set, the following bytes will indicate the address of the first failing parameter.<br>0 = Data can be programmed.<br>1 = Data could not be programmed. |
| 2 | HT | The measured internal temperature is above the allowed OTP programming temperature range.<br>0 = Temperature is within the allowed range.<br>1 = Temperature is too high to program OTP. |
| 1 | LV | The measured stack voltage is below the allowed OTP programming voltage.<br>0 = The measured stack voltage is above the minimum OTP programming voltage.<br>1 = The measured stack voltage is below the minimum OTP programming voltage. |
| 0 | HV | The measured stack voltage is above the allowed OTP programming voltage.<br>0 = The measured stack voltage is below the maximum OTP programming voltage.<br>1 = The measured stack voltage is above the maximum OTP programming voltage. |

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## 7.6 Data Memory Settings

The data memory values in BQ76942 are accessed in similar fashion to subcommands, using the address for a data value rather than the subcommand address. For example, to write the ***Calibration:Voltage:Cell 0 Gain*** to a value of 12410 (0x307A), determine the register address from the Data Memory Table at Table 105, which shows this address is 0x9180. Then the data is written as shown below:

1. Write lower byte of address to 0x3E (0x80 in this example)
2. Write upper byte of address to 0x3F (0x91 in this example)
3. Write the data memory value in little endian format into the transfer buffer (0x40 to 0x5F). Note: up to 32 bytes of data memory can be written in one block write. In this example, write 0x7A to 0x40, write 0x30 to 0x41.
4. Write the checksum of data written (0x44 in this example) into 0x60, and the length of data (0x06 in this example) into 0x61.
5. The data can be verified by reading it back. Write the lower byte of address to 0x3E (0x80), write the upper byte of address to 0x3F (0x91).

## Data Memory Settings (continued)

6. Read the length of response from 0x61. The transfer buffer will be populated with a 32-byte block of data, so length will be 36-bytes, or 0x24 for this example.
7. Read buffer starting at 0x40 for the length of data. The new value for ***Calibration:Voltage:Cell 0 Gain*** is seen in 0x40 (0x7A) and 0x41 (0x30).
8. Read the checksum at 0x60 and verify it matches the data read for the full transfer buffer.

Note: 0x61 provides the length of the buffer data + 4 (that is, length of buffer data + length of 0x3E and 0x3F + length of 0x60 and 0x61).

The checksum is calculated over 0x3E and 0x3F and the buffer data, it does not include the checksum or length in 0x60 and 0x61.

The configuration settings for the BQ76942 device are shown below.

### 7.6.1 Calibration

#### *7.6.1.1 Calibration:Voltage*

##### 7.6.1.1.1 Calibration:Voltage:Cell 1 Gain

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Voltage | Cell 1 Gain | I2 | –32767 | 32767 | 0 | — |

**Description**: Cell voltage calculations use a linear gain set by this value. Gain is factory-calibrated but can be modified by adjusting this value. While in CONFIG_UPDATE mode, this value will reflect the programmed setting. While not in CONFIG_UPDATE mode, this value will reflect the value that is being used in calculations.

0 = Use factory-calibrated value.

All other values = Use specified value.

##### 7.6.1.1.2 Calibration:Voltage:Cell 2 Gain

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Voltage | Cell 2 Gain | I2 | –32767 | 32767 | 0 | — |

**Description**: Cell voltage calculations use a linear gain set by this value. Gain is factory-calibrated but can be modified by adjusting this value. While in CONFIG_UPDATE mode, this value will reflect the programmed setting. While not in CONFIG_UPDATE mode, this value will reflect the value that is being used in calculations.

0 = Use factory-calibrated value.

All other values = Use specified value.

##### 7.6.1.1.3 Calibration:Voltage:Cell 3 Gain

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Voltage | Cell 3 Gain | I2 | –32767 | 32767 | 0 | — |

**Description**: Cell voltage calculations use a linear gain set by this value. Gain is factory-calibrated but can be modified by adjusting this value. While in CONFIG_UPDATE mode, this value will reflect the programmed setting. While not in CONFIG_UPDATE mode, this value will reflect the value that is being used in calculations.

0 = Use factory-calibrated value.

All other values = Use specified value.

##### 7.6.1.1.4 Calibration:Voltage:Cell 4 Gain

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Voltage | Cell 4 Gain | I2 | –32767 | 32767 | 0 | — |

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**Description**: Cell voltage calculations use a linear gain set by this value. Gain is factory-calibrated but can be modified by adjusting this value. While in CONFIG_UPDATE mode, this value will reflect the programmed setting. While not in CONFIG_UPDATE mode, this value will reflect the value that is being used in calculations.

0 = Use factory-calibrated value.

All other values = Use specified value.

#### 7.6.1.1.5 Calibration:Voltage:Cell 5 Gain

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Voltage | Cell 5 Gain | I2 | –32767 | 32767 | 0 | — |

**Description**: Cell voltage calculations use a linear gain set by this value. Gain is factory-calibrated but can be modified by adjusting this value. While in CONFIG_UPDATE mode, this value will reflect the programmed setting. While not in CONFIG_UPDATE mode, this value will reflect the value that is being used in calculations.

0 = Use factory-calibrated value.

All other values = Use specified value.

#### 7.6.1.1.6 Calibration:Voltage:Cell 6 Gain

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Voltage | Cell 6 Gain | I2 | –32767 | 32767 | 0 | — |

**Description**: Cell voltage calculations use a linear gain set by this value. Gain is factory-calibrated but can be modified by adjusting this value. While in CONFIG_UPDATE mode, this value will reflect the programmed setting. While not in CONFIG_UPDATE mode, this value will reflect the value that is being used in calculations.

0 = Use factory-calibrated value.

All other values = Use specified value.

#### 7.6.1.1.7 Calibration:Voltage:Cell 7 Gain

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Voltage | Cell 7 Gain | I2 | –32767 | 32767 | 0 | — |

**Description**: Cell voltage calculations use a linear gain set by this value. Gain is factory-calibrated but can be modified by adjusting this value. While in CONFIG_UPDATE mode, this value will reflect the programmed setting. While not in CONFIG_UPDATE mode, this value will reflect the value that is being used in calculations.

0 = Use factory-calibrated value.

All other values = Use specified value.

#### 7.6.1.1.8 Calibration:Voltage:Cell 8 Gain

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Voltage | Cell 8 Gain | I2 | –32767 | 32767 | 0 | — |

**Description**: Cell voltage calculations use a linear gain set by this value. Gain is factory-calibrated but can be modified by adjusting this value. While in CONFIG_UPDATE mode, this value will reflect the programmed setting. While not in CONFIG_UPDATE mode, this value will reflect the value that is being used in calculations.

0 = Use factory-calibrated value.

All other values = Use specified value.

#### 7.6.1.1.9 Calibration:Voltage:Cell 9 Gain

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Voltage | Cell 9 Gain | I2 | –32767 | 32767 | 0 | — |

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**Description**: Cell voltage calculations use a linear gain set by this value. Gain is factory-calibrated but can be modified by adjusting this value. While in CONFIG_UPDATE mode, this value will reflect the programmed setting. While not in CONFIG_UPDATE mode, this value will reflect the value that is being used in calculations.

0 = Use factory-calibrated value.

All other values = Use specified value.

#### 7.6.1.1.10 Calibration:Voltage:Cell 10 Gain

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Voltage | Cell 10 Gain | I2 | –32767 | 32767 | 0 | — |

**Description**: Cell voltage calculations use a linear gain set by this value. Gain is factory-calibrated but can be modified by adjusting this value. While in CONFIG_UPDATE mode, this value will reflect the programmed setting. While not in CONFIG_UPDATE mode, this value will reflect the value that is being used in calculations.

0 = Use factory-calibrated value.

All other values = Use specified value.

#### 7.6.1.1.11 Calibration:Voltage:Pack Gain

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Voltage | Pack Gain | U2 | 0 | 65535 | 35507 | — |

**Description**: The PACK pin voltage calculation uses a linear gain set by this value.

#### 7.6.1.1.12 Calibration:Voltage:TOS Gain

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Voltage | TOS Gain | U2 | 0 | 65535 | 35507 | — |

**Description**: The Top-of-Stack voltage calculation uses a linear gain set by this value.

#### 7.6.1.1.13 Calibration:Voltage:LD Gain

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Voltage | LD Gain | U2 | 0 | 65535 | 35507 | — |

**Description**: The LD pin voltage calculation uses a linear gain set by this value.

#### 7.6.1.1.14 Calibration:Voltage:ADC Gain

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Voltage | ADC Gain | I2 | –32767 | 32767 | 0 | — |

**Description**: Pins configured as ADCIN use this linear gain value to convert ADC counts to millivolts.

### *7.6.1.2 Calibration:Current*

#### 7.6.1.2.1 Calibration:Current:CC Gain

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Current | CC Gain | F4 | 1.00E–01 | 10.00E+00 | 7.4768 | — |

**Description**: This parameter sets the gain factor used to convert coulomb counter raw count measurements to current. The value is given by

***Calibration:Current:CC Gain*** = 7.4768 / (Rsense in mOhm)

This value should be adjusted based on the sense resistor value in the system and can be further calibrated, if desired.

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#### 7.6.1.2.2 Calibration:Current:Capacity Gain

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Current | Capacity Gain | F4 | 2.98262E+04 | 4.193046E+06 | 2230042.463 | — |

**Description**: This parameter sets the gain factor used to convert coulomb counter raw count measurements to passed charge. The value is given by

***Calibration:Current:Capacity Gain*** = ***Calibration:Current:CC Gain*** x 298261.6178

This should be adjusted based on the sense resistor value in the system and can be further calibrated, if desired.

### *7.6.1.3 Calibration:Vcell Offset*

#### 7.6.1.3.1 Calibration:Vcell Offset:Vcell Offset

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Vcell Offset | Vcell Offset | I2 | –32767 | 32767 | 0 | mV |

**Description**: This offset is subtracted from all cell voltage measurement values and can be used to calibrate out offset error.

### *7.6.1.4 Calibration:V Divider Offset*

#### 7.6.1.4.1 Calibration:V Divider Offset:Vdiv Offset

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | V Divider Offset | Vdiv Offset | I2 | –32767 | 32767 | 0 | userV |

**Description**: This offset is subtracted from all *Stack Voltage()*, *PACK Pin Voltage()*, and *LD Pin Voltage()* measurements and can be used to calibrate out offset error.

### *7.6.1.5 Calibration:Current Offset*

#### 7.6.1.5.1 Calibration:Current Offset:Coulomb Counter Offset Samples

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Current Offset | Coulomb Counter Offset Samples | U2 | 0 | 65535 | 64 | — |

**Description**: Sets the scale of ***Calibration:Current Offset:Board Offset***. That parameter is defined as how many counts of offset error would accumulate over this many coulomb counter conversions.

#### 7.6.1.5.2 Calibration:Current Offset:Board Offset

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Current Offset | Board Offset | I2 | –32768 | 32767 | 0 | — |

**Description**: This board-level offset is subtracted from the coulomb counter conversion results in current calculations. To enable higher-resolution calibration, this value is divided by ***Calibration:Current Offset:Coulomb Counter Offset Samples*** before being used. This enables subtraction of fractional-count offsets.

### *7.6.1.6 Calibration:Temperature*

#### 7.6.1.6.1 Calibration:Temperature:Internal Temp Offset

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Temperature | Internal Temp Offset | I1 | –128 | 127 | 0 | 0.1°C |

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**Description**: This offset is added to internal temperature measurements to increase accuracy.

#### 7.6.1.6.2 Calibration:Temperature:CFETOFF Temp Offset

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Temperature | CFETOFF Temp Offset | I1 | –128 | 127 | 0 | 0.1°C |

**Description**: This offset is added to temperature measurements when this pin is used as a thermistor and a polynomial is enabled. This is not applied if the pin is configured as ADCIN or when using no polynomial.

#### 7.6.1.6.3 Calibration:Temperature:DFETOFF Temp Offset

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Temperature | DFETOFF Temp Offset | I1 | –128 | 127 | 0 | 0.1°C |

**Description**: This offset is added to temperature measurements when this pin is used as a thermistor and a polynomial is enabled. This is not applied if the pin is configured as ADCIN or when using no polynomial.

#### 7.6.1.6.4 Calibration:Temperature:ALERT Temp Offset

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Temperature | ALERT Temp Offset | I1 | –128 | 127 | 0 | 0.1°C |

**Description**: This offset is added to temperature measurements when this pin is used as a thermistor and a polynomial is enabled. This is not applied if the pin is configured as ADCIN or when using no polynomial.

#### 7.6.1.6.5 Calibration:Temperature:TS1 Temp Offset

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Temperature | TS1 Temp Offset | I1 | –128 | 127 | 0 | 0.1°C |

**Description**: This offset is added to temperature measurements when this pin is used as a thermistor and a polynomial is enabled. This is not applied if the pin is configured as ADCIN or when using no polynomial.

#### 7.6.1.6.6 Calibration:Temperature:TS2 Temp Offset

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Temperature | TS2 Temp Offset | I1 | –128 | 127 | 0 | 0.1°C |

**Description**: This offset is added to temperature measurements when this pin is used as a thermistor and a polynomial is enabled. This is not applied if the pin is configured as ADCIN or when using no polynomial.

#### 7.6.1.6.7 Calibration:Temperature:TS3 Temp Offset

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Temperature | TS3 Temp Offset | I1 | –128 | 127 | 0 | 0.1°C |

**Description**: This offset is added to temperature measurements when this pin is used as a thermistor and a polynomial is enabled. This is not applied if the pin is configured as ADCIN or when using no polynomial.

#### 7.6.1.6.8 Calibration:Temperature:HDQ Temp Offset

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Temperature | HDQ Temp Offset | I1 | –128 | 127 | 0 | 0.1°C |

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**Description**: This offset is added to temperature measurements when this pin is used as a thermistor and a polynomial is enabled. This is not applied if the pin is configured as ADCIN or when using no polynomial.

#### 7.6.1.6.9 Calibration:Temperature:DCHG Temp Offset

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Temperature | DCHG Temp Offset | I1 | –128 | 127 | 0 | 0.1°C |

**Description**: This offset is added to temperature measurements when this pin is used as a thermistor and a polynomial is enabled. This is not applied if the pin is configured as ADCIN or when using no polynomial.

#### 7.6.1.6.10 Calibration:Temperature:DDSG Temp Offset

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Temperature | DDSG Temp Offset | I1 | –128 | 127 | 0 | 0.1°C |

**Description**: This offset is added to temperature measurements when this pin is used as a thermistor and a polynomial is enabled. This is not applied if the pin is configured as ADCIN or when using no polynomial.

### *7.6.1.7 Calibration:Internal Temp Model*

#### 7.6.1.7.1 Calibration:Internal Temp Model:Int Gain

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Internal Temp Model | Int Gain | I2 | –32768 | 32767 | 25390 | — |

**Description**: The internal temperature calculation uses a linear gain set by this value.

#### 7.6.1.7.2 Calibration:Internal Temp Model:Int base offset

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Internal Temp Model | Int base offset | I2 | –32768 | 32767 | 33 | — |

**Description**: The internal temperature calculation adds this offset to the result after gain is applied.

#### 7.6.1.7.3 Calibration:Internal Temp Model:Int Maximum AD

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Internal Temp Model | Int Maximum AD | I2 | –32768 | 32767 | 16383 | — |

**Description**: The internal temperature calculation accuracy is limited when counts exceed a certain value. When the counts are greater than that value, a fixed value is reported for internal temperature. This parameter specifies that threshold. This value should not normally be changed.

#### 7.6.1.7.4 Calibration:Internal Temp Model:Int Maximum Temp

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Internal Temp Model | Int Maximum Temp | I2 | 0 | 32767 | 6379 | 0.1K |

**Description**: When the internal temperature ADC measurement's counts exceed ***Calibration:Internal Temp Model:Int Maximum AD***, this temperature is reported for internal temperature. This value should not normally be changed.

### *7.6.1.8 Calibration:18K Temperature Model*

#### 7.6.1.8.1 Calibration:18K Temperature Model:Coeff a1

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | 18K Temperature Model | Coeff a1 | I2 | –32768 | 32767 | –11130 | — |

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**Description**: This is the coefficient of the 4th power element of the first temperature polynomial.

#### 7.6.1.8.2 Calibration:18K Temperature Model:Coeff a2

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | 18K Temperature Model | Coeff a2 | I2 | –32768 | 32767 | 19142 | — |

**Description**: This is the coefficient of the 3rd power element of the first temperature polynomial.

#### 7.6.1.8.3 Calibration:18K Temperature Model:Coeff a3

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | 18K Temperature Model | Coeff a3 | I2 | –32768 | 32767 | –19262 | — |

**Description**: This is the coefficient of the 2nd power element of the first temperature polynomial.

#### 7.6.1.8.4 Calibration:18K Temperature Model:Coeff a4

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | 18K Temperature Model | Coeff a4 | I2 | –32768 | 32767 | 28203 | — |

**Description**: This is the coefficient of the 1st power element of the first temperature polynomial.

#### 7.6.1.8.5 Calibration:18K Temperature Model:Coeff a5

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | 18K Temperature Model | Coeff a5 | I2 | –32768 | 32767 | 892 | — |

**Description**: This is the coefficient of the 0th power element of the first temperature polynomial.

#### 7.6.1.8.6 Calibration:18K Temperature Model:Coeff b1

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | 18K Temperature Model | Coeff b1 | I2 | –32768 | 32767 | 328 | — |

**Description**: This is the coefficient of the 3rd power element of the second temperature polynomial.

#### 7.6.1.8.7 Calibration:18K Temperature Model:Coeff b2

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | 18K Temperature Model | Coeff b2 | I2 | –32768 | 32767 | –605 | — |

**Description**: This is the coefficient of the 2nd power element of the second temperature polynomial.

#### 7.6.1.8.8 Calibration:18K Temperature Model:Coeff b3

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | 18K Temperature Model | Coeff b3 | I2 | –32768 | 32767 | –2443 | — |

**Description**: This is the coefficient of the 1st power element of the second temperature polynomial.

#### 7.6.1.8.9 Calibration:18K Temperature Model:Coeff b4

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | 18K Temperature Model | Coeff b4 | I2 | –32768 | 32767 | 4696 | — |

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**Description**: This is the coefficient of the 0th power element of the second temperature polynomial.

#### 7.6.1.8.10 Calibration:18K Temperature Model:Adc0

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | 18K Temperature Model | Adc0 | I2 | –32768 | 32767 | 11703 | — |

**Description**: Temperature correction factor corresponding to actual ADC measurement at the calibration temperature, with a scale factor included. With the thermistor attached to TS1 at the calibration temperature, the TS1 Raw ADC Counts (in 32-bit format) is divided by 256, then multiplied by 5/3, and used for this setting.

### *7.6.1.9 Calibration:180K Temperature Model*

#### 7.6.1.9.1 Calibration:180K Temperature Model:Coeff a1

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | 180K Temperature Model | Coeff a1 | I2 | –32768 | 32767 | –17513 | — |

**Description**: This is the coefficient of the fourth power element of the first temperature polynomial.

#### 7.6.1.9.2 Calibration:180K Temperature Model:Coeff a2

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | 180K Temperature Model | Coeff a2 | I2 | –32768 | 32767 | 25759 | — |

**Description**: This is the coefficient of the third power element of the first temperature polynomial.

#### 7.6.1.9.3 Calibration:180K Temperature Model:Coeff a3

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | 180K Temperature Model | Coeff a3 | I2 | –32768 | 32767 | –23593 | — |

**Description**: This is the coefficient of the second power element of the first temperature polynomial.

#### 7.6.1.9.4 Calibration:180K Temperature Model:Coeff a4

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | 180K Temperature Model | Coeff a4 | I2 | –32768 | 32767 | 32175 | — |

**Description**: This is the coefficient of the first power element of the first temperature polynomial.

#### 7.6.1.9.5 Calibration:180K Temperature Model:Coeff a5

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | 180K Temperature Model | Coeff a5 | I2 | –32768 | 32767 | 2090 | — |

**Description**: This is the coefficient of the zeroth power element of the first temperature polynomial.

#### 7.6.1.9.6 Calibration:180K Temperature Model:Coeff b1

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | 180K Temperature Model | Coeff b1 | I2 | –32768 | 32767 | –2055 | — |

**Description**: This is the coefficient of the third power element of the second temperature polynomial.

#### 7.6.1.9.7 Calibration:180K Temperature Model:Coeff b2

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | 180K Temperature Model | Coeff b2 | I2 | –32768 | 32767 | 2955 | — |

**Description**: This is the coefficient of the second power element of the second temperature polynomial.

#### 7.6.1.9.8 Calibration:180K Temperature Model:Coeff b3

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | 180K Temperature Model | Coeff b3 | I2 | –32768 | 32767 | –3427 | — |

**Description**: This is the coefficient of the first power element of the second temperature polynomial.

#### 7.6.1.9.9 Calibration:180K Temperature Model:Coeff b4

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | 180K Temperature Model | Coeff b4 | I2 | –32768 | 32767 | 4385 | — |

**Description**: This is the coefficient of the zeroth power element of the second temperature polynomial.

#### 7.6.1.9.10 Calibration:180K Temperature Model:Adc0

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | 180K Temperature Model | Adc0 | I2 | –32768 | 32767 | 17246 | — |

**Description**: Temperature correction factor corresponding to actual ADC measurement at the calibration temperature, with a scale factor included. With the thermistor attached to TS1 at the calibration temperature, the TS1 Raw ADC Counts (in 32-bit format) is divided by 256, then multiplied by 5/3, and used for this setting.

### *7.6.1.10 Calibration:Custom Temperature Model*

#### 7.6.1.10.1 Calibration:Custom Temperature Model:Coeff a1

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Custom Temperature Model | Coeff a1 | I2 | –32768 | 32767 | 0 | — |

**Description**: This is the coefficient of the fourth power element of the first temperature polynomial.

#### 7.6.1.10.2 Calibration:Custom Temperature Model:Coeff a2

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Custom Temperature Model | Coeff a2 | I2 | –32768 | 32767 | 0 | — |

**Description**: This is the coefficient of the third power element of the first temperature polynomial.

#### 7.6.1.10.3 Calibration:Custom Temperature Model:Coeff a3

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Custom Temperature Model | Coeff a3 | I2 | –32768 | 32767 | 0 | — |

**Description**: This is the coefficient of the second power element of the first temperature polynomial.

#### 7.6.1.10.4 Calibration:Custom Temperature Model:Coeff a4

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Custom Temperature Model | Coeff a4 | I2 | –32768 | 32767 | 0 | — |

**Description**: This is the coefficient of the first power element of the first temperature polynomial.

#### 7.6.1.10.5 Calibration:Custom Temperature Model:Coeff a5

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Custom Temperature Model | Coeff a5 | I2 | –32768 | 32767 | 0 | — |

**Description**: This is the coefficient of the zeroth power element of the first temperature polynomial.

#### 7.6.1.10.6 Calibration:Custom Temperature Model:Coeff b1

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Custom Temperature Model | Coeff b1 | I2 | –32768 | 32767 | 0 | — |

**Description**: This is the coefficient of the third power element of the second temperature polynomial.

#### 7.6.1.10.7 Calibration:Custom Temperature Model:Coeff b2

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Custom Temperature Model | Coeff b2 | I2 | –32768 | 32767 | 0 | — |

**Description**: This is the coefficient of the second power element of the second temperature polynomial.

#### 7.6.1.10.8 Calibration:Custom Temperature Model:Coeff b3

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Custom Temperature Model | Coeff b3 | I2 | –32768 | 32767 | 0 | — |

**Description**: This is the coefficient of the first power element of the second temperature polynomial.

#### 7.6.1.10.9 Calibration:Custom Temperature Model:Coeff b4

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Custom Temperature Model | Coeff b4 | I2 | –32768 | 32767 | 0 | — |

**Description**: This is the coefficient of the zeroth power element of the second temperature polynomial.

#### 7.6.1.10.10 Calibration:Custom Temperature Model:Rc0

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Custom Temperature Model | Rc0 | I2 | –32768 | 32767 | 0 | — |

**Description**: Temperature correction factor corresponding to ideal ADC measurement at the calibration temperature after scaling by 5/3. For example, using calibration temperature of 25C, assuming thermistor value of 10-kOhm, pull-up resistor of 18-kOhm, this is calculated as Rthermistor / (Rthermistor + Rpull-up) * 32767.

#### 7.6.1.10.11 Calibration:Custom Temperature Model:Adc0

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Custom Temperature Model | Adc0 | I2 | –32768 | 32767 | 0 | — |

**Description**: Temperature correction factor corresponding to actual ADC measurement at the calibration temperature, with a scale factor included. With the thermistor attached to TS1 at the calibration temperature, the TS1 Raw ADC Counts (in 32-bit format) is divided by 256, then multiplied by 5/3, and used for this setting.

### *7.6.1.11 Calibration:Current Deadband*

#### 7.6.1.11.1 Calibration:Current Deadband:Coulomb Counter Deadband

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Calibration | Current Deadband | Coulomb Counter Deadband | U1 | 0 | 255 | 9 | 234 nV |

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**Description**: To enable accurate charge accumulation, a deadband threshold is used to filter out signals below the expected noise floor. When the average coulomb counter output is below the deadband threshold, the charge is discarded instead of accumulated. This normally should not be changed.

### 7.6.2 Settings

#### *7.6.2.1 Settings:Fuse*

##### 7.6.2.1.1 Settings:Fuse:Min Blow Fuse Voltage

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Fuse | Min Blow Fuse Voltage | I2 | 0 | 32767 | 500 | cV |

**Description**: The device will normally attempt to blow the fuse only if the stack voltage is above this threshold. If ***Settings:Protection:Protection Configuration[PACK_FUSE]*** is set, pack voltage is used instead of stack voltage. However, if FET failure (CFETF or DFETF) is detected and ***Settings:Protection:Protection Configuration[FETF_FUSE]*** is set, this voltage threshold is ignored.

##### 7.6.2.1.2 Settings:Fuse:Fuse Blow Timeout

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Fuse | Fuse Blow Timeout | U1 | 0 | 255 | 30 | s |

**Description**: When blowing the fuse, the device will assert the fuse blow output for this duration.

0 = Drive fuse blow output indefinitely (no timeout)

All other values = Drive fuse blow output for this many seconds when blowing the fuse

#### *7.6.2.2 Settings:Configuration*

##### 7.6.2.2.1 Settings:Configuration:Power Config

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Configuration | Power Config | H2 | 0x0000 | 0xFFFF | 0x0182 | Hex |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | DPSLP_LDO | DPSLP_LFO | SLEEP |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OTSD | FASTADC | CB_LOOP_SLOW_1 | CB_LOOP_SLOW_0 | LOOP_SLOW_1 | LOOP_SLOW_0 | RSVD_1 | RSVD_0 |

**Table 70. Power Config Register Field Descriptions**

| Bit | Field | Default | Description |
|---|---|---|---|
| 10 | DPSLP_LDO | 0 | Determines whether or not REG1 and REG2 are disabled in DEEPSLEEP mode<br>0 = Disable REG1 and REG2 when entering DEEPSLEEP mode<br>1 = Leave REG1 and REG2 in present state when entering DEEPSLEEP |
| 9 | DPSLP_LFO | 0 | Determines whether or not to disable the Low Frequency Oscillator in DEEPSLEEP mode to conserve power.<br>0 = Disable the Low Frequency Oscillator in DEEPSLEEP mode (recommended)<br>1 = Enable the Low Frequency Oscillator in DEEPSLEEP mode |
| 8 | SLEEP | 1 | Sets the default value of *BatteryStatus()[SLEEP_EN]* which enables or disables SLEEP mode. After initialization, SLEEP_EN can stil be changed through the SLEEP_ENABLE and SLEEP_DISABLE subcommands.<br>0 = Disable SLEEP mode by default<br>1 = Enable SLEEP mode by default |

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**Table 70. Power Config Register Field Descriptions (continued)**

| Bit | Field | Default | Description |
|---|---|---|---|
| 7 | OTSD | 1 | Enables or disables the on-chip over-temperature detection circuit to shut down the device in case of a severe on-chip over-temperature condition.<br>0 = Disable SHUTDOWN from on-chip over-temperature detection circuit (not recommended)<br>1 = Enter SHUTDOWN mode when on-chip over-temperature condition is detected |
| 6 | FASTADC | 0 | Selects ADC conversion speed for voltage and simultaneous current measurements. Higher speed results in lower accuracy.<br>0 = 3 ms per conversion<br>1 = 1.5 ms per conversion |
| 5–4 | CB_LOOP_SLOW_1–CB_LOOP_SLOW_0 | 0 | Selects ADC scan loop speed while cell balancing is active by inserting current-only measurements after each voltage and temperature scan loop. This can be used to slow down voltage measurements while balancing to increase the duty-cycle, since balancing must be paused during measurement of the cell.<br>0 = Full speed<br>1 = Half speed<br>3 = Quarter speed<br>4 = Eighth speed |
| 3–2 | LOOP_SLOW_1–LOOP_SLOW_0 | 0 | Selects normal ADC scan loop speed by inserting current-only measurements after each voltage and temperature scan loop. This setting is used while cell balancing is not active.<br>0 = Full speed<br>1 = Half speed<br>2 = Quarter speed<br>3 = Eighth speed |

#### 7.6.2.2.2 Settings:Configuration:REG12 Config

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Configuration | REG12 Config | H1 | 0x00 | 0xFF | 0x00 | Hex |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| REG2V_2 | REG2V_1 | REG2V_0 | REG2_EN | REG1V_2 | REG1V_1 | REG1V_0 | REG1_EN |

**Description**: Configuration options for the voltage regulator outputs

**Table 71. REG12 Config Register Field Descriptions**

| Bit | Field | Default | Description |
|---|---|---|---|
| 7–5 | REG2V_2–REG2V_0 | 0 | Selects voltage level for REG2 This setting should not be changed while REG2 is enabled.<br>0–3 = 1.8 V<br>4 = 2.5 V<br>5 = 3 V<br>6 = 3.3 V<br>7 = 5 V |
| 4 | REG2_EN | 0 | Configure default state for REG2 output. This setting is reapplied when initializing after reset or DEEPSLEEP mode.<br>0 = REG2 Disabled<br>1 = REG2 Enabled |
| 3–1 | REG1V_2–REG1V_0 | 0 | Selects voltage level for REG1 This setting should not be changed while REG1 is enabled.<br>0–3 = 1.8 V<br>4 = 2.5 V<br>5 = 3 V<br>6 = 3.3 V<br>7 = 5 V |

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**Table 71. REG12 Config Register Field Descriptions (continued)**

| Bit | Field | Default | Description |
|---|---|---|---|
| 0 | REG1_EN | 0 | Configure default state for REG1 output. This setting is reapplied when initializing after reset or DEEPSLEEP mode.<br>0 = REG1 Disabled<br>1 = REG1 Enabled |

#### 7.6.2.2.3 Settings:Configuration:REG0 Config

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Configuration | REG0 Config | H1 | 0x00 | 0x01 | 0x00 | Hex |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | REG0_EN |

**Description**: REG0 (pre-regulator) can be enabled with this configuration option. This must be enabled if the regulator output is used and REGIN is not supplied externally.

**Table 72. REG0 Config Register Field Descriptions**

| Bit | Field | Default | Description |
|---|---|---|---|
| 0 | REG0_EN | 0 | Enable or disable pre-regulator for REG1 and REG2<br>0 = Pre-regulator is disabled<br>1 = Pre-regulator is enabled |

#### 7.6.2.2.4 Settings:Configuration:HWD Regulator Options

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Configuration | HWD Regulator Options | H1 | 0x00 | 0xFF | 0x00 | Hex |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RSVD_0 | RSVD_0 | TOGGLE_OPT_1 | TOGGLE_OPT_0 | TOGGLE_TIME_3 | TOGGLE_TIME_2 | TOGGLE_TIME_1 | TOGGLE_TIME_0 |

**Description**: Configures the action to be taken when the Host Watchdog protection is triggered. This can be configured turn the REG1 and REG2 output off and on to potentially reset a host microcontroller that has stopped communicating.

**Table 73. HWD Regulator Options Register Field Descriptions**

| Bit | Field | Default | Description |
|---|---|---|---|
| 5–4 | TOGGLE_OPT_1–TOGGLE_OPT_0 | 0 | Action to take when HWD protection is triggered<br>0 = Take no action on REG1 and REG2 regulators.<br>1 = Turn REG1 and REG2 regulators off.<br>2 = Turn REG1 and REG2 regulators off for configured duration and then back on again.<br>3 = Reserved. Do not use. |
| 3–0 | TOGGLE_TIME_3–TOGGLE_TIME_0 | 0 | How long to keep REG1 and REG2 regulators off when configured to toggle.<br>0 = Turn REG1 and REG2 regulators off and do not turn back on again.<br>1–15 = Turn REG1 and REG2 regulators back on again after this many seconds. |

#### 7.6.2.2.5 Settings:Configuration:Comm Type

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Configuration | Comm Type | U1 | 0x00 | 0x1F | 0 | — |

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**Description**: Selects the active communication mode. This mode is applied on reset or when the SWAP_COMM_MODE command is received.

0x00 = Default ($I^2C$ Fast, for use above 100 kHz bus speed)

0xff = Default ($I^2C$ Fast, for use above 100 kHz bus speed)

0x03 = HDQ (using ALERT pin)

0x04 = HDQ (using HDQ pin)

0x07 = $I^2C$ (for use up to 100 kHz bus speed)

0x08 = $I^2C$ Fast (for use above 100 kHz bus speed)

0x09 = $I^2C$ Fast with Timeouts (for use above 100 kHz bus speed)

0x0f = SPI

0x10 = SPI with CRC

0x11 = $I^2C$ with CRC (for use up to 100 kHz bus speed)

0x12 = $I^2C$ Fast with CRC (for use above 100 kHz bus speed)

0x1e = $I^2C$ with Timeouts (for use up to 100 kHz bus speed)

All other values = Reserved. Do not use

#### 7.6.2.2.6 Settings:Configuration:I2C Address

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Configuration | I2C Address | U1 | 0x00 | 0xFF | 0 | — |

**Description**: Sets the device address for $I^2C$-based communication modes. This applied on reset or when SWAP_COMM_MODE subcommand is received.

0 = Use default $I^2C$ device address (0x10)

All other values = Use specified $I^2C$ device address

#### 7.6.2.2.7 Settings:Configuration:Comm Idle Time

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Configuration | Comm Idle Time | U1 | 0 | 255 | 0 | s |

**Description**: Configures the number of seconds to leave the High-Frequency Oscillator enabled after communications. Note: the one-second timer is asynchronous to communications, so the oscillator may turn off up to one second after than this delay. For $I^2C$, this can reduce clock stretching at the expense of higher power consumption. For SPI, setting this parameter to a nonzero value enables a shorter time between Chip Select assertion and the first clock edge after the first transaction.

0 = High-Frequency Oscillator not left enabled for extra time after communications.

All other values = High-Frequency Oscillator left enabled for up to this many seconds after communications.

#### 7.6.2.2.8 Settings:Configuration:CFETOFF Pin Config

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Configuration | CFETOFF Pin Config | H1 | 0x00 | 0xFF | 0x00 | Hex |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OPT5 | OPT4 | OPT3 | OPT2 | OPT1 | OPT0 | PIN_FXN1 | PIN_FXN0 |

ADVANCE INFORMATION

**Description**: This parameter configures the CFETOFF pin functionality. Depending on the pin function selected, the meaning of the OPT bitfield changes.

**Table 74. CFETOFF Pin Config Register Field Descriptions**

| Bit | Field | Default | Description |
|---|---|---|---|
| 7–2 | OPT5–OPT0 | 0 | These bits configure the options for the selected pin function.<br>OPT[5]:<br>Polarity when configured for CFETOFF (does not affect GPO mode).<br>• 0 = selects active-high.<br>• 1 = selects active-low.<br>OPT[4]:<br>• Unused.<br>OPT[3]:<br>• 0 = output high drive uses REG18.<br>• 1 = output high drive uses REG1.<br>OPT[2]:<br>• 0 = weak pull-up to REG1 is disabled.<br>• 1 = weak pull-up to REG1 is enabled.<br>Note: this should only be selected if OPT[3] and OPT[1] = 0.<br>OPT[1]:<br>• 0 = pin drives tri-state when controlled to be driven *high* (not available when OPT[3] is set).<br>• 1 = pin drives active-high when controlled to be driven *high*.<br>OPT[0]:<br>• 0 = weak pulldown to VSS is disabled.<br>• 1 = weak pulldown to VSS is enabled.<br>When a pin is selected for ADCIN or thermistor functionality, the OPT[5:0] bits are used as shown below.<br>OPT[5:4]:<br>Pull-up control<br>• 00 = selects 18-kOhm pull-up for thermistor measurement.<br>• 01 = selects 180-kOhm pull-up for thermistor measurement.<br>• 10 = selects no pull-up (used for ADCIN functionality).<br>OPT[3:2]:<br>Polynomial selection for thermistor temperature measurement.<br>• 00 = selects the 18K Temperature Model.<br>• 01 = selects the 180K Temperature Model.<br>• 10 = selects the Custom Temperature Model.<br>• 11 = no polynomial is used, raw ADC counts are reported.<br>OPT[1:0]:<br>Measurement type<br>• 00 = general purpose ADC input<br>• 01 = thermistor temperature measurement, used for cell temperature protections.<br>• 10 = thermistor temperature measurement, reported but not used for protections.<br>• 11 = thermistor temperature measurement, used for FET temperature protection. |
| 1–0 | PIN_FXN1–PIN_FXN0 | 0 | These bits configure which function this pin is used for.<br>0 = SPI_CS or Unused<br>1 = General Purpose Output<br>2 = CFETOFF<br>3 = ADC Input or Thermistor |

### 7.6.2.2.9 Settings:Configuration:DFETOFF Pin Config

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Configuration | DFETOFF Pin Config | H1 | 0x00 | 0xFF | 0x00 | Hex |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OPT5 | OPT4 | OPT3 | OPT2 | OPT1 | OPT0 | PIN_FXN1 | PIN_FXN0 |

ADVANCE INFORMATION

**Description**: This parameter configures the DFETOFF pin functionality. Depending on the pin function selected, the meaning of the OPT bitfield changes.

**Table 75. DFETOFF Pin Config Register Field Descriptions**

| Bit | Field | Default | Description |
|---|---|---|---|
| 7–2 | OPT5–OPT0 | 0 | These bits configure the options for the selected pin function.<br>OPT[5]:<br>Polarity when configured for DFETOFF (does not affect GPO mode).<br>• 0 = selects active-high.<br>• 1 = selects active-low.<br>OPT[4]:<br>• 0 = selects DFETOFF functionality.<br>• 1 = selects BOTHOFF functionality.<br>OPT[3]:<br>• 0 = output high drive uses REG18.<br>• 1 = output high drive uses REG1.<br>OPT[2]:<br>• 0 = weak pull-up to REG1 is disabled.<br>• 1 = weak pull-up to REG1 is enabled.<br>Note: this should only be selected if OPT[3] and OPT[1] = 0:<br>OPT[1]:<br>• 0 = pin drives tri-state when controlled to be driven *high* (not available when OPT[3] is set).<br>• 1 = pin drives active-high when controlled to be driven *high*.<br>OPT[0]:<br>• 0 = weak pulldown to VSS is disabled.<br>• 1 = weak pulldown to VSS is enabled.<br>When a pin is selected for ADCIN or thermistor functionality, the OPT[5:0] bits are used as shown below.<br>OPT[5:4]:<br>Pull-up control<br>• 00 = selects 18-kOhm pull-up for thermistor measurement.<br>• 01 = selects 180-kOhm pull-up for thermistor measurement.<br>• 10 = selects no pull-up (used for ADCIN functionality).<br>OPT[3:2]:<br>Polynomial selection for thermistor temperature measurement<br>• 00 = selects the 18K Temperature Model.<br>• 01 = selects the 180K Temperature Model.<br>• 10 = selects the Custom Temperature Model.<br>• 11 = no polynomial is used, raw ADC counts are reported.<br>OPT[1:0]:<br>Measurement type<br>• 00 = general purpose ADC input<br>• 01 = thermistor temperature measurement, used for cell temperature protections.<br>• 10 = thermistor temperature measurement, reported but not used for protections.<br>• 11 = thermistor temperature measurement, used for FET temperature protection. |
| 1–0 | PIN_FXN1–PIN_FXN0 | 0 | These bits configure which function this pin is used for.<br>0 = Unused<br>1 = General Purpose Output<br>2 = DFETOFF or BOTHOFF<br>3 = ADC Input or Thermistor |

#### 7.6.2.2.10 Settings:Configuration:ALERT Pin Config

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Configuration | ALERT Pin Config | H1 | 0x00 | 0xFF | 0x00 | Hex |

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| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OPT5 | OPT4 | OPT3 | OPT2 | OPT1 | OPT0 | PIN_FXN1 | PIN_FXN0 |

**Description**: This parameter configures the ALERT pin functionality. Depending on the pin function selected, the meaning of the OPT bitfield changes.

**Table 76. ALERT Pin Config Register Field Descriptions**

| Bit | Field | Default | Description |
|---|---|---|---|
| 7–2 | OPT5–OPT0 | 0 | These bits configure the options for the selected pin function.<br>OPT[5]:<br>Polarity when configured for ALERT (does not affect GPO mode).<br>• 0 = selects active-high.<br>• 1 = selects active-low.<br>OPT[4]:<br>Unused<br>OPT[3]:<br>• 0 = output high drive uses REG18.<br>• 1 = output high drive uses REG1.<br>OPT[2]:<br>• 0 = weak pull-up to REG1 is disabled.<br>• 1 = weak pull-up to REG1 is enabled.<br>Note: this should only be selected if OPT[3] and OPT[1] = 0.<br>OPT[1]:<br>• 0 = pin drives tri-state when controlled to be driven *high* (not available when OPT[3] is set).<br>• 1 = pin drives active-high when controlled to be driven *high*.<br>OPT[0]:<br>• 0 = weak pulldown to VSS is disabled.<br>• 1 = weak pulldown to VSS is enabled.<br>When a pin is selected for ADCIN or thermistor functionality, the OPT[5:0] bits are used as shown below.<br>OPT[5:4]:<br>Pull-up control<br>• 00 = selects 18-kOhm pull-up for thermistor measurement.<br>• 01 = selects 180-kOhm pull-up for thermistor measurement.<br>• 10 = selects no pull-up (used for ADCIN functionality).<br>OPT[3:2]:<br>Polynomial selection for thermistor temperature measurement.<br>• 00 = selects the 18K Temperature Model.<br>• 01 = selects the 180K Temperature Model.<br>• 10 = selects the Custom Temperature Model.<br>• 11 = no polynomial is used, raw ADC counts are reported.<br>OPT[1:0]:<br>Measurement type<br>• 00 = general purpose ADC input.<br>• 01 = thermistor temperature measurement, used for cell temperature protections.<br>• 10 = thermistor temperature measurement, reported but not used for protections.<br>• 11 = thermistor temperature measurement, used for FET temperature protection. |
| 1–0 | PIN_FXN1–PIN_FXN0 | 0 | These bits configure which function this pin is used for.<br>0 = HDQ or Unused<br>1 = General Purpose Output<br>2 = ALERT<br>3 = ADC Input or Thermistor |

#### 7.6.2.2.11 Settings:Configuration:TS1 Config

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Configuration | TS1 Config | H1 | 0x00 | 0xFF | 0x07 | Hex |

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| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OPT5 | OPT4 | OPT3 | OPT2 | OPT1 | OPT0 | PIN_FXN1 | PIN_FXN0 |

**Description**: This parameter configures the TS1 pin functionality.

**Table 77. TS1 Config Register Field Descriptions**

| Bit | Field | Default | Description |
|---|---|---|---|
| 7–2 | OPT5–OPT0 | 1 | The OPT[5:0] bits configure the options for the TS1 pin function.<br>OPT[5:4]:<br>Pull-up control<br>• 00 = selects 18-kOhm pull-up for thermistor measurement.<br>• 01 = selects 180-kOhm pull-up for thermistor measurement.<br>• 10 = selects no pull-up (used for ADCIN functionality).<br>OPT[3:2]:<br>Polynomial selection for thermistor temperature measurement<br>• 00 = selects the 18K Temperature Model.<br>• 01 = selects the 180K Temperature Model.<br>• 10 = selects the Custom Temperature Model.<br>• 11 = no polynomial is used, raw ADC counts are reported.<br>OPT[1:0]:<br>Measurement type<br>• 00 = general purpose ADC input<br>• 01 = thermistor temperature measurement, used for cell temperature protections<br>• 10 = thermistor temperature measurement, reported but not used for protections<br>• 11 = thermistor temperature measurement, used for FET temperature protection |
| 1–0 | PIN_FXN1–PIN_FXN0 | 3 | These bits configure which function this pin is used for.<br>0 = Unused<br>1 = Unused<br>2 = Unused<br>3 = ADC Input or Thermistor |

#### 7.6.2.2.12 Settings:Configuration:TS2 Config

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Configuration | TS2 Config | H1 | 0x00 | 0xFF | 0x00 | Hex |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OPT5 | OPT4 | OPT3 | OPT2 | OPT1 | OPT0 | PIN_FXN1 | PIN_FXN0 |

ADVANCE INFORMATION

**Description**: This parameter configures the TS2 pin functionality.

**Table 78. TS2 Config Register Field Descriptions**

| Bit | Field | Default | Description |
|---|---|---|---|
| 7–2 | OPT5–OPT0 | 0 | The OPT[5:0] bits configure the options for the TS2 pin function.<br>OPT[5:4]:<br>Pull-up control<br>• 00 = selects 18-kOhm pull-up for thermistor measurement.<br>• 01 = selects 180-kOhm pull-up for thermistor measurement.<br>• 10 = selects no pull-up (used for ADCIN functionality).<br>OPT[3:2]:<br>Polynomial selection for thermistor temperature measurement<br>• 00 = selects the 18K Temperature Model.<br>• 01 = selects the 180K Temperature Model.<br>• 10 = selects the Custom Temperature Model.<br>• 11 = no polynomial is used, raw ADC counts are reported.<br>OPT[1:0]:<br>Measurement type<br>• 00 = general purpose ADC input.<br>• 01 = thermistor temperature measurement, used for cell temperature protections.<br>• 10 = thermistor temperature measurement, reported but not used for protections.<br>• 11 = thermistor temperature measurement, used for FET temperature protection. |
| 1–0 | PIN_FXN1–PIN_FXN0 | 0 | These bits configure which function this pin is used for.<br>0 = Unused<br>1 = Unused<br>2 = Unused<br>3 = ADC Input or Thermistor |

### 7.6.2.2.13 Settings:Configuration:TS3 Config

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Configuration | TS3 Config | H1 | 0x00 | 0xFF | 0x00 | Hex |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OPT5 | OPT4 | OPT3 | OPT2 | OPT1 | OPT0 | PIN_FXN1 | PIN_FXN0 |

**Description**: This parameter configures the TS3 pin functionality.

**Table 79. TS3 Config Register Field Descriptions**

| Bit | Field | Default | Description |
|---|---|---|---|
| 7–2 | OPT5–OPT0 | 0 | The OPT[5:0] bits configure the options for the TS3 pin function.<br>OPT[5:4]:<br>Pull-up control<br>• 00 = selects 18-kOhm pull-up for thermistor measurement.<br>• 01 = selects 180-kOhm pull-up for thermistor measurement.<br>• 10 = selects no pull-up (used for ADCIN functionality).<br>OPT[3:2]:<br>Polynomial selection for thermistor temperature measurement<br>• 00 = selects the 18K Temperature Model.<br>• 01 = selects the 180K Temperature Model.<br>• 10 = selects the Custom Temperature Model.<br>• 11 = no polynomial is used, raw ADC counts are reported.<br>OPT[1:0]:<br>Measurement type<br>• 00 = general purpose ADC input<br>• 01 = thermistor temperature measurement, used for cell temperature protections.<br>• 10 = thermistor temperature measurement, reported but not used for protections.<br>• 11 = thermistor temperature measurement, used for FET temperature protection. |

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**Table 79. TS3 Config Register Field Descriptions (continued)**

| Bit | Field | Default | Description |
|---|---|---|---|
| 1–0 | PIN_FXN1–PIN_FXN0 | 0 | These bits configure which function this pin is used for.<br>0 = Unused<br>1 = Unused<br>2 = Unused<br>3 = ADC Input or Thermistor |

#### 7.6.2.2.14 Settings:Configuration:HDQ Pin Config

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Configuration | HDQ Pin Config | H1 | 0x00 | 0xFF | 0x00 | Hex |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OPT5 | OPT4 | OPT3 | OPT2 | OPT1 | OPT0 | PIN_FXN1 | PIN_FXN0 |

ADVANCE INFORMATION

**Description**: This parameter configures the HDQ pin functionality. Depending on the pin function selected, the meaning of the OPT bitfield changes.

**Table 80. HDQ Pin Config Register Field Descriptions**

| Bit | Field | Default | Description |
|---|---|---|---|
| 7–2 | OPT5–OPT0 | 0 | These bits configure the options for the selected pin function.<br>OPT[5]:<br>Polarity when configured for HDQ (does not affect GPO mode)<br>• 0 = selects active-high.<br>• 1 = selects active-low.<br>OPT[4]:<br>Unused<br>OPT[3]:<br>• 0 = output high drive uses REG18.<br>• 1 = output high drive uses REG1.<br>OPT[2]:<br>• 0 = weak pull-up to REG1 is disabled.<br>• 1 = weak pull-up to REG1 is enabled.<br>Note: this should only be selected if OPT[3] and OPT[1] = 0.<br>OPT[1]:<br>• 0 = pin drives tri-state when controlled to be driven *high*(not available when OPT[3] is set).<br>• 1 = pin drives active-high when controlled to be driven *high*.<br>OPT[0]:<br>• 0 = weak pulldown to VSS is disabled.<br>• 1 = weak pulldown to VSS is enabled.<br>When a pin is selected for ADCIN or thermistor functionality, the OPT[5:0] bits are used as shown below.<br>OPT[5:4]:<br>Pull-up control<br>• 00 = selects 18-kOhm pull-up for thermistor measurement.<br>• 01 = selects 180-kOhm pull-up for thermistor measurement.<br>• 10 = selects no pull-up (used for ADCIN functionality).<br>OPT[3:2]:<br>Polynomial selection for thermistor temperature measurement.<br>• 00 = selects the 18K Temperature Model.<br>• 01 = selects the 180K Temperature Model.<br>• 10 = selects the Custom Temperature Model.<br>• 11 = no polynomial is used, raw ADC counts are reported.<br>OPT[1:0]:<br>Measurement type<br>• 00 = general purpose ADC input.<br>• 01 = thermistor temperature measurement, used for cell temperature protections.<br>• 10 = thermistor temperature measurement, reported but not used for protections.<br>• 11 = thermistor temperature measurement, used for FET temperature protection. |
| 1–0 | PIN_FXN1–PIN_FXN0 | 0 | These bits configure which function this pin is used for.<br>0 = HDQ or SPI_MOSI or Unused<br>1 = General Purpose Output<br>2 = Unused<br>3 = ADC Input or Thermistor |

### 7.6.2.2.15 Settings:Configuration:DCHG Pin Config

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Configuration | DCHG Pin Config | H1 | 0x00 | 0xFF | 0x00 | Hex |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OPT5 | OPT4 | OPT3 | OPT2 | OPT1 | OPT0 | PIN_FXN1 | PIN_FXN0 |

ADVANCE INFORMATION

**Description**: This parameter configures the DCHG pin functionality. Depending on the pin function selected, the meaning of the OPT bitfield changes.

**Table 81. DCHG Pin Config Register Field Descriptions**

| Bit | Field | Default | Description |
|---|---|---|---|
| 7–2 | OPT5–OPT0 | 0 | These bits configure the options for the selected pin function.<br>OPT[5]:<br>Polarity when configured for HDQ (does not affect GPO mode)<br>• 0 = selects active-high.<br>• 1 = selects active-low.<br>OPT[4]:<br>Unused<br>OPT[3]:<br>• 0 = output high drive uses REG18.<br>• 1 = output high drive uses REG1.<br>OPT[2]:<br>• 0 = weak pull-up to REG1 is disabled.<br>• 1 = weak pull-up to REG1 is enabled.<br>Note: this should only be selected if OPT[3] and OPT[1] = 0.<br>OPT[1]:<br>• 0 = pin drives tri-state when controlled to be driven *high*(not available when OPT[3] is set).<br>• 1 = pin drives active-high when controlled to be driven *high*.<br>OPT[0]:<br>• 0 = weak pulldown to VSS is disabled.<br>• 1 = weak pulldown to VSS is enabled.<br>When a pin is selected for ADCIN or thermistor functionality, the OPT[5:0] bits are used as shown below.<br>OPT[5:4]:<br>Pull-up control<br>• 00 = selects 18-kOhm pull-up for thermistor measurement.<br>• 01 = selects 180-kOhm pull-up for thermistor measurement.<br>• 10 = selects no pull-up (used for ADCIN functionality).<br>OPT[3:2]:<br>Polynomial selection for thermistor temperature measurement.<br>• 00 = selects the 18K Temperature Model.<br>• 01 = selects the 180K Temperature Model.<br>• 10 = selects the Custom Temperature Model.<br>• 11 = no polynomial is used, raw ADC counts are reported.<br>OPT[1:0]:<br>Measurement type<br>• 00 = general purpose ADC input.<br>• 01 = thermistor temperature measurement, used for cell temperature protections.<br>• 10 = thermistor temperature measurement, reported but not used for protections.<br>• 11 = thermistor temperature measurement, used for FET temperature protection. |
| 1–0 | PIN_FXN1–PIN_FXN0 | 0 | These bits configure which function this pin is used for.<br>0 = Unused<br>1 = General Purpose Output<br>2 = DCHG<br>3 = ADC Input or Thermistor |

### 7.6.2.2.16 Settings:Configuration:DDSG Pin Config

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Configuration | DDSG Pin Config | H1 | 0x00 | 0xFF | 0x00 | Hex |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OPT5 | OPT4 | OPT3 | OPT2 | OPT1 | OPT0 | PIN_FXN1 | PIN_FXN0 |

**Description**: This parameter configures the DDSG pin functionality. Depending on the pin function selected, the meaning of the OPT bitfield changes.

**Table 82. DDSG Pin Config Register Field Descriptions**

| Bit | Field | Default | Description |
|---|---|---|---|
| 7–2 | OPT5–OPT0 | 0 | These bits configure the options for the selected pin function.<br>OPT[5]:<br>Polarity when configured for DDSG (does not affect GPO mode).<br>• 0 = selects active-high.<br>• 1 = selects active-low.<br>OPT[4]:<br>• Unused.<br>OPT[3]:<br>• 0 = output high drive uses REG18.<br>• 1 = output high drive uses REG1.<br>OPT[2]:<br>• 0 = weak pull-up to REG1 is disabled.<br>• 1 = weak pull-up to REG1 is enabled.<br>Note: this should only be selected if OPT[3] and OPT[1] = 0.<br>OPT[1]:<br>• 0 = pin drives tri-state when controlled to be driven *high* (not available when OPT[3] is set).<br>• 1 = pin drives active-high when controlled to be driven *high*.<br>OPT[0]:<br>• 0 = weak pulldown to VSS is disabled.<br>• 1 = weak pulldown to VSS is enabled.<br>When a pin is selected for ADCIN or thermistor functionality, the OPT[5:0] bits are used as shown below.<br>OPT[5:4]:<br>Pull-up control<br>• 00 = selects 18-kOhm pull-up for thermistor measurement.<br>• 01 = selects 180-kOhm pull-up for thermistor measurement.<br>• 10 = selects no pull-up (used for ADCIN functionality).<br>OPT[3:2]:<br>Polynomial selection for thermistor temperature measurement.<br>• 00 = selects the 18K Temperature Model.<br>• 01 = selects the 180K Temperature Model.<br>• 10 = selects the Custom Temperature Model.<br>• 11 = no polynomial is used, raw ADC counts are reported.<br>OPT[1:0]:<br>Measurement type<br>• 00 = general purpose ADC input.<br>• 01 = thermistor temperature measurement, used for cell temperature protections.<br>• 10 = thermistor temperature measurement, reported but not used for protections.<br>• 11 = thermistor temperature measurement, used for FET temperature protection. |
| 1–0 | PIN_FXN1–PIN_FXN0 | 0 | These bits configure which function this pin is used for.<br>0 = Unused<br>1 = General Purpose Output<br>2 = DDSG<br>3 = ADC Input or Thermistor |

### 7.6.2.2.17 Settings:Configuration:DA Configuration

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Configuration | DA Configuration | H1 | 0x00 | 0xFF | 0x05 | Hex |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RSVD_0 | RSVD_0 | RSVD_0 | TINT_FETT | TINT_EN | USER_VOLTS_CV | USER_AMPS_1 | USER_AMPS_0 |

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**Table 83. DA Configuration Register Field Descriptions**

| Bit | Field | Default | Description |
|---|---|---|---|
| 4 | TINT_FETT | 0 | TINT_FETT enables the internal temperature source to be used as the "FET Temperature." TINT_EN must also be set for this to apply. When TINT_EN = 0, this bit is ignored. When configured for FET temperature, it is not factored into minimum, maximum, and average cell temperature calculations.<br>0 = Internal temperature is not used for "FET Temperature"<br>1 = Internal temperature is used for "FET Temperature" if TINT_EN is also set |
| 3 | TINT_EN | 0 | TINT_EN enables the internal temperature source to be used as the “Cell Temperature” for protections and logic that use minimum, maximum, or average temperature.<br>0 = Internal temperature is not used for "Cell Temperature"<br>1 = Internal temperature is used for "Cell Temperature" |
| 2 | USER_VOLTS_CV | 1 | Some of the BQ769x2 family of devices support high voltages. To ensure the Top-of-Stack, PACK, and LD pin voltages fit in a signed 16-bit integer type, their units are configurable. This configurable unit is called user-volts and can be set to either centivolts or millivolts. For applications which will not exceed 32 V, millivolts may be used. Other applications should use centivolts to avoid saturating at 32767 mV.<br>0 = Millivolt (1 mV) units are selected for user-volts<br>1 = Centivolt (10 mV) units are selected for user-volts |
| 1–0 | USER_AMPS_1–USER_AMPS_0 | 1 | In order to support a wide range of applications, the device allows its units of current to be configurable. This configurable unit is called user-amps and can be mapped to different units of current. This extends the range of the reported 16-bit current to allow it to scale with the anticipated load.<br>0 = Decimilliamp (0.1 mA) units are selected for user-amps.<br>1 = Milliamp (1 mA) units are selected for user-amps.<br>2 = Centiamp (10 mA) units are selected for user-amps.<br>3 = Deciamp (100 mA) units are selected for user-amps. |

#### 7.6.2.2.18 Settings:Configuration:Vcell Mode

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Configuration | Vcell Mode | H2 | 0x0000 | 0x03FF | 0x001F | Hex |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | Cell 10 Mode | Cell 9 Mode |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Cell 8 Mode | Cell 7 Mode | Cell 6 Mode | Cell 5 Mode | Cell 4 Mode | Cell 3 Mode | Cell 2 Mode | Cell 1 Mode |

**Description**: Not every system will use all of the cell input pins. If the system has fewer cells than the device supports, some VC input pins may be shorted together or used to measure interconnect resistance between cells. To prevent action being taken for cell under-voltage conditions on pins that are shorted or used to measure interconnect resistance, the corresponding Vcell mode bit should be cleared.

**Table 84. Vcell Mode Register Field Descriptions**

| Bit | Field | Default | Description |
|---|---|---|---|
| 9 | Cell 10 Mode | 0 | 0 = A cell is not connected between VC10 and VC9. Disable protections on Cell 10.<br>1 = A cell is connected between VC10 and VC9. Enable protections on Cell 10. |
| 8 | Cell 9 Mode | 0 | 0 = A cell is not connected between VC9 and VC8. Disable protections on Cell 9.<br>1 = A cell is connected between VC9 and VC8. Enable protections on Cell 9. |
| 7 | Cell 8 Mode | 0 | 0 = A cell is not connected between VC8 and VC7. Disable protections on Cell 8.<br>1 = A cell is connected between VC8 and VC7. Enable protections on Cell 8. |
| 6 | Cell 7 Mode | 0 | 0 = A cell is not connected between VC7 and VC6. Disable protections on Cell 7.<br>1 = A cell is connected between VC7 and VC6. Enable protections on Cell 7. |
| 5 | Cell 6 Mode | 0 | 0 = A cell is not connected between VC6 and VC5. Disable protections on Cell 6.<br>1 = A cell is connected between VC6 and VC5. Enable protections on Cell 6. |

**Table 84. Vcell Mode Register Field Descriptions (continued)**

| Bit | Field | Default | Description |
|---|---|---|---|
| 4 | Cell 5 Mode | 1 | 0 = A cell is not connected between VC5 and VC4. Disable protections on Cell 5.<br>1 = A cell is connected between VC5 and VC4. Enable protections on Cell 5. |
| 3 | Cell 4 Mode | 1 | 0 = A cell is not connected between VC4 and VC3. Disable protections on Cell 4.<br>1 = A cell is connected between VC4 and VC3. Enable protections on Cell 4. |
| 2 | Cell 3 Mode | 1 | 0 = A cell is not connected between VC3 and VC2. Disable protections on Cell 3.<br>1 = A cell is connected between VC3 and VC2. Enable protections on Cell 3. |
| 1 | Cell 2 Mode | 1 | 0 = A cell is not connected between VC2 and VC1. Disable protections on Cell 2.<br>1 = A cell is connected between VC2 and VC1. Enable protections on Cell 2. |
| 0 | Cell 1 Mode | 1 | 0 = A cell is not connected between VC1 and VC0. Disable protections on Cell 1.<br>1 = A cell is connected between VC1 and VC0. Enable protections on Cell 1. |

#### 7.6.2.2.19 Settings:Configuration:CC3 Samples

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Configuration | CC3 Samples | U1 | 2 | 255 | 80 | Num |

**Description**: The device provides an averaged current reading (CC3) over a configurable number of CC2 Current samples. This parameter defines the number of samples that are accumulated before calculating a new average.

### *7.6.2.3 Settings:Protection*

#### 7.6.2.3.1 Settings:Protection:Protection Configuration

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Protection | Protection Configuration | H2 | 0x0000 | 0x07FF | 0x0002 | Hex |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | SCDL_CURR_RECOV | OCDL_CURR_RECOV | FETF_FUSE |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PACK_FUSE | RSVD_0 | PF_OTP | PF_FUSE | PF_DPSLP | PF_REGS | PF_FETS | RSVD_0 |

**Table 85. Protection Configuration Register Field Descriptions**

| Bit | Field | Default | Description |
|---|---|---|---|
| 10 | SCDL_CURR_RECOV | 0 | The SCD Latch fault may recover based on load removal detection on the LD pin, by host command, or by charge current. When the current-based recovery mechanism is not desired, it can be disabled by clearing this bit.<br>0 = SCDL does not recover based on charge current.<br>1 = SCDL recovers when current is greater than or equal to ***Protections:SCDL:Recovery Threshold*** for ***Protections:SCDL:Recovery Time***. |
| 9 | OCDL_CURR_RECOV | 0 | The OCD Latch fault may recover based on load removal detection on the LD pin, by host command, or by charge current. When the current-based recovery mechanism is not desired, it can be disabled by clearing this bit.<br>0 = OCDL does not recover based on charge current.<br>1 = OCDL recovers when current is greater than or equal to ***Protections:OCDL:Recovery Threshold*** for ***Protections:OCDL:Recovery Time***. |

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**Table 85. Protection Configuration Register Field Descriptions (continued)**

| Bit | Field | Default | Description |
|---|---|---|---|
| 8 | FETF_FUSE | 0 | When a Permanent Failure has been detected, the device may be configured to blow the fuse. This normally requires the voltage being above ***Settings:Fuse:Min Blow Fuse Voltage***. When this bit is set and a FET failure occurs (CFETF or DFETF), the voltage requirement is bypassed.<br>0 = Voltage must be above a threshold to blow the fuse when CFETF or DFETF trips.<br>1 = If configured to blow the fuse and CFETF or DFETF occurs, fuse blow is attempted regardless of voltage. |
| 7 | PACK_FUSE | 0 | The fuse is typically located on the BAT side of the FETs, so the device monitors the Top of Stack voltage to determine if fuse blow is possible. However, some systems may place the fuse on the PACK side, in which case the PACK pin voltage should be monitored to determine if fuse blow is possible. Setting this bit causes the device to use the PACK pin voltage instead of the Top of Stack pin voltage for this comparison.<br>0 = Top of Stack voltage must be above ***Settings:Fuse:Min Blow Fuse Voltage*** in order to blow the fuse.<br>1 = PACK voltage must be above ***Settings:Fuse:Min Blow Fuse Voltage*** in order to blow the fuse. |
| 5 | PF_OTP | 0 | Since the device stores Permanent Failure status in RAM, that status would be lost when the device resets. To mitigate this, the device can write Permanent Failure status to OTP when this bit is set. OTP programming may be delayed in low-voltage and high-temperature conditions until OTP programming can reliably be accomplished. Note: writes to OTP during operation are only allowed if ***Settings:Manufacturing:Mfg Status Init[OTPW_EN]*** is set. If this bit is set but ***Settings:Manufacturing:Mfg Status Init[OTPW_EN]*** is clear, Permanent Failure status is saved to RAM that is preserved across a partial reset but will not be programmed to OTP. If this bit is not set, Permanent Failure status will be lost on any reset, including a partial reset through the RST_SHUT pin.<br>0 = Permanent Failure status is lost on reset.<br>1 = Permanent Failure status is preserved across reset when possible. |
| 3 | PF_DPSLP | 0 | Normally, a Permanent Failure causes the FETs to remain off indefinitely and the fuse may be blown. In that situation, there is no further action that would be taken on further monitoring operations. Additionally, charging would no longer be possible. To avoid rapidly draining the battery, the device may be configured to enter DEEPSLEEP mode when a Permanent Failure occurs. DEEPSLEEP will still be delayed until after fuse blow and OTP programming are completed if those options are enabled.<br>0 = Device does not automatically enter DEEPSLEEP mode when a Permanent Failure occurs.<br>1 = Device automatically enters DEEPSLEEP mode when a Permanent Failure occurs. |
| 4 | PF_FUSE | 0 | When a Permanent Failure occurs, the device may be configured to blow the fuse when voltage conditions are met.<br>0 = Permanent Failure does not cause the device to blow the fuse.<br>1 = Permanent Failure causes the device to blow the fuse. |
| 2 | PF_REGS | 0 | When a Permanent Failure occurs, the device may be configured to either turn the regulators off or to leave them in their present state. Once disabled, they may still be re-enabled through command.<br>0 = Permanent Failure does not cause the device to turn the regulators off.<br>1 = Permanent Failure causes the device to turn the regulators off. |
| 1 | PF_FETS | 1 | When a Permanent Failure occurs, the device normally will turn the FETs off. An option is provided to disable this behavior if the host wants to maintain greater control.<br>0 = Permanent Failure does not cause the device to turn the FETs off.<br>1 = Permanent Failure causes the device to turn the FETs off. |

#### 7.6.2.3.2 Settings:Protection:Enabled Protections A

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Protection | Enabled Protections A | U1 | 0x00 | 0xFF | 0x88 | Hex |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SCD | OCD2 | OCD1 | OCC | COV | CUV | RSVD_0 | RSVD_0 |

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**Description**: This bitfield enables or disables various protections. Protections which are enabled will set their corresponding Safety Status flags. Note: ***Settings:Protection:CHG FET Protections A*** and ***Settings:Protection:DSG FET Protections A*** must be appropriately configured to control the FET action taken when these faults are detected.

**Table 86. Enabled Protections A Register Field Descriptions**

| Bit | Field | Default | Description |
|---|---|---|---|
| 7 | SCD | 1 | Short Circuit in Discharge Protection<br>0 = Disabled<br>1 = Enabled |
| 6 | OCD2 | 0 | Overcurrent in Discharge 2nd Tier Protection<br>0 = Disabled<br>1 = Enabled |
| 5 | OCD1 | 0 | Overcurrent in Discharge 1st Tier Protection<br>0 = Disabled<br>1 = Enabled |
| 4 | OCC | 0 | Overcurrent in Charge Protection<br>0 = Disabled<br>1 = Enabled |
| 3 | COV | 1 | Cell Overvoltage Protection<br>0 = Disabled<br>1 = Enabled |
| 2 | CUV | 0 | Cell Undervoltage Protection<br>0 = Disabled<br>1 = Enabled |

#### 7.6.2.3.3 Settings:Protection:Enabled Protections B

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Protection | Enabled Protections B | U1 | 0x00 | 0xFF | 0x00 | Hex |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OTF | OTINT | OTD | OTC | RSVD_0 | UTINT | UTD | UTC |

**Description**: This bitfield enables or disables various protections. Protections which are enabled will set their corresponding Safety Status flags. Note: ***Settings:Protection:CHG FET Protections B*** and ***Settings:Protection:DSG FET Protections B*** must be appropriately configured to control the FET action taken when these faults are detected.

**Table 87. Enabled Protections B Register Field Descriptions**

| Bit | Field | Default | Description |
|---|---|---|---|
| 7 | OTF | 0 | FET Overtemperature<br>0 = Disabled<br>1 = Enabled |
| 6 | OTINT | 0 | Internal Overtemperature<br>0 = Disabled<br>1 = Enabled |
| 5 | OTD | 0 | Overtemperature in Discharge<br>0 = Disabled<br>1 = Enabled |
| 4 | OTC | 0 | Overtemperature in Charge<br>0 = Disabled<br>1 = Enabled |

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**Table 87. Enabled Protections B Register Field Descriptions (continued)**

| Bit | Field | Default | Description |
|---|---|---|---|
| 2 | UTINT | 0 | Internal Undertemperature<br>0 = Disabled<br>1 = Enabled |
| 1 | UTD | 0 | Undertemperature in Discharge<br>0 = Disabled<br>1 = Enabled |
| 0 | UTC | 0 | Undertemperature in Charge<br>0 = Disabled<br>1 = Enabled |

#### 7.6.2.3.4 Settings:Protection:Enabled Protections C

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Protection | Enabled Protections C | U1 | 0x00 | 0xFF | 0x00 | Hex |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OCD3 | SCDL | OCDL | COVL | RSVD | PTO | HWDF | RSVD_0 |

**Description**: This bitfield enables or disables various protections. Protections which are enabled will set their corresponding Safety Status flags. Note: ***Settings:Protection:CHG FET Protections C*** and ***Settings:Protection:DSG FET Protections C*** must be appropriately configured to control the FET action taken when these faults are detected.

**Table 88. Enabled Protections C Register Field Descriptions**

| Bit | Field | Default | Description |
|---|---|---|---|
| 7 | OCD3 | 0 | Overcurrent in Discharge 3rd Tier Protection<br>0 = Disabled<br>1 = Enabled |
| 6 | SCDL | 0 | Short Circuit in Discharge Latch<br>0 = Disabled<br>1 = Enabled |
| 5 | OCDL | 0 | Overcurrent in Discharge Latch<br>0 = Disabled<br>1 = Enabled |
| 4 | COVL | 0 | Cell Overvoltage Latch<br>0 = Disabled<br>1 = Enabled |
| 2 | PTO | 0 | Precharge Timeout<br>0 = Disabled<br>1 = Enabled |
| 1 | HWDF | 0 | Host Watchdog Fault<br>0 = Disabled<br>1 = Enabled |

#### 7.6.2.3.5 Settings:Protection:CHG FET Protections A

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Protection | CHG FET Protections A | U1 | 0x00 | 0xFF | 0x98 | Hex |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SCD | RSVD_0 | RSVD_0 | OCC | COV | RSVD_0 | RSVD_0 | RSVD_0 |

**Description**: This bitfield configures which protections will disable the CHG FET. Note: for the CHG FET turnoff action to occur immediately when a fault is detected, this value should only be set to 0x98 or 0x18. Setting it to other values can cause FET turnoff action to be delayed by up to 250 ms in NORMAL mode or 1 second in SLEEP mode.

**Table 89. CHG FET Protections A Register Field Descriptions**

| Bit | Field | Default | Description |
|---|---|---|---|
| 7 | SCD | 1 | Short Circuit in Discharge Protection<br>0 = CHG FET is not disabled when protection is triggered.<br>1 = CHG FET is disabled when protection is triggered. |
| 4 | OCC | 1 | Overcurrent in Charge Protection<br>0 = CHG FET is not disabled when protection is triggered.<br>1 = CHG FET is disabled when protection is triggered. |
| 3 | COV | 1 | Cell Overvoltage Protection<br>0 = CHG FET is not disabled when protection is triggered.<br>1 = CHG FET is disabled when protection is triggered. |

#### 7.6.2.3.6 Settings:Protection:CHG FET Protections B

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Protection | CHG FET Protections B | U1 | 0x00 | 0xFF | 0xD5 | Hex |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OTF | OTINT | RSVD_0 | OTC | RSVD_0 | UTINT | RSVD_0 | UTC |

**Description**: This bitfield configures which protections will disable the CHG FET. CHG FET action for any non-reserved bits may be individually selected.

**Table 90. CHG FET Protections B Register Field Descriptions**

| Bit | Field | Default | Description |
|---|---|---|---|
| 7 | OTF | 1 | FET Overtemperature<br>0 = CHG FET is not disabled when protection is triggered.<br>1 = CHG FET is disabled when protection is triggered. |
| 6 | OTINT | 1 | Internal Overtemperature<br>0 = CHG FET is not disabled when protection is triggered.<br>1 = CHG FET is disabled when protection is triggered. |
| 4 | OTC | 1 | Overtemperature in Charge<br>0 = CHG FET is not disabled when protection is triggered.<br>1 = CHG FET is disabled when protection is triggered. |
| 2 | UTINT | 1 | Internal Undertemperature<br>0 = CHG FET is not disabled when protection is triggered.<br>1 = CHG FET is disabled when protection is triggered. |
| 0 | UTC | 1 | Undertemperature in Charge<br>0 = CHG FET is not disabled when protection is triggered.<br>1 = CHG FET is disabled when protection is triggered. |

#### 7.6.2.3.7 Settings:Protection:CHG FET Protections C

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Protection | CHG FET Protections C | U1 | 0x00 | 0xFF | 0x56 | Hex |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RSVD_0 | SCDL | RSVD_0 | COVL | RSVD_0 | PTO | HWDF | RSVD_0 |

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**Description**: This bitfield configures which protections will disable the CHG FET. CHG FET action for any non-reserved bits may be individually selected.

**Table 91. CHG FET Protections C Register Field Descriptions**

| Bit | Field | Default | Description |
|---|---|---|---|
| 6 | SCDL | 1 | Short Circuit in Discharge Latch<br>0 = CHG FET is not disabled when protection is triggered.<br>1 = CHG FET is disabled when protection is triggered. |
| 4 | COVL | 1 | Cell Overvoltage Latch<br>0 = CHG FET is not disabled when protection is triggered.<br>1 = CHG FET is disabled when protection is triggered. |
| 2 | PTO | 1 | Precharge Timeout<br>0 = CHG FET is not disabled when protection is triggered.<br>1 = CHG FET is disabled when protection is triggered. |
| 1 | HWDF | 1 | Host Watchdog Fault<br>0 = CHG FET is not disabled when protection is triggered.<br>1 = CHG FET is disabled when protection is triggered. |

#### 7.6.2.3.8 Settings:Protection:DSG FET Protections A

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Protection | DSG FET Protections A | U1 | 0x00 | 0xFF | 0xE4 | Hex |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SCD | OCD2 | OCD1 | RSVD_0 | RSVD_0 | CUV | RSVD_0 | RSVD_0 |

**Description**: This bitfield configures which protections will disable the DSG FET. Note: for the DSG FET turnoff action to occur immediately when a fault is detected, this value should only be set to 0x80 or 0xE4. Setting it to other values can cause FET turnoff action to be delayed by up to 250 ms in NORMAL mode or 1 second in SLEEP mode

**Table 92. DSG FET Protections A Register Field Descriptions**

| Bit | Field | Default | Description |
|---|---|---|---|
| 7 | SCD | 1 | Short Circuit in Discharge Protection<br>0 = DSG FET is not disabled when protection is triggered.<br>1 = DSG FET is disabled when protection is triggered. |
| 6 | OCD2 | 1 | Overcurrent in Discharge 2nd Tier Protection<br>0 = DSG FET is not disabled when protection is triggered.<br>1 = DSG FET is disabled when protection is triggered. |
| 5 | OCD1 | 1 | Overcurrent in Discharge 1st Tier Protection<br>0 = DSG FET is not disabled when protection is triggered.<br>1 = DSG FET is disabled when protection is triggered. |
| 2 | CUV | 1 | Cell Undervoltage Protection<br>0 = DSG FET is not disabled when protection is triggered.<br>1 = DSG FET is disabled when protection is triggered. |

#### 7.6.2.3.9 Settings:Protection:DSG FET Protections B

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Protection | DSG FET Protections B | U1 | 0x00 | 0xFF | 0xE6 | Hex |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OTF | OTINT | OTD | RSVD_0 | RSVD_0 | UTINT | UTD | RSVD_0 |

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**Description**: This bitfield configures which protections will disable the DSG FET. DSG FET action for any non-reserved bits may be individually selected.

**Table 93. DSG FET Protections B Register Field Descriptions**

| Bit | Field | Default | Description |
|---|---|---|---|
| 7 | OTF | 1 | FET Overtemperature<br>0 = DSG FET is not disabled when protection is triggered.<br>1 = DSG FET is disabled when protection is triggered. |
| 6 | OTINT | 1 | Internal Overtemperature<br>0 = DSG FET is not disabled when protection is triggered.<br>1 = DSG FET is disabled when protection is triggered. |
| 5 | OTD | 1 | Overtemperature in Discharge<br>0 = DSG FET is not disabled when protection is triggered.<br>1 = DSG FET is disabled when protection is triggered. |
| 2 | UTINT | 1 | Internal Undertemperature<br>0 = DSG FET is not disabled when protection is triggered.<br>1 = DSG FET is disabled when protection is triggered. |
| 1 | UTD | 1 | Undertemperature in Discharge<br>0 = DSG FET is not disabled when protection is triggered.<br>1 = DSG FET is disabled when protection is triggered. |

#### 7.6.2.3.10 Settings:Protection:DSG FET Protections C

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Protection | DSG FET Protections C | U1 | 0x00 | 0xFF | 0xE2 | Hex |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OCD3 | SCDL | OCDL | RSVD_0 | RSVD_0 | RSVD_0 | HWDF | RSVD_0 |

**Description**: This bitfield configures which protections will disable the DSG FET. DSG FET action for any non-reserved bits may be individually selected.

**Table 94. DSG FET Protections C Register Field Descriptions**

| Bit | Field | Default | Description |
|---|---|---|---|
| 7 | OCD3 | 1 | Overcurrent in Discharge 3rd Tier Protection<br>0 = DSG FET is not disabled when protection is triggered.<br>1 = DSG FET is disabled when protection is triggered. |
| 6 | SCDL | 1 | Short Circuit in Discharge Latch<br>0 = DSG FET is not disabled when protection is triggered.<br>1 = DSG FET is disabled when protection is triggered. |
| 5 | OCDL | 1 | Overcurrent in Discharge Latch<br>0 = DSG FET is not disabled when protection is triggered.<br>1 = DSG FET is disabled when protection is triggered. |
| 1 | HWDF | 1 | Host Watchdog Fault<br>0 = DSG FET is not disabled when protection is triggered.<br>1 = DSG FET is disabled when protection is triggered. |

#### 7.6.2.3.11 Settings:Protection:Body Diode Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Protection | Body Diode Threshold | I2 | 0 | 32767 | 50 | mA |

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**Description**: To minimize power dissipation in the FET body diode, the FET is turned on when reverse current is detected and the other FET is on. When measured discharge current is greater in magnitude than ***Settings:Protection:Body Diode Threshold*** and the DSG FET or PDSG FET is on, the CHG FET is turned on, and the PCHG FET is turned off. When measured charge current is greater than ***Settings:Protection:Body Diode Threshold*** and the CHG FET or PCHG FET is on, the DSG FET is turned on, and the PDSG FET is turned off. When in parallel FET mode (***Settings:FET:FET Options[SFET]*** = 0), body diode protection is disabled and a FET will not be turned on in response to reverse current.

### *7.6.2.4 Settings:Alarm*

#### 7.6.2.4.1 Settings:Alarm:Default Alarm Mask

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Alarm | Default Alarm Mask | H2 | 0x0000 | 0xFFFF | 0xF800 | Hex |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| SSBC | SSA | PF | MSK_SFALERT | MSK_PFALERT | INITSTART | INITCOMP | RSVD_0 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FULLSCAN | XCHG | XDSG | SHUTV | FUSE | CB | ADSCAN | WAKE |

**Description**: This parameter sets the default value of the *AlarmEnable()* register. The default value is reloaded at reset and at exit of CONFIG_UPDATE mode.

**Table 95. Default Alarm Mask Register Field Descriptions**

| Bit | Field | Default | Description |
|---|---|---|---|
| 15 | SSBC | 1 | This bit is set when a bit is set in *Safety Status B()* or *Safety Status C()*. |
| 14 | SSA | 1 | This bit is set when a bit is set in *Safety Status A()*. |
| 13 | PF | 1 | This bit is set when an enabled Permanent Fail fault triggers. |
| 12 | MSK_SFALERT | 1 | This bit is set when a safety alert is triggered that is also enabled in the corresponding ***Settings:Alarm:SF Alert Mask A***, ***Settings:Alarm:SF Alert Mask B***, or ***Settings:Alarm:SF Alert Mask C*** register. |
| 11 | MSK_PFALERT | 1 | This bit is set when a Permanent Fail alert is triggered that is also enabled in the corresponding ***Settings:Alarm:PF Alert Mask A***, ***Settings:Alarm:PF Alert Mask B***, ***Settings:Alarm:PF Alert Mask C***, or ***Settings:Alarm:PF Alert Mask D*** register. |
| 10 | INITSTART | 0 | Initialization started (sets quickly after device powers up). |
| 9 | INITCOMP | 0 | Initialization completed (sets after the device has powered and completed one measurement scan). |
| 7 | FULLSCAN | 0 | Full Voltage Scan Complete. The necessary multiple ADC scans have been completed to collect the full voltag emeasurement loop data (including cell voltages, pin or thermistor voltages, etc). This bit sets each time a full scan completes (when enabled). |
| 6 | XCHG | 0 | This bit is set when the CHG FET is off. |
| 5 | XDSG | 0 | This bit is set when the DSG FET is off. |
| 4 | SHUTV | 0 | Stack voltage is below ***Power:Shutdown:Shutdown Stack Voltage***. |
| 3 | FUSE | 0 | FUSE Pin Driven. FUSE pin is being driven by either the device or the secondary protector. |
| 2 | CB | 0 | This bit is set when cell balancing is active. |
| 1 | ADSCAN | 0 | Voltage ADC Scan Complete. A single ADC scan is complete (cell voltages are measured on each scan). This bit sets each time a scan completes (when enabled). |
| 0 | WAKE | 0 | This bit is set when the device is wakened from SLEEP mode. |

#### 7.6.2.4.2 Settings:Alarm:SF Alert Mask A

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Alarm | SF Alert Mask A | U1 | 0x00 | 0xFF | 0xFC | Hex |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SCD | OCD2 | OCD1 | OCC | COV | CUV | RSVD_0 | RSVD_0 |

**Description**: This parameter selects which protections influence the setting of *AlarmRawStatus()[MSK_SFALERT]*. When the bitwise and of ***Settings:Alarm:SF Alert Mask A*** and *SafetyAlertA()* is nonzero, *AlarmRawStatus()[MSK_SFALERT]* is set.

#### 7.6.2.4.3 Settings:Alarm:SF Alert Mask B

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Alarm | SF Alert Mask B | U1 | 0x00 | 0xFF | 0xF7 | Hex |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OTF | OTINT | OTD | OTC | RSVD_0 | UTINT | UTD | UTC |

**Description**: This parameter selects which protections influence the setting of *AlarmRawStatus()[MSK_SFALERT]*. When the bitwise and of ***Settings:Alarm:SF Alert Mask B*** and *SafetyAlertB()* is nonzero, *AlarmRawStatus()[MSK_SFALERT]* is set.

#### 7.6.2.4.4 Settings:Alarm:SF Alert Mask C

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Alarm | SF Alert Mask C | U1 | 0x00 | 0xFF | 0xF6 | Hex |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OCD3 | SCDL | OCDL | COVL | RSVD_0 | PTO | RSVD_1 | RSVD_0 |

**Description**: This parameter selects which protections influence the setting of *AlarmRawStatus()[MSK_SFALERT]*. When the bitwise and of ***Settings:Alarm:SF Alert Mask C*** and *SafetyAlertC()* is nonzero, *AlarmRawStatus()[MSK_SFALERT]* is set.

#### 7.6.2.4.5 Settings:Alarm:PF Alert Mask A

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Alarm | PF Alert Mask A | U1 | 0x00 | 0xFF | 0x5F | Hex |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CUDEP | SOTF | RSVD_0 | SOT | SOCD | SOCC | SOV | SUV |

**Description**: This parameter selects which protections influence the setting of *AlarmRawStatus()[MSK_PFALERT]*. When the bitwise and of ***Settings:Alarm:PF Alert Mask A*** and *PFAlertA()* is nonzero, *AlarmRawStatus()[MSK_PFALERT]* is set.

#### 7.6.2.4.6 Settings:Alarm:PF Alert Mask B

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Alarm | PF Alert Mask B | U1 | 0x00 | 0xFF | 0x9F | Hex |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SCDL | RSVD_0 | RSVD_0 | VIMA | VIMR | 2LVL | DFETF | CFETF |

**Description**: This parameter selects which protections influence the setting of *AlarmRawStatus()[MSK_PFALERT]*. When the bitwise and of ***Settings:Alarm:PF Alert Mask B*** and *PFAlertB()* is nonzero, *AlarmRawStatus()[MSK_PFALERT]* is set.

#### 7.6.2.4.7 Settings:Alarm:PF Alert Mask C

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Alarm | PF Alert Mask C | U1 | 0x00 | 0xFF | 0x00 | Hex |

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| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RSVD_0 | HWMX | VSSF | VREF | LFOF | RSVD_0 | RSVD_0 | RSVD_0 |

**Description**: This parameter selects which protections influence the setting of *AlarmRawStatus()[MSK_PFALERT]*. When the bitwise and of ***Settings:Alarm:PF Alert Mask C*** and *PFAlertC()* is nonzero, *AlarmRawStatus()[MSK_PFALERT]* is set.

#### 7.6.2.4.8 Settings:Alarm:PF Alert Mask D

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Alarm | PF Alert Mask D | U1 | 0x00 | 0xFF | 0x00 | Hex |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | TOSF |

**Description**: This parameter selects which protections influence the setting of *AlarmRawStatus()[MSK_PFALERT]*. When the bitwise and of ***Settings:Alarm:PF Alert Mask D*** and *PFAlertD()* is nonzero, *AlarmRawStatus()[MSK_PFALERT]* is set.

### *7.6.2.5 Settings:Permanent Failure*

#### 7.6.2.5.1 Settings:Permanent Failure:Enabled PF A

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Permanent Failure | Enabled PF A | U1 | 0x00 | 0xFF | 0x00 | Hex |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CUDEP | SOTF | RSVD_0 | SOT | SOCD | SOCC | SOV | SUV |

**Table 96. Enabled PF A Register Field Descriptions**

| Bit | Field | Default | Description |
|---|---|---|---|
| 7 | CUDEP | 0 | Copper Deposition Permanent Fail<br>0 = Disabled<br>1 = Enabled |
| 6 | SOTF | 0 | Safety Overtemperature FET Permanent Fail<br>0 = Disabled<br>1 = Enabled |
| 4 | SOT | 0 | Safety Overtemperature Permanent Fail<br>0 = Disabled<br>1 = Enabled |
| 3 | SOCD | 0 | Safety Overcurrent in Discharge Permanent Fail<br>0 = Disabled<br>1 = Enabled |
| 2 | SOCC | 0 | Safety Overcurrent in Charge Permanent Fail<br>0 = Disabled<br>1 = Enabled |
| 1 | SOV | 0 | Safety Cell Overvoltage Permanent Fail<br>0 = Disabled<br>1 = Enabled |
| 0 | SUV | 0 | Safety Cell Undervoltage Permanent Fail<br>0 = Disabled<br>1 = Enabled |

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#### 7.6.2.5.2 Settings:Permanent Failure:Enabled PF B

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Permanent Failure | Enabled PF B | U1 | 0x00 | 0xFF | 0x00 | Hex |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SCDL | RSVD_0 | RSVD_0 | VIMA | VIMR | 2LVL | DFETF | CFETF |

**Table 97. Enabled PF B Register Field Descriptions**

| Bit | Field | Default | Description |
|---|---|---|---|
| 7 | SCDL | 0 | Short Circuit in Discharge Latch Permanent Fail<br>0 = Disabled<br>1 = Enabled |
| 4 | VIMA | 0 | Voltage Imbalance Active Permanent Fail<br>0 = Disabled<br>1 = Enabled |
| 3 | VIMR | 0 | Voltage Imbalance at Rest Permanent Fail<br>0 = Disabled<br>1 = Enabled |
| 2 | 2LVL | 0 | Second Level Protector Permanent Fail<br>0 = Disabled<br>1 = Enabled |
| 1 | DFETF | 0 | Discharge FET Permanent Fail<br>0 = Disabled<br>1 = Enabled |
| 0 | CFETF | 0 | Charge FET Permanent Fail<br>0 = Disabled<br>1 = Enabled |

#### 7.6.2.5.3 Settings:Permanent Failure:Enabled PF C

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Permanent Failure | Enabled PF C | U1 | 0x00 | 0xFF | 0x07 | Hex |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CMDF | HWMX | VSSF | VREF | LFOF | IRMF | DRMF | OTPF |

**Table 98. Enabled PF C Register Field Descriptions**

| Bit | Field | Default | Description |
|---|---|---|---|
| 7 | CMDF | 0 | Commanded Permanent Fail<br>0 = Disabled<br>1 = Enabled |
| 6 | HWMX | 0 | Internal Stuck Hardware Mux Permanent Fail<br>0 = Disabled<br>1 = Enabled |
| 5 | VSSF | 0 | Internal VSS Measurement Permanent Fail<br>0 = Disabled<br>1 = Enabled |
| 4 | VREF | 0 | Internal Voltage Reference Permanent Fail<br>0 = Disabled<br>1 = Enabled |
| 3 | LFOF | 0 | Internal LFO Permanent Fail<br>0 = Disabled<br>1 = Enabled |

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**Table 98. Enabled PF C Register Field Descriptions (continued)**

| Bit | Field | Default | Description |
|---|---|---|---|
| 2 | IRMF | 1 | Instruction ROM Permanent Fail<br>0 = Disabled<br>1 = Enabled |
| 1 | DRMF | 1 | Data ROM Permanent Fail<br>0 = Disabled<br>1 = Enabled |
| 0 | OTPF | 1 | OTP Memory Permanent Fail<br>0 = Disabled<br>1 = Enabled |

#### 7.6.2.5.4 Settings:Permanent Failure:Enabled PF D

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Permanent Failure | Enabled PF D | U1 | 0x00 | 0xFF | 0x00 | Hex |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | TOSF |

**Table 99. Enabled PF D Register Field Descriptions**

| Bit | Field | Default | Description |
|---|---|---|---|
| 0 | TOSF | 0 | Top of Stack versus Cell Sum Permanent Fail<br>0 = Disabled<br>1 = Enabled |

### *7.6.2.6 Settings:FET*

#### 7.6.2.6.1 Settings:FET:FET Options

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | FET | FET Options | H1 | 0x00 | 0xFF | 0x09 | Hex |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RSVD_0 | RSVD_0 | FET_INIT_OFF | PDSG_EN | FET_CTRL_EN | HOST_FET_EN | SLEEPCHG | SFET |

**Table 100. FET Options Register Field Descriptions**

| Bit | Field | Default | Description |
|---|---|---|---|
| 5 | FET_INIT_OFF | 0 | The host has the option to send commands to turn the FETs off or allow them to be turned on. This bit may be set for the device to wait for a host command before turning FETs on.<br>0 = Default host FET control state allows FETs to be on<br>1 = Default host FET control state forces FETs off |
| 4 | PDSG_EN | 0 | To reduce inrush current when the DSG FET turns on, the PDSG FET can be enabled for a short time first to charge up the load through a higher-resistance path. This bit enables this operation.<br>0 = PDSG FET is not used<br>1 = PDSG FET is turned on before DSG |
| 3 | FET_CTRL_EN | 1 | In systems where the device's FET drivers are not used, the charge pump should be disabled in ***Settings:FET:Chg Pump Control*** and this bit should be cleared to prevent the device from attempting to turn the FETs on.<br>0 = FETs will not be turned on<br>1 = FETs are controlled by the device |

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**Table 100. FET Options Register Field Descriptions (continued)**

| Bit | Field | Default | Description |
|---|---|---|---|
| 2 | HOST_FET_EN | 0 | Some systems need the ability to override the device's FET control and force the FETs to turn off through commands. If that functionality is not needed, it can be disabled to prevent commands from turning the FETs off.<br>0 = Host FET control commands are ignored<br>1 = Host FET control commands are allowed |
| 1 | SLEEPCHG | 0 | The CHG FET can be disabled while in SLEEP mode to conserve power. This bit configures whether or not to allow the CHG FET to be enabled in SLEEP mode.<br>0 = CHG FET is turned off in SLEEP mode<br>1 = CHG FET may be enabled in SLEEP mode |
| 0 | SFET | 1 | The device supports both series and parallel FET configurations. When the CHG and DSG FETs are in series, current may flow through the body diode of one of the FETs when the other is enabled. In this configuration, body diode protection is used to turn the FET on when current above a threshold is detected to be flowing through that FET. When the system has separate DSG and CHG paths and parallel FETs, body diode protection is not needed and should be disabled.<br>0 = Parallel FET mode: Body diode protection is disabled<br>1 = Series FET mode: Body diode protection is enabled |

#### 7.6.2.6.2 Settings:FET:Chg Pump Control

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | FET | Chg Pump Control | U1 | 0x00 | 0xFF | 0x01 | Hex |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | SFMODE_SLEEP | LVEN | CPEN |

**Table 101. Chg Pump Control Register Field Descriptions**

| Bit | Field | Default | Description |
|---|---|---|---|
| 2 | SFMODE_SLEEP | 0 | To conserve power in SLEEP mode, the DSG FET driver may be configured to enter source-follower mode. This is normally only used when ***Settings:FET:FET Options[SLEEPCHG]*** is set to zero. When current is detected by the CC2 Wake Comparator, source-follower mode is disabled and the FET driver operates normally. Source-follower mode is also disabled when SLEEP mode is exited through other means.<br>0 = Source-follower mode is not enabled on the DSG FET driver<br>1 = Source-follower mode is enabled on the DSG FET driver while in SLEEP mode |
| 1 | LVEN | 0 | This bit selects the charge pump overdrive level.<br>0 = Charge pump high overdrive level (11 V) is selected<br>1 = Charge pump low overdrive level (5.5 V) is selected |
| 0 | CPEN | 1 | This bit enables or disables the charge pumps for the FET drivers. If FET drivers are not to be used at all, ***Settings:FET:FET Options[FET_CTRL_EN]*** should also be set to zero.<br>0 = Charge pumps for FET drivers are disabled<br>1 = Charge pumps for FET drivers are enabled |

#### 7.6.2.6.3 Settings:FET:Precharge Start Voltage

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | FET | Precharge Start Voltage | I2 | 0 | 32767 | 0 | mV |

**Description**: Precharge mode can be used to provide lower-current charging through the PCHG FET instead of the CHG FET for an under-voltage battery. When the minimum cell voltage is less than this threshold, precharge mode is activated. To disable precharge mode, set this value to 0.

#### 7.6.2.6.4 Settings:FET:Precharge Stop Voltage

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | FET | Precharge Stop Voltage | I2 | 0 | 32767 | 0 | mV |

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**Description**: Precharge mode can be used to provide lower-current charging through the PCHG FET instead of the CHG FET for an under-voltage battery. When the minimum cell voltage is greater than or equal to this threshold, precharge mode is deactivated. To disable precharge mode, set this value to 0.

#### 7.6.2.6.5 Settings:FET:Predischarge Timeout

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | FET | Predischarge Timeout | U1 | 0 | 255 | 5 | 10ms |

**Description**: When predischarge mode is enabled, the maxiumum duration of predischarge mode can be set in 10-ms increments.

0 = No timeout. Predischarge mode is exited when voltage conditions are met.

All other values = Predischarge mode is exited and DSG is turned on after configured timeout.

#### 7.6.2.6.6 Settings:FET:Predischarge Stop Delta

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | FET | Predischarge Stop Delta | U1 | 0 | 255 | 50 | cV |

**Description**: Every 250 ms, the device checks the last measured LD pin and top-of-stack voltages if in predischarge mode. Predischarge mode is exited if the voltage on the LD pin is greater than or equal to the top-of-stack voltage minus this delta.

0 = Predischarge voltage check disabled. Predischarge mode is exited for timeout.

All other values = Predischarge mode exited when the LD pin voltage is measured within this delta of the top-of-stack voltage.

### *7.6.2.7 Settings:Current Thresholds*

#### 7.6.2.7.1 Settings:Current Thresholds:Dsg Current Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Current Thresholds | Dsg Current Threshold | I2 | 0 | 32767 | 100 | userA |

**Description**: Certain device features depend upon whether the system is in a discharge state or not. The system is considered to be discharging when measured negative current is larger in magnitude than this threshold.

#### 7.6.2.7.2 Settings:Current Thresholds:Chg Current Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Current Thresholds | Chg Current Threshold | I2 | 0 | 32767 | 50 | userA |

**Description**: Certain device features depend upon whether the system is in a charging state or not. The system is considered to be charging when measured positive current is larger in magnitude than this threshold.

### *7.6.2.8 Settings:Cell Open-Wire*

#### 7.6.2.8.1 Settings:Cell Open-Wire:Check Time

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Cell Open-Wire | Check Time | U1 | 0 | 255 | 5 | s |

**Description**: If a cell connection to the device is detached, the capacitance on the node may maintain the voltage for some time. To detect this condition, the device can periodically enable a current source to VSS on each cell connection to drain the charge on the node. When a cell is detached, that node voltage is discharged, and an over-voltage or under-voltage event will be triggered on that cell or an adjacent cell differential measurement. The current source is enabled for the duration of an ADC measurement (3 ms by default) once per the interval defined by this parameter. A longer interval decreases the average current consumption at the cost of detection time. When using this feature, cell balancing should be considered as well since the current flows from the cell pin to VSS, resulting in a higher average current drawn from lower cells.

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0 = Cell open-wire check is disabled.

All other values = Cell open-wire check current source is enabled briefly for each cell on this interval.

### *7.6.2.9 Settings:Interconnect Resistances*

#### 7.6.2.9.1 Settings:Interconnect Resistances:Cell 1 Interconnect

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Interconnect Resistances | Cell 1 Interconnect | I2 | 0 | 32767 | 0 | mΩ |

**Description**: When a significant interconnect resistance exists between cells, this parameter can be used to account for it in cell voltage measurements. Cell voltage calcualtions utilize the simultaneous current measurement and this resistance value to accurately calculate the cell voltage.

#### 7.6.2.9.2 Settings:Interconnect Resistances:Cell 2 Interconnect

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Interconnect Resistances | Cell 2 Interconnect | I2 | 0 | 32767 | 0 | mΩ |

**Description**: When a significant interconnect resistance exists between cells, this parameter can be used to account for it in cell voltage measurements. Cell voltage calcualtions utilize the simultaneous current measurement and this resistance value to accurately calculate the cell voltage.

#### 7.6.2.9.3 Settings:Interconnect Resistances:Cell 3 Interconnect

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Interconnect Resistances | Cell 3 Interconnect | I2 | 0 | 32767 | 0 | mΩ |

**Description**: When a significant interconnect resistance exists between cells, this parameter can be used to account for it in cell voltage measurements. Cell voltage calcualtions utilize the simultaneous current measurement and this resistance value to accurately calculate the cell voltage.

#### 7.6.2.9.4 Settings:Interconnect Resistances:Cell 4 Interconnect

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Interconnect Resistances | Cell 4 Interconnect | I2 | 0 | 32767 | 0 | mΩ |

**Description**: When a significant interconnect resistance exists between cells, this parameter can be used to account for it in cell voltage measurements. Cell voltage calcualtions utilize the simultaneous current measurement and this resistance value to accurately calculate the cell voltage.

#### 7.6.2.9.5 Settings:Interconnect Resistances:Cell 5 Interconnect

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Interconnect Resistances | Cell 5 Interconnect | I2 | 0 | 32767 | 0 | mΩ |

**Description**: When a significant interconnect resistance exists between cells, this parameter can be used to account for it in cell voltage measurements. Cell voltage calcualtions utilize the simultaneous current measurement and this resistance value to accurately calculate the cell voltage.

#### 7.6.2.9.6 Settings:Interconnect Resistances:Cell 6 Interconnect

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Interconnect Resistances | Cell 6 Interconnect | I2 | 0 | 32767 | 0 | mΩ |

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**Description**: When a significant interconnect resistance exists between cells, this parameter can be used to account for it in cell voltage measurements. Cell voltage calcualtions utilize the simultaneous current measurement and this resistance value to accurately calculate the cell voltage.

#### 7.6.2.9.7 Settings:Interconnect Resistances:Cell 7 Interconnect

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Interconnect Resistances | Cell 7 Interconnect | I2 | 0 | 32767 | 0 | mΩ |

**Description**: When a significant interconnect resistance exists between cells, this parameter can be used to account for it in cell voltage measurements. Cell voltage calcualtions utilize the simultaneous current measurement and this resistance value to accurately calculate the cell voltage.

#### 7.6.2.9.8 Settings:Interconnect Resistances:Cell 8 Interconnect

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Interconnect Resistances | Cell 8 Interconnect | I2 | 0 | 32767 | 0 | mΩ |

**Description**: When a significant interconnect resistance exists between cells, this parameter can be used to account for it in cell voltage measurements. Cell voltage calcualtions utilize the simultaneous current measurement and this resistance value to accurately calculate the cell voltage.

#### 7.6.2.9.9 Settings:Interconnect Resistances:Cell 9 Interconnect

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Interconnect Resistances | Cell 9 Interconnect | I2 | 0 | 32767 | 0 | mΩ |

**Description**: When a significant interconnect resistance exists between cells, this parameter can be used to account for it in cell voltage measurements. Cell voltage calcualtions utilize the simultaneous current measurement and this resistance value to accurately calculate the cell voltage.

#### 7.6.2.9.10 Settings:Interconnect Resistances:Cell 10 Interconnect

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Interconnect Resistances | Cell 10 Interconnect | I2 | 0 | 32767 | 0 | mΩ |

**Description**: When a significant interconnect resistance exists between cells, this parameter can be used to account for it in cell voltage measurements. Cell voltage calcualtions utilize the simultaneous current measurement and this resistance value to accurately calculate the cell voltage.

### *7.6.2.10 Settings:Manufacturing*

#### 7.6.2.10.1 Settings:Manufacturing:Mfg Status Init

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Manufacturing | Mfg Status Init | H2 | 0x0000 | 0xFFFF | 0x0040 | Hex |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OTPW_EN | PF_EN | RSVD_0 | FET_EN | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 |

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**Description**: This is the initial Value loaded to Manufacturing Status when the device resets or receives the SEAL or SET_CFGUPDATE commands.

**Table 102. Mfg Status Init Register Field Descriptions**

| Bit | Field | Default | Description |
|---|---|---|---|
| 7 | OTPW_EN | 0 | This bit enables or disables writes to OTP during operation. The device can program diagnostic information in OTP when a PF occurs or when the fuse is blown to retain state after a full reset. It also can program MANU_DATA upon request (if in FULLACCESS mode). This bit enables the device to program this runtime data to OTP. Programming will only occur when the stack voltage and temperature are within allowed limits. If this bit is not set, programming may still be done in CONFIG_UPDATE mode.<br>0 = Device will not program OTP during operation.<br>1 = Device may program OTP during operation. |
| 6 | PF_EN | 1 | This bit enables or disables Permanent Failure checks. Clearing this bit prevents Permanent Failure from triggering which is useful during manufacturing.<br>0 = Permanent Failure checks are disabled.<br>1 = Permanent Failure checks are enabled. |
| 4 | FET_EN | 0 | This bit enables or disables FET Test mode. In FET Test mode, the FET states are controlled by the FET Test subcommands. This is typically used during manufacturing to test FET circuitry. Note: safety checks still may force FETs off (or for body diode protection, on) in FET Test mode.<br>0 = Normal FET control is disabled. FET Test mode is enabled. Device will not turn on FETs unless FET Test subcommands instruct it to do so.<br>1 = Normal FET control is enabled. FET Test mode is disabled. Device will ignore FET Test subcommands. |

### *7.6.2.11 Settings:Cell Balancing Config*

#### 7.6.2.11.1 Settings:Cell Balancing Config:Balancing Configuration

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Cell Balancing Config | Balancing Configuration | H1 | 0x00 | 0xFF | 0x00 | Hex |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RSVD_0 | RSVD_0 | RSVD_0 | CB_NO_CMD | CB_NOSLEEP | CB_SLEEP | CB_RLX | CB_CHG |

**Table 103. Balancing Configuration Register Field Descriptions**

| Bit | Field | Default | Description |
|---|---|---|---|
| 4 | CB_NO_CMD | 0 | This bit allows blocking of cell balancing commands if host-controlled balancing is not desired.<br>0 = Host-controlled balancing commands are accepted.<br>1 = Host-controlled balancing commands are ignored. |
| 3 | CB_NOSLEEP | 0 | This bit configures the device to exit sleep mode to perform cell balancing. When this bit is set, CB_SLEEP should also be set.<br>0 = SLEEP mode is allowed while cell balancing is active.<br>1 = SLEEP is prevented while cell balancing is active. |
| 2 | CB_SLEEP | 0 | This bit configures whether or not the device is allowed to perform cell balancing while in SLEEP mode.<br>0 = Cell balancing is not performed in SLEEP mode.<br>1 = Cell balancing may be performed while in SLEEP mode. |
| 1 | CB_RLX | 0 | This bit enables cell balancing while current is under ***Settings:Current Thresholds:Chg Current Threshold*** and above -***Settings:Current Thresholds:Dsg Current Threshold***. Note: this only applies to automatic cell balancing. Host-controlled balancing is not affected by this bit.<br>0 = Cell balancing is not allowed in relax conditions.<br>1 = Cell balancing is allowed in relax conditions. |

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**Table 103. Balancing Configuration Register Field Descriptions (continued)**

| Bit | Field | Default | Description |
|---|---|---|---|
| 0 | CB_CHG | 0 | This bit enables cell balancing while current is above ***Settings:Current Thresholds:Chg Current Threshold***. Note: this only applies to automatic cell balancing. Host-controlled balancing is not affected by this bit.<br>0 = Cell balancing is not allowed while charging.<br>1 = Cell balancing is allowed while charging. |

#### 7.6.2.11.2 Settings:Cell Balancing Config:Min Cell Temp

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Cell Balancing Config | Min Cell Temp | I1 | –128 | 127 | –20 | °C |

**Description**: When the minimum cell temperature is below this value, cell balancing is not allowed. This affects both host-controlled balancing and automatic cell balancing.

#### 7.6.2.11.3 Settings:Cell Balancing Config:Max Cell Temp

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Cell Balancing Config | Max Cell Temp | I1 | –128 | 127 | 60 | °C |

**Description**: When the maximum cell temperature is above this value, cell balancing is not allowed. This affects both host-controlled balancing and automatic cell balancing.

#### 7.6.2.11.4 Settings:Cell Balancing Config:Cell Balance Interval

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Cell Balancing Config | Cell Balance Interval | U1 | 1 | 255 | 20 | s |

**Description**: The cell balancing algorithm recalculates which cell to balance after this many seconds. Once a cell is chosen, balancing on that cell will continue for this interval unless one of the conditions which blocks balancing is present. This interval is also used with the commands for host-controlled balancing. A command to balance a cell will keep balancing active for this amount of time. The host may send the command again before the timer expires to reset it and continue balancing.

#### 7.6.2.11.5 Settings:Cell Balancing Config:Cell Balance Min Cell V (Charge)

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Cell Balancing Config | Cell Balance Min Cell V (Charge) | I2 | 0 | 5000 | 3900 | mV |

**Description**: While charging, automatic cell balancing is disabled if the minimum cell voltage is less than this threshold.

#### 7.6.2.11.6 Settings:Cell Balancing Config:Cell Balance Min Delta (Charge)

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Cell Balancing Config | Cell Balance Min Delta (Charge) | U1 | 0 | 255 | 40 | mV |

**Description**: While charging, the delta between the maximum and minimum cell voltages must be greater than this value for automatic cell balancing to begin.

#### 7.6.2.11.7 Settings:Cell Balancing Config:Cell Balance Min Cell V (Relax)

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Cell Balancing Config | Cell Balance Min Cell V (Relax) | I2 | 0 | 5000 | 3900 | mV |

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**Description**: While not charging or discharging, automatic cell balancing is disabled if the minimum cell voltage is less than this threshold.

#### 7.6.2.11.8 Settings:Cell Balancing Config:Cell Balance Min Delta (Relax)

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Settings | Cell Balancing Config | Cell Balance Min Delta (Relax) | U1 | 0 | 255 | 40 | mV |

**Description**: While not charging or discharging, the delta between the maximum and minimum cell voltages must be greater than this value for automatic cell balancing to begin.

### 7.6.3 Power

#### *7.6.3.1 Power:Shutdown*

#### 7.6.3.1.1 Power:Shutdown:Shutdown Cell Voltage

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Power | Shutdown | Shutdown Cell Voltage | I2 | 0 | 32767 | 0 | mV |

**Description**: Configures the cell voltage threshold at which the device will enter SHUTDOWN mode. This threshold does not apply to VC pins configured as interconnects.

Note: consider setting this parameter to zero if the cell open wire feature is enabled, since an open wire will result in a low voltage on the disconnected cell, and the device may shut down before the open wire event is recorded.

0 = Cell-Voltage-based shutdown disabled

All other values = Cell voltage shutdown threshold

#### 7.6.3.1.2 Power:Shutdown:Shutdown Stack Voltage

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Power | Shutdown | Shutdown Stack Voltage | I2 | 0 | 32767 | 600 | cV |

**Description**: Configures the pack voltage threshold at which the device will enter SHUTDOWN mode

#### 7.6.3.1.3 Power:Shutdown:Shutdown Temperature

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Power | Shutdown | Shutdown Temperature | U1 | 0 | 150 | 85 | °C |

**Description**: Configures the internal temperature threshold at which the device will shut down

0 = Shutdown based on measured internal temperature disabled

All other values = Shutdown Internal Temperature threshold

#### 7.6.3.1.4 Power:Shutdown:Shutdown Temperature Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Power | Shutdown | Shutdown Temperature Delay | U1 | 0 | 254 | 5 | s |

**Description**: Configures the number of consecutive seconds the device must measure an internal temperature above ***Power:Shutdown:Shutdown Temperature*** to enter SHUTDOWN mode.

#### 7.6.3.1.5 Power:Shutdown:Charger Present Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Power | Shutdown | Charger Present Threshold | I2 | 0 | 32767 | 300 | cV |

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**Description**: The device will delay voltage-based shutdown until the PACK pin voltage is less than this value. This allows the device to remain powered while the pack is charged up past the shutdown voltage threshold.

#### 7.6.3.1.6 Power:Shutdown:FET Off Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Power | Shutdown | FET Off Delay | U1 | 0 | 127 | 0 | 0.25s |

**Description**: When the SHUTDOWN command is received or the RST_SHUT pin is detected high for one second, the FETs are turned off after this delay.

#### 7.6.3.1.7 Power:Shutdown:Shutdown Command Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Power | Shutdown | Shutdown Command Delay | U1 | 0 | 254 | 0 | 0.25s |

**Description**: When the SHUTDOWN command is received or the RST_SHUT pin is detected high for one second, the device will enter SHUTDOWN after this delay. If the LD pin voltage is still high after this delay, the device will delay entering SHUTDOWN further until that voltage is no longer present.

#### 7.6.3.1.8 Power:Shutdown:Auto Shutdown Time

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Power | Shutdown | Auto Shutdown Time | U1 | 0 | 250 | 0 | min |

**Description**: As a countermeasure to inadvertent wake from SHUTDOWN, the device can be configured to automatically enter SHUTDOWN again after a number of minutes defined by this parameter. If communications occur after the first second, or if charge current is detected, or if discharge current above the SLEEP current threshold is detected after one minute, automatic shutdown is cancelled. If none of those events occur, after this number of minutes, the FETs will be turned off for up to five seconds. During that 5 seconds, if the PACK and LD pin voltages fall, the device will enter shutdown. If the voltage on those pins remain above their respective thresholds, auto-shutdown is cancelled based on a conclusion that a charger is present.

0 = Auto-shutdown feature is disabled.

All other values = Auto-shutdown occurs after this many minutes if it is not cancelled.

#### 7.6.3.1.9 Power:Shutdown:RAM Fail Shutdown Time

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Power | Shutdown | RAM Fail Shutdown Time | U1 | 0 | 255 | 5 | s |

**Description**: The device performs periodic RAM integrity checks and forces a watchdog reset if corruption is detected. To avoid unwanted reset loops in case of a failure, the device will enter SHUTDOWN mode instead of resetting if it detects a RAM error within this number of seconds of a watchdog reset.

### *7.6.3.2 Power:Sleep*

#### 7.6.3.2.1 Power:Sleep:Sleep Current

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Power | Sleep | Sleep Current | I2 | 0 | 32767 | 20 | mA |

**Description**: Configures the current threshold above which the device will not enter SLEEP mode. If current is measured above this value during a periodic measurement in SLEEP mode, SLEEP mode will be exited.

#### 7.6.3.2.2 Power:Sleep:Voltage Time

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Power | Sleep | Voltage Time | U1 | 1 | 20 | 5 | s |

ADVANCE INFORMATION

**Description**: This parameter sets how often the device wakes to measure voltages and temperatures while in SLEEP mode. While in sleep mode, the device begins 4-second current measurements one second after measuring voltages and temperatures. These measurements interrupt the 4-second current measurement and start it over. That means that setting this parameter to a value less than 5 seconds will result in no completed 4-second current measurements in sleep. The most common settings of this parameter are 1 second, 5 seconds, or (4 * n + 1) seconds.

#### 7.6.3.2.3 Power:Sleep:Wake Comparator Current

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Power | Sleep | Wake Comparator Current | I2 | 500 | 32767 | 500 | mA |

**Description**: Configures the current wake comparator threshold in sleep mode. Note: the default wake comparator conversion speed (12 ms) results in lower accuracy conversions than the normal current measurements. The smallest recommended threshold at this speed is 500 mA.

#### 7.6.3.2.4 Power:Sleep:Sleep Hysteresis Time

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Power | Sleep | Sleep Hysteresis Time | U1 | 0 | 255 | 10 | s |

**Description**: After transitioning to NORMAL mode, the device will not enter SLEEP mode again until this number of seconds has passed.

#### 7.6.3.2.5 Power:Sleep:Sleep Charger Voltage Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Power | Sleep | Sleep Charger Voltage Threshold | I2 | 0 | 32767 | 2000 | cV |

**Description**: The Top-of-Stack voltage must be below this threshold to block SLEEP mode based on charger presence.

#### 7.6.3.2.6 Power:Sleep:Sleep Charger PACK-TOS Delta

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Power | Sleep | Sleep Charger PACK-TOS Delta | U1 | 10 | 255 | 10 | cV |

**Description**: If the PACK pin voltage is higher than the Top-of-Stack by more than this threshold and the Top-of-Stack voltage is less than ***Power:Sleep:Sleep Charger Voltage Threshold***, SLEEP mode is not allowed.

### 7.6.4 System Data

#### *7.6.4.1 System Data:Integrity*

#### 7.6.4.1.1 System Data:Integrity:Config RAM Signature

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| System Data | Integrity | Config RAM Signature | U2 | 0x0000 | 0x7FFF | 0 | Hex |

**Description**: The lower 15 bits of the signature of static configuration options (which is returned by the STATIC_CFG_SIG subcommand) should be programmed into this parameter. When the STATIC_CFG_SIG subcommand is sent, the response will be checked against this value. If the value does not match, the top bit will be set in the response returned. This enables the system to validate the static config signature without having knowledge of the signature itself.

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### 7.6.5 Protections

#### *7.6.5.1 Protections:CUV*

##### 7.6.5.1.1 Protections:CUV:Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | CUV | Threshold | U1 | 20 | 90 | 50 | 50 mV |

**Description**: This parameter sets the Cell Undervoltage Protection threshold in units of 50 mV.

##### 7.6.5.1.2 Protections:CUV:Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | CUV | Delay | U2 | 1 | 2047 | 74 | 3.3 ms |

**Description**: This parameter sets the Cell Undervoltage Protection delay in units of 3.3 ms with a 6.6ms offset. This means a setting of 1 gives 10 ms, 2 gives 13.3 ms, and so on.

##### 7.6.5.1.3 Protections:CUV:Recovery Hysteresis

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | CUV | Recovery Hysteresis | U1 | 2 | 20 | 2 | 50 mV |

**Description**: This parameter sets the Cell Undervoltage Protection hysteresis threshold in units of 50mV. The minimum cell voltage must be greater than or equal to the CUV threshold plus this hysteresis for ***Protections:Recovery:Time*** to recover from a CUV condition.

#### *7.6.5.2 Protections:COV*

##### 7.6.5.2.1 Protections:COV:Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | COV | Threshold | U1 | 20 | 110 | 86 | 50 mV |

**Description**: This parameter sets the Cell Overvoltage Protection threshold in units of 50 mV.

##### 7.6.5.2.2 Protections:COV:Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | COV | Delay | U2 | 1 | 2047 | 74 | 3.3 ms |

**Description**: This parameter sets the Cell Overvoltage Protection delay in units of 3.3 ms with a 6.6ms offset. This means a setting of 1 gives 10 ms, 2 gives 13.3 ms, and so on.

##### 7.6.5.2.3 Protections:COV:Recovery Hysteresis

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | COV | Recovery Hysteresis | U1 | 2 | 20 | 2 | 50 mV |

**Description**: This parameter sets the Cell Overvoltage Protection hysteresis threshold in units of 50 mV. The maximum cell voltage must be less than or equal to the COV threshold minus this hysteresis for ***Protections:Recovery:Time*** to recover from a COV condition.

#### *7.6.5.3 Protections:COVL*

##### 7.6.5.3.1 Protections:COVL:Latch Limit

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | COVL | Latch Limit | U1 | 0 | 255 | 0 | — |

ADVANCE INFORMATION

**Description**: Whenever a COV event occurs, the COV latch counter is incremented. If the latch counter reaches this limit, the Cell Overvoltage Latch Protection is triggered. This protection allows for a longer recovery time when repeated COV events occur because the action of turning the CHG FET off cause the voltage to drop enough to recover.

#### 7.6.5.3.2 Protections:COVL:Counter Dec Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | COVL | Counter Dec Delay | U1 | 0 | 255 | 10 | s |

**Description**: Whenever a COV event occurs, the COV latch counter is incremented. While the counter is nonzero, it will be decremented after the delay set by this parameter. This parameter should be set to a value larger than ***Protections:Recovery:Time*** to ensure that repeated COV events can increment the counter faster than this would decrement it. This parameter should be set to a value smaller than ***Protections:COVL:Recovery Time*** to ensure that the latch counter is decremented before recovering. Otherwise, the protection would trigger again since the latch counter is still at the limit.

#### 7.6.5.3.3 Protections:COVL:Recovery Time

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | COVL | Recovery Time | U1 | 0 | 255 | 15 | s |

**Description**: This parameter sets the delay after which the Cell Overvoltage Latch Protection will recover. It should be set longer than ***Protections:COVL:Counter Dec Delay*** to ensure that the latch counter is decremented before recovering. Otherwise, the protection will trigger again since the latch counter is still at the limit.

### *7.6.5.4 Protections:OCC*

#### 7.6.5.4.1 Protections:OCC:Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | OCC | Threshold | U1 | 2 | 62 | 2 | 2 mV |

**Description**: This parameter sets the Overcurrent in Charge Protection threshold for the sense resistor voltage in units of 2 mV.

#### 7.6.5.4.2 Protections:OCC:Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | OCC | Delay | U1 | 1 | 127 | 4 | 3.3 ms |

**Description**: This parameter sets the delay before the fault is triggered in units of 3.3 ms with a 6.6ms offset. This means a setting of 1 gives 10 ms, 2 gives 13.3 ms, and so on.

#### 7.6.5.4.3 Protections:OCC:Recovery Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | OCC | Recovery Threshold | I2 | –32768 | 32767 | –200 | mA |

**Description**: This sets the recovery threshold for the Overcurrent in Charge Protection. If measured current is less than or equal to this threshold for ***Protections:Recovery:Time***, recovery occurs.

#### 7.6.5.4.4 Protections:OCC:PACK-TOS Delta

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | OCC | PACK-TOS Delta | U1 | 10 | 255 | 10 | cV |

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**Description**: This parameter configures an alternate recovery mechanism for Overcurrent in Charge. If the PACK pin voltage is less than or equal to the Top-of-Stack voltage minus this delta for ***Protections:Recovery:Time*** second, recovery occurs.

### *7.6.5.5 Protections:OCD1*

#### 7.6.5.5.1 Protections:OCD1:Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | OCD1 | Threshold | U1 | 2 | 62 | 4 | 2mV |

**Description**: This parameter sets the Overcurrent in Discharge 1st Tier Protection threshold for the sense resistor voltage in units of 2 mV.

#### 7.6.5.5.2 Protections:OCD1:Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | OCD1 | Delay | U1 | 1 | 127 | 1 | 3.3 ms |

**Description**: This parameter sets the delay before the fault is triggered in units of 3.3 ms with a 6.6 ms offset. This means a setting of 1 gives 10 ms, 2 gives 13.3 ms, and so on.

### *7.6.5.6 Protections:OCD2*

#### 7.6.5.6.1 Protections:OCD2:Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | OCD2 | Threshold | U1 | 2 | 62 | 3 | 2 mV |

**Description**: This parameter sets the Overcurrent in Discharge 2nd Tier Protection threshold for the sense resistor voltage in units of 2 mV.

#### 7.6.5.6.2 Protections:OCD2:Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | OCD2 | Delay | U1 | 1 | 127 | 7 | 3.3 ms |

**Description**: This parameter sets the delay before the fault is triggered in units of 3.3 ms with a 6.6 ms offset. This means a setting of 1 gives 10 ms, 2 gives 13.3 ms, and so on.

### *7.6.5.7 Protections:SCD*

#### 7.6.5.7.1 Protections:SCD:Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | SCD | Threshold | U1 | 0 | 15 | 0 | — |

**Description**: This parameter sets the Short Circuit in Discharge Protection threshold for the sense resistor voltage.

0 = 10 mV

1 = 20 mV

2 = 40 mV

3 = 60 mV

4 = 80 mV

5 = 100 mV

6 = 125 mV

7 = 150 mV

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8 = 175 mV

9 = 200 mV

10 = 250 mV

11 = 300 mV

12 = 350 mV

13 = 400 mV

14 = 450 mV

15 = 500 mV

#### 7.6.5.7.2 Protections:SCD:Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | SCD | Delay | U1 | 1 | 31 | 2 | 15 µs |

**Description**: This parameter sets the delay before the fault is triggered in units of 15 µs.

1 = Protection is enabled with no delay.

All other values = Enabled with a delay of (value - 1) * 15 µs

#### 7.6.5.7.3 Protections:SCD:Recovery Time

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | SCD | Recovery Time | U1 | 0 | 255 | 5 | s |

**Description**: This parameter configures the delay after which the Short Circuit in Discharge Protection recovers. If time-based recovery from SCD is not desired, the Short Circuit in Discharge Latch protection can be used with a ***Protections:SCDL:Latch Limit*** of 1.

### *7.6.5.8 Protections:OCD3*

#### 7.6.5.8.1 Protections:OCD3:Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | OCD3 | Threshold | I2 | –32768 | 0 | –4000 | userA |

**Description**: This parameter sets the Overcurrent in Discharge 3rd Tier Protection threshold. Units of reported current are configurable. This parameter uses the same units as reported current, so it is in units of user-amps.

#### 7.6.5.8.2 Protections:OCD3:Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | OCD3 | Delay | U1 | 0 | 255 | 2 | s |

**Description**: This parameter sets the delay for Overcurrent in Discharge 3rd Tier to trigger in units of seconds.

### *7.6.5.9 Protections:OCD*

#### 7.6.5.9.1 Protections:OCD:Recovery Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | OCD | Recovery Threshold | I2 | –32768 | 32767 | 200 | mA |

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**Description**: This sets the recovery threshold for Overcurrent in Discharge 1st, 2nd, and 3rd Tier Protections. Measured current must be greater than or equal to this threshold for ***Protections:Recovery:Time*** to recover. Note: the sign of current when configuring this parameter; by default it requires charge current above this threshold.

### *7.6.5.10 Protections:OCDL*

#### 7.6.5.10.1 Protections:OCDL:Latch Limit

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | OCDL | Latch Limit | U1 | 0 | 255 | 0 | — |

**Description**: Whenever an OCD event occurs, the OCD latch counter is incremented. If the latch counter reaches this limit, the Overcurrent Latch Protection is triggered. This protection allows for alternate recovery conditions when repeated Overcurrent in Discharge events occur.

#### 7.6.5.10.2 Protections:OCDL:Counter Dec Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | OCDL | Counter Dec Delay | U1 | 0 | 255 | 10 | s |

**Description**: Whenever an OCD event occurs, the OCD latch counter is incremented. While the counter is nonzero, it will be decremented after the delay set by this parameter. This parameter should be set to a value larger than ***Protections:Recovery:Time*** to ensure that repeated OCD events can increment the counter faster than this would decrement it.

#### 7.6.5.10.3 Protections:OCDL:Recovery Time

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | OCDL | Recovery Time | U1 | 0 | 255 | 15 | s |

**Description**: This parameter sets the recovery delay for the Overcurrent in Discharge Latch Protection. Measured current must be greater than or equal to the ***Protections:OCDL:Recovery Threshold*** for this many seconds for recovery to occur through this mechanism. This recovery mechanism is disabled when ***Settings:Protection:Protection Configuration[OCDL_CURR_RECOV]*** is not set.

#### 7.6.5.10.4 Protections:OCDL:Recovery Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | OCDL | Recovery Threshold | I2 | –32768 | 32767 | 200 | mA |

**Description**: This parameter sets the recovery threshold for the Overcurrent in Discharge Latch Protection. Measured current must be greater than or equal to this value for ***Protections:OCDL:Recovery Time*** seconds for recovery to occur through this mechanism. This recovery mechanism is disabled when ***Settings:Protection:Protection Configuration[OCDL_CURR_RECOV]*** is not set.

### *7.6.5.11 Protections:SCDL*

#### 7.6.5.11.1 Protections:SCDL:Latch Limit

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | SCDL | Latch Limit | U1 | 0 | 255 | 0 | — |

**Description**: Whenever an SCD event occurs, the SCD latch counter is incremented. If the latch counter reaches this limit, the Short Circuit in Discharge Latch Protection is triggered. This protection allows for alternate recovery conditions when repeated Short Circuit in Discharge events occur.

#### 7.6.5.11.2 Protections:SCDL:Counter Dec Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | SCDL | Counter Dec Delay | U1 | 0 | 255 | 10 | s |

**Description**: Whenever an SCD event occurs, the SCD latch counter is incremented. While the counter is nonzero, it will be decremented after the delay set by this parameter. This parameter should be set to a value larger than ***Protections:SCD:Recovery Time*** to ensure that repeated SCD events can increment the counter faster than this would decrement it.

#### 7.6.5.11.3 Protections:SCDL:Recovery Time

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | SCDL | Recovery Time | U1 | 0 | 255 | 15 | s |

**Description**: This parameter sets the recovery delay for the Short Circuit in Discharge Latch Protection. Measured current must be greater than or equal to the ***Protections:SCDL:Recovery Threshold*** for this many seconds for recovery to occur through this mechanism. This recovery mechanism is disabled when ***Settings:Protection:Protection Configuration[SCDL_CURR_RECOV]*** is not set.

#### 7.6.5.11.4 Protections:SCDL:Recovery Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | SCDL | Recovery Threshold | I2 | –32768 | 32767 | 200 | mA |

**Description**: This parameter sets the recovery threshold for the Short Circuit in Discharge Latch Protection. Measured current must be greater than or equal to this value for ***Protections:SCDL:Recovery Time*** seconds for recovery to occur through this mechanism. This recovery mechanism is disabled when ***Settings:Protection:Protection Configuration[SCDL_CURR_RECOV]*** is not set.

### *7.6.5.12 Protections:OTC*

#### 7.6.5.12.1 Protections:OTC:Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | OTC | Threshold | I1 | –40 | 120 | 55 | °C |

**Description**: This parameter sets the Overtemperature in Charge Protection threshold. When the maximum cell temperature is greater than or equal to this threshold for ***Protections:OTC:Delay*** seconds, the protection is triggered. Note that charging does not need to be occurring for this protection to trigger. It is intended to be the threshold at which charging should not be allowed, not an indicator of if charging happened at this temperature.

#### 7.6.5.12.2 Protections:OTC:Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | OTC | Delay | U1 | 0 | 255 | 2 | s |

**Description**: This parameter sets the Overtemperature in Charge Protection delay. When the maximum cell temperature is greater than or equal to ***Protections:OTC:Threshold*** for this many seconds, the protection is triggered. Note: charging does not need to be occurring for this protection to trigger. It is intended to be the threshold at which charging should not be allowed, not an indicator of if charging happened at this temperature.

#### 7.6.5.12.3 Protections:OTC:Recovery

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | OTC | Recovery | I1 | –40 | 120 | 50 | °C |

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**Description**: This parameter sets the Overtemperature in Charge Protection recovery threshold. Recovery occurs when the maximum cell temperature is less than or equal to this threshold for ***Protections:Recovery:Time*** seconds.

### *7.6.5.13 Protections:OTD*

#### 7.6.5.13.1 Protections:OTD:Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | OTD | Threshold | I1 | –40 | 120 | 60 | °C |

**Description**: This parameter sets the Overtemperature in Discharge Protection threshold. When the maximum cell temperature is greater than or equal to this threshold for ***Protections:OTD:Delay*** seconds, the protection is triggered. Note: discharging does not need to be occurring for this protection to trigger. It is intended to be the threshold at which discharging should not be allowed, not an indicator of if discharging happened at this temperature.

#### 7.6.5.13.2 Protections:OTD:Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | OTD | Delay | U1 | 0 | 255 | 2 | s |

**Description**: This parameter sets the Overtemperature in Discharge Protection delay. When the maximum cell temperature is greater than or equal to ***Protections:OTD:Threshold*** for this many seconds, the protection is triggered. Note: discharging does not need to be occurring for this protection to trigger. It is intended to be the threshold at which discharging should not be allowed, not an indicator of if discharging happened at this temperature.

#### 7.6.5.13.3 Protections:OTD:Recovery

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | OTD | Recovery | I1 | –40 | 120 | 55 | °C |

**Description**: This parameter sets the Overtemperature in Discharge Protection recovery threshold. Recovery occurs when the maximum cell temperature is less than or equal to this threshold for ***Protections:Recovery:Time*** seconds.

### *7.6.5.14 Protections:OTF*

#### 7.6.5.14.1 Protections:OTF:Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | OTF | Threshold | U1 | 0 | 150 | 80 | °C |

**Description**: This parameter sets the FET Overtemperature threshold. When the FET temperature is greater than or equal to this threshold for ***Protections:OTF:Delay*** seconds, the protection is triggered.

#### 7.6.5.14.2 Protections:OTF:Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | OTF | Delay | U1 | 0 | 255 | 2 | s |

**Description**: This parameter sets the FET Overtemperature Protection delay. When the FET temperature is greater than or equal to ***Protections:OTF:Threshold*** for this many seconds, the protection is triggered.

#### 7.6.5.14.3 Protections:OTF:Recovery

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | OTF | Recovery | U1 | 0 | 150 | 65 | °C |

**Description**: This parameter sets the FET Overtemperature Protection recovery threshold. Recovery occurs when the FET temperature is less than or equal to this threshold for ***Protections:Recovery:Time*** seconds.

### *7.6.5.15 Protections:OTINT*

#### 7.6.5.15.1 Protections:OTINT:Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | OTINT | Threshold | I1 | –40 | 120 | 85 | °C |

**Description**: This parameter sets the Internal Overtemperature threshold. When the internal temperature is greater than or equal to this threshold for ***Protections:OTINT:Delay*** seconds, the protection is triggered.

#### 7.6.5.15.2 Protections:OTINT:Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | OTINT | Delay | U1 | 0 | 255 | 2 | s |

**Description**: This parameter sets the Internal Overtemperature Protection delay. When the internal temperature is greater than or equal to ***Protections:OTINT:Threshold*** for this many seconds, the protection is triggered.

#### 7.6.5.15.3 Protections:OTINT:Recovery

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | OTINT | Recovery | I1 | –40 | 120 | 80 | °C |

**Description**: This parameter sets the Internal Overtemperature Protection recovery threshold. Recovery occurs when the internal temperature is less than or equal to this threshold for ***Protections:Recovery:Time*** seconds.

### *7.6.5.16 Protections:UTC*

#### 7.6.5.16.1 Protections:UTC:Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | UTC | Threshold | I1 | –40 | 120 | 0 | °C |

**Description**: This parameter sets the Undertemperature in Charge Protection threshold. When the minimum cell temperature is less than or equal to this threshold for ***Protections:UTC:Delay*** seconds, the protection is triggered. Note: charging does not need to be occurring for this protection to trigger. It is intended to be the threshold at which charging should not be allowed, not an indicator of if charging happened at this temperature.

#### 7.6.5.16.2 Protections:UTC:Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | UTC | Delay | U1 | 0 | 255 | 2 | s |

**Description**: This parameter sets the Undertemperature in Charge Protection delay. When the minimum cell temperature is less than or equal to ***Protections:UTC:Threshold*** for this many seconds, the protection is triggered. Note: charging does not need to be occurring for this protection to trigger. It is intended to be the threshold at which charging should not be allowed, not an indicator of if charging happened at this temperature.

#### 7.6.5.16.3 Protections:UTC:Recovery

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | UTC | Recovery | I1 | –40 | 120 | 5 | °C |

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**Description**: This parameter sets the Undertemperature in Charge Protection recovery threshold. Recovery occurs when the minimum cell temperature is greater than or equal to this threshold for ***Protections:Recovery:Time*** seconds.

### *7.6.5.17 Protections:UTD*

#### 7.6.5.17.1 Protections:UTD:Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | UTD | Threshold | I1 | –40 | 120 | 0 | °C |

**Description**: This parameter sets the Undertemperature in Discharge Protection threshold. When the minimum cell temperature is less than or equal to this threshold for ***Protections:UTD:Delay*** seconds, the protection is triggered. Note: discharging does not need to be occurring for this protection to trigger. It is intended to be the threshold at which discharging should not be allowed, not an indicator of if discharging happened at this temperature.

#### 7.6.5.17.2 Protections:UTD:Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | UTD | Delay | U1 | 0 | 255 | 2 | s |

**Description**: This parameter sets the Undertemperature in Discharge Protection delay. When the minimum cell temperature is less than or equal to ***Protections:UTD:Threshold*** for this many seconds, the protection is triggered. Note: discharging does not need to be occurring for this protection to trigger. It is intended to be the threshold at which discharging should not be allowed, not an indicator of if discharging happened at this temperature.

#### 7.6.5.17.3 Protections:UTD:Recovery

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | UTD | Recovery | I1 | –40 | 120 | 5 | °C |

**Description**: This parameter sets the Undertemperature in Discharge Protection recovery threshold. Recovery occurs when the minimum cell temperature is greater than or equal to this threshold for ***Protections:Recovery:Time*** seconds.

### *7.6.5.18 Protections:UTINT*

#### 7.6.5.18.1 Protections:UTINT:Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | UTINT | Threshold | I1 | –40 | 120 | –20 | °C |

**Description**: This parameter sets the Internal Undertemperature threshold. When the internal temperature is less than or equal to this threshold for ***Protections:UTINT:Delay*** seconds, the protection is triggered.

#### 7.6.5.18.2 Protections:UTINT:Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | UTINT | Delay | U1 | 0 | 255 | 2 | s |

**Description**: This parameter sets the Internal Undertemperature Protection delay. When the internal temperature is less than or equal to ***Protections:UTINT:Threshold*** for this many seconds, the protection is triggered.

#### 7.6.5.18.3 Protections:UTINT:Recovery

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | UTINT | Recovery | I1 | –40 | 120 | –15 | °C |

**Description**: This parameter sets the Internal Undertemperature Protection recovery threshold. Recovery occurs when the internal temperature is greater than or equal to this threshold for ***Protections:Recovery:Time*** seconds.

### *7.6.5.19 Protections:Recovery*

#### 7.6.5.19.1 Protections:Recovery:Time

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | Recovery | Time | U1 | 0 | 255 | 3 | s |

**Description**: This parameter configures the recovery time used by several protections in units of seconds. The recovery criteria must be met for this delay for recovery to occur.

### *7.6.5.20 Protections:HWD*

#### 7.6.5.20.1 Protections:HWD:Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | HWD | Delay | U1 | 0 | 255 | 60 | s |

**Description**: This parameter configures the Host Watchdog timeout. If communications are not received for this many seconds, the Host Watchdog Fault is triggered.

### *7.6.5.21 Protections:Load Detect*

#### 7.6.5.21.1 Protections:Load Detect:Active Time

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | Load Detect | Active Time | U1 | 0 | 255 | 0 | s |

**Description**: The Short Circuit in Discharge Latch and Overcurrent in Discharge Latch protections can be configured to recover when the load removal is detected. The device can enable a current source on the LD pin and checks for the voltage level rising above 3V. This parameter controls how long the current source is enabled before waiting ***Protections:Load Detect:Retry Delay*** seconds and trying again. This should be set longer than ***Power:Sleep:Voltage Time*** to ensure that voltage is measured while the current source is enabled.

0 = Recovery based on Load Detect functionality is disabled.

All other values = Load Detect current source is enabled for this many seconds at a time.

#### 7.6.5.21.2 Protections:Load Detect:Retry Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | Load Detect | Retry Delay | U1 | 0 | 255 | 50 | s |

**Description**: The Short Circuit in Discharge Latch and Overcurrent in Discharge Latch protections can be configured to recover when the load removal is detected. The device can enable a current source on the LD pin and checks for the voltage level rising above 3 V. The current source is enabled only temporarily to save power. This parameter controls the delay between periods when the LD current source is active.

0 = Load Detect current source stays on until ***Protections:Load Detect:Timeout*** or recovery.

All other values = Load detect current source is disabled for this many seconds before trying again.

#### 7.6.5.21.3 Protections:Load Detect:Timeout

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | Load Detect | Timeout | U2 | 0 | 65535 | 1 | hrs |

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**Description**: To prevent the Load Detect function from indefinitely operating and draining the battery, a timeout may be configured. This timeout starts when Load Detect is first enabled to check recovery and is measured in hours. After this timeout, Load Detect is no longer checked until the latch faults have recovered or a command to retry is received.

#### *7.6.5.22 Protections:PTO*

##### 7.6.5.22.1 Protections:PTO:Charge Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | PTO | Charge Threshold | I2 | –32768 | 32767 | 250 | mA |

**Description**: This parameter sets the current threshold for the Precharge Timeout Protection. When in Precharge mode but the current is less than or equal to this threshold, the timeout timer is not incremented and the Precharge Timeout Suspend (PTOS) bit is set.

##### 7.6.5.22.2 Protections:PTO:Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | PTO | Delay | U2 | 0 | 65535 | 1800 | s |

**Description**: This parameter sets the Precharge Timeout threshold. When in Precharge mode with current above ***Protections:PTO:Charge Threshold***, a timer is incremented. If the timer reaches this value, the Precharge Timeout Protection is triggered. This should be set to a value sufficiently long enough for Precharge to complete and normal charge to start.

##### 7.6.5.22.3 Protections:PTO:Reset

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Protections | PTO | Reset | I2 | 0 | 10000 | 2 | userAh |

**Description**: The timer for the Precharge Timeout Protection is reset when a continuous discharge of this much capacity occurs. This discharge must be larger in magnitude than ***Settings:Current Thresholds:Dsg Current Threshold*** for long enough to accumulate this amount of charge. Note: the units of this parameter scale with the selected units for reported current (user-amps).

### 7.6.6 Permanent Fail

#### *7.6.6.1 Permanent Fail:CUDEP*

##### 7.6.6.1.1 Permanent Fail:CUDEP:Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Permanent Fail | CUDEP | Threshold | I2 | 0 | 32767 | 1500 | mV |

**Description**: When a cell is severely overdischarged, copper deposition can occur, resulting in very high impedance. Normally the device is shut down before the cells reach this low voltage, but in certain configurations the device may wake with a charger attached. If the FETs were turned on at this point, the voltage would rise sharply and the cells would appear to be fine due to the high charging current flowing. When enabled, the copper deposition check holds the FETs off until the voltage is greater than or equal to ***Permanent Fail:CUDEP:Threshold*** for ***Permanent Fail:CUDEP:Delay*** seconds. If the voltage is below ***Permanent Fail:CUDEP:Threshold*** for ***Permanent Fail:CUDEP:Delay*** seconds, the CUDEP Permanent Fail is triggered.

##### 7.6.6.1.2 Permanent Fail:CUDEP:Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Permanent Fail | CUDEP | Delay | U1 | 0 | 255 | 2 | s |

**Description**: When a cell is severely overdischarged, copper deposition can occur, resulting in very high impedance. Normally the device is shut down before the cells reach this low voltage, but in certain configurations the device may wake with a charger attached. If the FETs were turned on at this point, the voltage would rise sharply and the cells would appear to be fine due to the high charging current flowing. When enabled, the copper deposition check holds the FETs off until the voltage is greater than or equal to ***Permanent Fail:CUDEP:Threshold*** for ***Permanent Fail:CUDEP:Delay*** seconds. If the voltage is below ***Permanent Fail:CUDEP:Threshold*** for ***Permanent Fail:CUDEP:Delay*** seconds, the CUDEP Permanent Fail is triggered.

### *7.6.6.2 Permanent Fail:SUV*

#### 7.6.6.2.1 Permanent Fail:SUV:Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Permanent Fail | SUV | Threshold | I2 | 0 | 32767 | 2200 | mV |

**Description**: This parameter sets the Safety Undervoltage Permanent Fail threshold. When the minimum cell voltage is less than or equal to ***Permanent Fail:SUV:Threshold*** for ***Permanent Fail:SUV:Delay*** seconds, the SUV Permanent Fail is triggered.

#### 7.6.6.2.2 Permanent Fail:SUV:Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Permanent Fail | SUV | Delay | U1 | 0 | 255 | 5 | s |

**Description**: This parameter sets the Safety Undervoltage Permanent Fail delay. When the minimum cell voltage is less than or equal to***Permanent Fail:SUV:Threshold*** for ***Permanent Fail:SUV:Delay*** seconds, the SUV Permanent Fail is triggered.

### *7.6.6.3 Permanent Fail:SOV*

#### 7.6.6.3.1 Permanent Fail:SOV:Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Permanent Fail | SOV | Threshold | I2 | 0 | 32767 | 4500 | mV |

**Description**: This parameter sets the Safety Overvoltage Permanent Fail threshold. When the maximum cell voltage is greater than or equal to ***Permanent Fail:SOV:Threshold*** for ***Permanent Fail:SOV:Delay*** seconds, the SOV Permanent Fail is triggered.

#### 7.6.6.3.2 Permanent Fail:SOV:Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Permanent Fail | SOV | Delay | U1 | 0 | 255 | 5 | s |

**Description**: This parameter sets the Safety Undervoltage Permanent Fail delay. When the maximum cell voltage is greater than or equal to ***Permanent Fail:SOV:Threshold*** for ***Permanent Fail:SOV:Delay*** seconds, the SOV Permanent Fail is triggered.

### *7.6.6.4 Permanent Fail:TOS*

#### 7.6.6.4.1 Permanent Fail:TOS:Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Permanent Fail | TOS | Threshold | I2 | 0 | 32767 | 100 | mV |

ADVANCE INFORMATION

**Description**: This parameter sets the Top of Stack versus Cell Sum Permanent Fail threshold. The threshold is based on cell voltage, so it is multiplied by the number of used cells before the comparison. The device compares the measured Top of Stack voltage to the sum of individually measured cell voltages. When the absolute value of the difference is greater than or equal to the number of used cells times the ***Permanent Fail:TOS:Threshold*** for ***Permanent Fail:TOS:Delay*** seconds, the TOSF Permanent Fail is triggered. This check is skipped when the current reading during any of these voltage measurements is above ***Power:Sleep:Sleep Current*** to avoid false triggers due to changing loads.

#### 7.6.6.4.2 Permanent Fail:TOS:Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Permanent Fail | TOS | Delay | U1 | 0 | 255 | 5 | s |

**Description**: This parameter sets the Top of Stack versus Cell Sum Permanent Fail threshold. The device compares the measured Top of Stack voltage to the sum of individually measured cell voltages. When the absolute value of the difference is greater than or equal to the number of used cells times the ***Permanent Fail:TOS:Threshold*** for ***Permanent Fail:TOS:Delay*** seconds, the TOSF Permanent Fail is triggered. This check is skipped when the current reading during any of these voltage measurements is above ***Power:Sleep:Sleep Current*** to avoid false triggers due to changing loads.

### *7.6.6.5 Permanent Fail:SOCC*

#### 7.6.6.5.1 Permanent Fail:SOCC:Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Permanent Fail | SOCC | Threshold | I2 | –32768 | 32767 | 10000 | userA |

**Description**: This parameter sets the Safety Overcurrent in Charge Permanent Fail threshold. When the measured current is greater than or equal to ***Permanent Fail:SOCC:Threshold*** for ***Permanent Fail:SOCC:Delay*** seconds, the SOCC Permanent Fail is triggered.

#### 7.6.6.5.2 Permanent Fail:SOCC:Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Permanent Fail | SOCC | Delay | U1 | 0 | 255 | 5 | s |

**Description**: This parameter sets the Safety Overcurrent in Charge Permanent Fail delay. When the measured current is greater than or equal to ***Permanent Fail:SOCC:Threshold*** for ***Permanent Fail:SOCC:Delay*** seconds, the SOCC Permanent Fail is triggered.

### *7.6.6.6 Permanent Fail:SOCD*

#### 7.6.6.6.1 Permanent Fail:SOCD:Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Permanent Fail | SOCD | Threshold | I2 | –32768 | 32767 | –32000 | userA |

**Description**: This parameter sets the Safety Overcurrent in Discharge Permanent Fail threshold. When the measured current is greater than or equal to ***Permanent Fail:SOCD:Threshold*** for ***Permanent Fail:SOCD:Delay*** seconds, the SOCD Permanent Fail is triggered.

#### 7.6.6.6.2 Permanent Fail:SOCD:Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Permanent Fail | SOCD | Delay | U1 | 0 | 255 | 5 | s |

**Description**: This parameter sets the Safety Overcurrent in Discharge Permanent Fail delay. When the measured current is greater than or equal to ***Permanent Fail:SOCD:Threshold*** for ***Permanent Fail:SOCD:Delay*** seconds, the SOCD Permanent Fail is triggered.

### *7.6.6.7 Permanent Fail:SOT*

#### 7.6.6.7.1 Permanent Fail:SOT:Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Permanent Fail | SOT | Threshold | I1 | –40 | 120 | 65 | °C |

**Description**: This parameter sets the Safety Overtemperature Permanent Fail threshold. When the maximum cell temperature is greater than or equal to ***Permanent Fail:SOT:Threshold*** for ***Permanent Fail:SOT:Delay*** seconds, the SOT Permanent Fail is triggered.

#### 7.6.6.7.2 Permanent Fail:SOT:Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Permanent Fail | SOT | Delay | U1 | 0 | 255 | 5 | s |

**Description**: This parameter sets the Safety Overtemperature Permanent Fail delay. When the maximum cell temperature is greater than or equal to ***Permanent Fail:SOT:Threshold*** for ***Permanent Fail:SOT:Delay*** seconds, the SOT Permanent Fail is triggered.

### *7.6.6.8 Permanent Fail:SOTF*

#### 7.6.6.8.1 Permanent Fail:SOTF:Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Permanent Fail | SOTF | Threshold | U1 | 0 | 150 | 85 | °C |

**Description**: This parameter sets the Safety Overtemperature FET Permanent Fail threshold. When the FET temperature is greater than or equal to ***Permanent Fail:SOTF:Threshold*** for ***Permanent Fail:SOTF:Delay*** seconds, the SOTF Permanent Fail is triggered.

#### 7.6.6.8.2 Permanent Fail:SOTF:Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Permanent Fail | SOTF | Delay | U1 | 0 | 255 | 5 | s |

**Description**: This parameter sets the Safety Overtemperature FET Permanent Fail delay. When the FET temperature is greater than or equal to ***Permanent Fail:SOTF:Threshold*** for ***Permanent Fail:SOTF:Delay*** seconds, the SOTF Permanent Fail is triggered.

### *7.6.6.9 Permanent Fail:VIMR*

#### 7.6.6.9.1 Permanent Fail:VIMR:Check Voltage

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Permanent Fail | VIMR | Check Voltage | I2 | 0 | 5500 | 3500 | mV |

ADVANCE INFORMATION

**Description**: The Voltage Imbalance at Rest Permanent Fail is not checked when the maximum cell voltage is less than this threshold. This is because at lower states of charge, the voltage differences for a smaller imbalance are amplified.

#### 7.6.6.9.2 Permanent Fail:VIMR:Max Relax Current

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Permanent Fail | VIMR | Max Relax Current | I2 | 10 | 32767 | 10 | mA |

**Description**: The Voltage Imbalance at Rest Permanent Fail is not checked when the absolute value of measured current is greater than or equal to this threshold.

#### 7.6.6.9.3 Permanent Fail:VIMR:Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Permanent Fail | VIMR | Threshold | I2 | 0 | 5500 | 500 | mV |

**Description**: This parameter sets the Voltage Imbalance at Rest Permanent Fail threshold. When the delta between the maximum and minimum cell voltages is greater than or equal to ***Permanent Fail:VIMR:Threshold*** for ***Permanent Fail:VIMR:Delay*** seconds while VIMR check conditions are met, the VIMR Permanent Fail is triggered.

#### 7.6.6.9.4 Permanent Fail:VIMR:Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Permanent Fail | VIMR | Delay | U1 | 0 | 255 | 5 | s |

**Description**: This parameter sets the Voltage Imbalance at Rest Permanent Fail delay. When the delta between the maximum and minimum cell voltages is greater than or equal to ***Permanent Fail:VIMR:Threshold*** for ***Permanent Fail:VIMR:Delay*** seconds while VIMR check conditions are met, the VIMR Permanent Fail is triggered.

#### 7.6.6.9.5 Permanent Fail:VIMR:Relax Min Duration

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Permanent Fail | VIMR | Relax Min Duration | U2 | 0 | 65535 | 100 | s |

**Description**: The Voltage Imbalance at Rest Permanent Fail is not checked unless the ***Permanent Fail:VIMR:Check Voltage*** and ***Permanent Fail:VIMR:Max Relax Current*** conditions have been met for this duration.

### *7.6.6.10 Permanent Fail:VIMA*

#### 7.6.6.10.1 Permanent Fail:VIMA:Check Voltage

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Permanent Fail | VIMA | Check Voltage | I2 | 0 | 5500 | 3700 | mV |

**Description**: The Voltage Imbalance Active Permanent Fail is not checked when the maximum cell voltage is less than this threshold. This is because at lower states of charge, the voltage differences for a smaller imbalance are amplified.

#### 7.6.6.10.2 Permanent Fail:VIMA:Min Active Current

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Permanent Fail | VIMA | Min Active Current | I2 | 10 | 32767 | 50 | mA |

ADVANCE INFORMATION

**Description**: The Voltage Imbalance Active Permanent Fail is not checked when the absolute value of measured current is less than this threshold.

#### 7.6.6.10.3 Permanent Fail:VIMA:Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Permanent Fail | VIMA | Threshold | I2 | 0 | 5500 | 200 | mV |

**Description**: This parameter sets the Voltage Imbalance Active Permanent Fail threshold. When the delta between the maximum and minimum cell voltages is greater than or equal to ***Permanent Fail:VIMA:Threshold*** for ***Permanent Fail:VIMA:Delay*** seconds while VIMA check conditions are met, the VIMA Permanent Fail is triggered.

#### 7.6.6.10.4 Permanent Fail:VIMA:Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Permanent Fail | VIMA | Delay | U1 | 0 | 255 | 5 | s |

**Description**: This parameter sets the Voltage Imbalance Active Permanent Fail delay. When the delta between the maximum and minimum cell voltages is greater than or equal to ***Permanent Fail:VIMA:Threshold*** for ***Permanent Fail:VIMA:Delay*** seconds while VIMA check conditions are met, the VIMA Permanent Fail is triggered.

### *7.6.6.11 Permanent Fail:CFETF*

#### 7.6.6.11.1 Permanent Fail:CFETF:OFF Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Permanent Fail | CFETF | OFF Threshold | I2 | 10 | 5000 | 20 | mA |

**Description**: This parameter sets the Charge FET Permanent Fail current threshold. When the measured current is greater than or equal to ***Permanent Fail:CFETF:OFF Threshold*** for ***Permanent Fail:CFETF:OFF Delay*** seconds while the CHG FET is off, the CFETF Permanent Fail is triggered.

#### 7.6.6.11.2 Permanent Fail:CFETF:OFF Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Permanent Fail | CFETF | OFF Delay | U1 | 0 | 255 | 5 | s |

**Description**: This parameter sets the Charge FET Permanent Fail delay. When the measured current is greater than or equal to ***Permanent Fail:CFETF:OFF Threshold*** for ***Permanent Fail:CFETF:OFF Delay*** seconds while the CHG FET is off, the CFETF Permanent Fail is triggered.

### *7.6.6.12 Permanent Fail:DFETF*

#### 7.6.6.12.1 Permanent Fail:DFETF:OFF Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Permanent Fail | DFETF | OFF Threshold | I2 | –5000 | –10 | –20 | mA |

ADVANCE INFORMATION

**Description**: This parameter sets the Discharge FET Permanent Fail current threshold. When the measured current is less (more negative) than or equal to ***Permanent Fail:DFETF:OFF Threshold*** for ***Permanent Fail:DFETF:OFF Delay*** seconds while the DSG FET is off, the DFETF Permanent Fail is triggered.

#### 7.6.6.12.2 Permanent Fail:DFETF:OFF Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Permanent Fail | DFETF | OFF Delay | U1 | 0 | 255 | 5 | s |

**Description**: This parameter sets the Discharge FET Permanent Fail delay. When the measured current is less (more negative) than or equal to ***Permanent Fail:DFETF:OFF Threshold*** for ***Permanent Fail:DFETF:OFF Delay*** seconds while the DSG FET is off, the DFETF Permanent Fail is triggered.

### *7.6.6.13 Permanent Fail:VSSF*

#### 7.6.6.13.1 Permanent Fail:VSSF:Fail Threshold

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Permanent Fail | VSSF | Fail Threshold | I2 | 1 | 32767 | 100 | — |

**Description**: This parameter sets the Internal VSS Measurement Permanent Fail threshold. When the ADC count value measured for the internal VSS channel is greater than or equal to ***Permanent Fail:VSSF:Fail Threshold*** for ***Permanent Fail:VSSF:Delay*** seconds, the VSSF Permanent Fail is triggered.

#### 7.6.6.13.2 Permanent Fail:VSSF:Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Permanent Fail | VSSF | Delay | U1 | 0 | 255 | 5 | s |

**Description**: This parameter sets the Internal VSS Measurement Permanent Fail delay. When the ADC count value measured for the internal VSS channel is greater than or equal to ***Permanent Fail:VSSF:Fail Threshold*** for ***Permanent Fail:VSSF:Delay*** seconds, the VSSF Permanent Fail is triggered.

### *7.6.6.14 Permanent Fail:2LVL*

#### 7.6.6.14.1 Permanent Fail:2LVL:Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Permanent Fail | 2LVL | Delay | U1 | 0 | 255 | 5 | s |

**Description**: This parameter sets the Second Level Protector Permanent Fail delay. The device checks the FUSE pin each second, and if it is asserted by the second level protector for ***Permanent Fail:2LVL:Delay*** seconds, the 2LVL PF is triggered.

### *7.6.6.15 Permanent Fail:LFOF*

#### 7.6.6.15.1 Permanent Fail:LFOF:Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Permanent Fail | LFOF | Delay | U1 | 0 | 255 | 5 | s |

**Description**: This parameter sets the Internal LFO Permanent Fail delay. The device monitors the output of its Low-Frequency Oscillator integrity check. If the error bit is set for ***Permanent Fail:LFOF:Delay*** seconds, the LFOF Permanent Failure is triggered.

#### *7.6.6.16 Permanent Fail:HWMX*

##### 7.6.6.16.1 Permanent Fail:HWMX:Delay

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Permanent Fail | HWMX | Delay | U1 | 0 | 255 | 5 | s |

**Description**: This parameter sets the Hardware Mux Permanent Fail delay. The device periodically performs an integrity check of the input mux for the hardware protection comparator subsystem, which is used for the OV, UV, OCC, OCD1, and OCD2 primary protections. If this check fails for ***Permanent Fail:HWMX:Delay*** seconds, the Hardware Mux Permanent Failure is triggered.

### 7.6.7 Security

#### *7.6.7.1 Security:Settings*

##### 7.6.7.1.1 Security:Settings:Security Settings

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Security | Settings | Security Settings | H1 | 0x00 | 0x07 | 0x00 | Hex |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | RSVD_0 | PERM_SEAL | LOCK_CFG | SEAL |

**Description**: This parameter contains security-related configuration options.

**Table 104. Security Settings Register Field Descriptions**

| Bit | Field | Default | Description |
|---|---|---|---|
| 2 | PERM_SEAL | 0 | Setting this bit prevents unsealing the device once it is sealed. If this is not programmed to OTP, this setting will be lost on a full reset and the device will again be able to UNSEAL.<br>0 = The device can be unsealed by sending the correct security keys.<br>1 = The device cannot be unsealed. |
| 1 | LOCK_CFG | 0 | Setting this bit prevents entry into CONFIG_UPDATE and FULLACCESS modes. This prevents further modifications to the device configuration after CONFIG_UPDATE mode is exited.<br>0 = Configuration parameters can be changed in CONFIG_UPDATE mode.<br>1 = Configuration parameters cannot be changed. |
| 0 | SEAL | 0 | Setting this bit causes the device to enter SEALED mode when reset or exiting CONFIG_UPDATE and DEEPSLEEP modes. In production systems, this bit should be set for security purposes.<br>0 = Device does not default to SEALED mode.<br>1 = Device default state is SEALED. |

#### *7.6.7.2 Security:Keys*

##### 7.6.7.2.1 Security:Keys:Unseal Key Step 1

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Security | Keys | Unseal Key Step 1 | U2 | 0x0100 | 0xFFFF | 0x0414 | Hex |

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**Description**: This is the first word of the security key that must be sent to transition from SEALED to UNSEALED mode.

#### 7.6.7.2.2 Security:Keys:Unseal Key Step 2

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Security | Keys | Unseal Key Step 2 | U2 | 0x0100 | 0xFFFF | 0x3672 | Hex |

**Description**: This is the second word of the security key that must be sent to transition from SEALED to UNSEALED mode. It must be sent within 5 seconds of the first word of the key and with no other commands in between.

#### 7.6.7.2.3 Security:Keys:Full Access Key Step 1

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Security | Keys | Full Access Key Step 1 | U2 | 0x0100 | 0xFFFF | 0xFFFF | Hex |

**Description**: This is the second word of the security key that must be sent to transition from UNSEALED to FULLACCESS mode.

#### 7.6.7.2.4 Security:Keys:Full Access Key Step 2

| Class | Subclass | Name | Type | Min | Max | Default | Unit |
|---|---|---|---|---|---|---|---|
| Security | Keys | Full Access Key Step 2 | U2 | 0x0100 | 0xFFFF | 0xFFFF | Hex |

**Description**: This is the second word of the security key that must be sent to transition from UNSEALED to FULLACCESS mode. It must be sent within 5 seconds of the first word of the key and with no other commands in between.

### 7.6.8 Data Memory Summary

**Table 105. Data Memory Table**

| Class | Subclass | Address | Name | Type | Min Value | Max Value | Default | Units |
|---|---|---|---|---|---|---|---|---|
| Calibration | Voltage | 0x9180 | Cell 1 Gain | I2 | –32767 | 32767 | 0 | — |
| Calibration | Voltage | 0x9182 | Cell 2 Gain | I2 | –32767 | 32767 | 0 | — |
| Calibration | Voltage | 0x9184 | Cell 3 Gain | I2 | –32767 | 32767 | 0 | — |
| Calibration | Voltage | 0x9186 | Cell 4 Gain | I2 | –32767 | 32767 | 0 | — |
| Calibration | Voltage | 0x9188 | Cell 5 Gain | I2 | –32767 | 32767 | 0 | — |
| Calibration | Voltage | 0x918A | Cell 6 Gain | I2 | –32767 | 32767 | 0 | — |
| Calibration | Voltage | 0x918C | Cell 7 Gain | I2 | –32767 | 32767 | 0 | — |
| Calibration | Voltage | 0x918E | Cell 8 Gain | I2 | –32767 | 32767 | 0 | — |
| Calibration | Voltage | 0x9190 | Cell 9 Gain | I2 | –32767 | 32767 | 0 | — |
| Calibration | Voltage | 0x9192 | Cell 10 Gain | I2 | –32767 | 32767 | 0 | — |
| Calibration | Voltage | 0x91A0 | Pack Gain | U2 | 0 | 65535 | 35507 | — |
| Calibration | Voltage | 0x91A2 | TOS Gain | U2 | 0 | 65535 | 35507 | — |
| Calibration | Voltage | 0x91A4 | LD Gain | U2 | 0 | 65535 | 35507 | — |
| Calibration | Voltage | 0x91A6 | ADC Gain | I2 | –32767 | 32767 | 0 | — |
| Calibration | Current | 0x91A8 | CC Gain | F4 | 1.00E–01 | 10.00E+00 | 7.4768 | — |
| Calibration | Current | 0x91AC | Capacity Gain | F4 | 2.98262E+04 | 4.193046E+06 | 2230042.463 | — |
| Calibration | Vcell Offset | 0x91B0 | Vcell Offset | I2 | –32767 | 32767 | 0 | mV |
| Calibration | V Divider Offset | 0x91B2 | Vdiv Offset | I2 | –32767 | 32767 | 0 | userV |
| Calibration | Current Offset | 0x91B6 | Coulomb Counter Offset Samples | U2 | 0 | 65535 | 64 | — |
| Calibration | Current Offset | 0x91B8 | Board Offset | I2 | –32768 | 32767 | 0 | — |
| Calibration | Temperature | 0x91BA | Internal Temp Offset | I1 | –128 | 127 | 0 | 0.1°C |
| Calibration | Temperature | 0x91BB | CFETOFF Temp Offset | I1 | –128 | 127 | 0 | 0.1°C |
| Calibration | Temperature | 0x91BC | DFETOFF Temp Offset | I1 | –128 | 127 | 0 | 0.1°C |

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**Table 105. Data Memory Table (continued)**

| Class | Subclass | Address | Name | Type | Min Value | Max Value | Default | Units |
|---|---|---|---|---|---|---|---|---|
| Calibration | Temperature | 0x91BD | ALERT Temp Offset | I1 | –128 | 127 | 0 | 0.1°C |
| Calibration | Temperature | 0x91BE | TS1 Temp Offset | I1 | –128 | 127 | 0 | 0.1°C |
| Calibration | Temperature | 0x91BF | TS2 Temp Offset | I1 | –128 | 127 | 0 | 0.1°C |
| Calibration | Temperature | 0x91C0 | TS3 Temp Offset | I1 | –128 | 127 | 0 | 0.1°C |
| Calibration | Temperature | 0x91C1 | HDQ Temp Offset | I1 | –128 | 127 | 0 | 0.1°C |
| Calibration | Temperature | 0x91C2 | DCHG Temp Offset | I1 | –128 | 127 | 0 | 0.1°C |
| Calibration | Temperature | 0x91C3 | DDSG Temp Offset | I1 | –128 | 127 | 0 | 0.1°C |
| Calibration | Internal Temp Model | 0x91C6 | Int Gain | I2 | –32768 | 32767 | 25390 | — |
| Calibration | Internal Temp Model | 0x91C8 | Int base offset | I2 | –32768 | 32767 | 33 | — |
| Calibration | Internal Temp Model | 0x91CA | Int Maximum AD | I2 | –32768 | 32767 | 16383 | — |
| Calibration | Internal Temp Model | 0x91CC | Int Maximum Temp | I2 | 0 | 32767 | 6379 | 0.1K |
| Calibration | 18K Temperature Model | 0x91CE | Coeff a1 | I2 | –32768 | 32767 | –11130 | — |
| Calibration | 18K Temperature Model | 0x91D0 | Coeff a2 | I2 | –32768 | 32767 | 19142 | — |
| Calibration | 18K Temperature Model | 0x91D2 | Coeff a3 | I2 | –32768 | 32767 | –19262 | — |
| Calibration | 18K Temperature Model | 0x91D4 | Coeff a4 | I2 | –32768 | 32767 | 28203 | — |
| Calibration | 18K Temperature Model | 0x91D6 | Coeff a5 | I2 | –32768 | 32767 | 892 | — |
| Calibration | 18K Temperature Model | 0x91D8 | Coeff b1 | I2 | –32768 | 32767 | 328 | — |
| Calibration | 18K Temperature Model | 0x91DA | Coeff b2 | I2 | –32768 | 32767 | –605 | — |
| Calibration | 18K Temperature Model | 0x91DC | Coeff b3 | I2 | –32768 | 32767 | –2443 | — |
| Calibration | 18K Temperature Model | 0x91DE | Coeff b4 | I2 | –32768 | 32767 | 4696 | — |
| Calibration | 18K Temperature Model | 0x91E2 | Adc0 | I2 | –32768 | 32767 | 11703 | — |
| Calibration | 180K Temperature Model | 0x91E4 | Coeff a1 | I2 | –32768 | 32767 | –17513 | — |
| Calibration | 180K Temperature Model | 0x91E6 | Coeff a2 | I2 | –32768 | 32767 | 25759 | — |
| Calibration | 180K Temperature Model | 0x91E8 | Coeff a3 | I2 | –32768 | 32767 | –23593 | — |
| Calibration | 180K Temperature Model | 0x91EA | Coeff a4 | I2 | –32768 | 32767 | 32175 | — |
| Calibration | 180K Temperature Model | 0x91EC | Coeff a5 | I2 | –32768 | 32767 | 2090 | — |
| Calibration | 180K Temperature Model | 0x91EE | Coeff b1 | I2 | –32768 | 32767 | –2055 | — |
| Calibration | 180K Temperature Model | 0x91F0 | Coeff b2 | I2 | –32768 | 32767 | 2955 | — |
| Calibration | 180K Temperature Model | 0x91F2 | Coeff b3 | I2 | –32768 | 32767 | –3427 | — |
| Calibration | 180K Temperature Model | 0x91F4 | Coeff b4 | I2 | –32768 | 32767 | 4385 | — |
| Calibration | 180K Temperature Model | 0x91F8 | Adc0 | I2 | –32768 | 32767 | 17246 | — |
| Calibration | Custom Temperature Model | 0x91FA | Coeff a1 | I2 | –32768 | 32767 | 0 | — |
| Calibration | Custom Temperature Model | 0x91FC | Coeff a2 | I2 | –32768 | 32767 | 0 | — |
| Calibration | Custom Temperature Model | 0x91FE | Coeff a3 | I2 | –32768 | 32767 | 0 | — |

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**Table 105. Data Memory Table (continued)**

| Class | Subclass | Address | Name | Type | Min Value | Max Value | Default | Units |
|---|---|---|---|---|---|---|---|---|
| Calibration | Custom Temperature Model | 0x9200 | Coeff a4 | I2 | –32768 | 32767 | 0 | — |
| Calibration | Custom Temperature Model | 0x9202 | Coeff a5 | I2 | –32768 | 32767 | 0 | — |
| Calibration | Custom Temperature Model | 0x9204 | Coeff b1 | I2 | –32768 | 32767 | 0 | — |
| Calibration | Custom Temperature Model | 0x9206 | Coeff b2 | I2 | –32768 | 32767 | 0 | — |
| Calibration | Custom Temperature Model | 0x9208 | Coeff b3 | I2 | –32768 | 32767 | 0 | — |
| Calibration | Custom Temperature Model | 0x920A | Coeff b4 | I2 | –32768 | 32767 | 0 | — |
| Calibration | Custom Temperature Model | 0x920C | Rc0 | I2 | –32768 | 32767 | 0 | — |
| Calibration | Custom Temperature Model | 0x920E | Adc0 | I2 | –32768 | 32767 | 0 | — |
| Calibration | Current Deadband | 0x9211 | Coulomb Counter Deadband | U1 | 0 | 255 | 9 | 234 nV |
| Settings | Fuse | 0x9215 | Min Blow Fuse Voltage | I2 | 0 | 32767 | 500 | cV |
| Settings | Fuse | 0x9217 | Fuse Blow Timeout | U1 | 0 | 255 | 30 | s |
| Settings | Configuration | 0x9218 | Power Config | H2 | 0x0000 | 0xFFFF | 0x0182 | Hex |
| Settings | Configuration | 0x921A | REG12 Config | H1 | 0x00 | 0xFF | 0x00 | Hex |
| Settings | Configuration | 0x921B | REG0 Config | H1 | 0x00 | 0x01 | 0x00 | Hex |
| Settings | Configuration | 0x921C | HWD Regulator Options | H1 | 0x00 | 0xFF | 0x00 | Hex |
| Settings | Configuration | 0x921D | Comm Type | U1 | 0x00 | 0x1F | 0 | — |
| Settings | Configuration | 0x921E | I2C Address | U1 | 0x00 | 0xFF | 0 | — |
| Settings | Configuration | 0x9221 | Comm Idle Time | U1 | 0 | 255 | 0 | s |
| Settings | Configuration | 0x92E0 | CFETOFF Pin Config | H1 | 0x00 | 0xFF | 0x00 | Hex |
| Settings | Configuration | 0x92E1 | DFETOFF Pin Config | H1 | 0x00 | 0xFF | 0x00 | Hex |
| Settings | Configuration | 0x92E2 | ALERT Pin Config | H1 | 0x00 | 0xFF | 0x00 | Hex |
| Settings | Configuration | 0x92E3 | TS1 Config | H1 | 0x00 | 0xFF | 0x07 | Hex |
| Settings | Configuration | 0x92E4 | TS2 Config | H1 | 0x00 | 0xFF | 0x00 | Hex |
| Settings | Configuration | 0x92E5 | TS3 Config | H1 | 0x00 | 0xFF | 0x00 | Hex |
| Settings | Configuration | 0x92E6 | HDQ Pin Config | H1 | 0x00 | 0xFF | 0x00 | Hex |
| Settings | Configuration | 0x92E7 | DCHG Pin Config | H1 | 0x00 | 0xFF | 0x00 | Hex |
| Settings | Configuration | 0x92E8 | DDSG Pin Config | H1 | 0x00 | 0xFF | 0x00 | Hex |
| Settings | Configuration | 0x92E9 | DA Configuration | H1 | 0x00 | 0xFF | 0x05 | Hex |
| Settings | Configuration | 0x92EA | Vcell Mode | H2 | 0x0000 | 0x03FF | 0x001F | Hex |
| Settings | Configuration | 0x92EC | CC3 Samples | U1 | 2 | 255 | 80 | Num |
| Settings | Protection | 0x9241 | Protection Configuration | H2 | 0x0000 | 0x07FF | 0x0002 | Hex |
| Settings | Protection | 0x9243 | Enabled Protections A | U1 | 0x00 | 0xFF | 0x88 | Hex |
| Settings | Protection | 0x9244 | Enabled Protections B | U1 | 0x00 | 0xFF | 0x00 | Hex |
| Settings | Protection | 0x9245 | Enabled Protections C | U1 | 0x00 | 0xFF | 0x00 | Hex |
| Settings | Protection | 0x9247 | CHG FET Protections A | U1 | 0x00 | 0xFF | 0x98 | Hex |
| Settings | Protection | 0x9248 | CHG FET Protections B | U1 | 0x00 | 0xFF | 0xD5 | Hex |
| Settings | Protection | 0x9249 | CHG FET Protections C | U1 | 0x00 | 0xFF | 0x56 | Hex |
| Settings | Protection | 0x924B | DSG FET Protections A | U1 | 0x00 | 0xFF | 0xE4 | Hex |
| Settings | Protection | 0x924C | DSG FET Protections B | U1 | 0x00 | 0xFF | 0xE6 | Hex |
| Settings | Protection | 0x924D | DSG FET Protections C | U1 | 0x00 | 0xFF | 0xE2 | Hex |
| Settings | Protection | 0x9255 | Body Diode Threshold | I2 | 0 | 32767 | 50 | mA |
| Settings | Alarm | 0x924F | Default Alarm Mask | H2 | 0x0000 | 0xFFFF | 0xF800 | Hex |
| Settings | Alarm | 0x9251 | SF Alert Mask A | U1 | 0x00 | 0xFF | 0xFC | Hex |
| Settings | Alarm | 0x9252 | SF Alert Mask B | U1 | 0x00 | 0xFF | 0xF7 | Hex |
| Settings | Alarm | 0x9253 | SF Alert Mask C | U1 | 0x00 | 0xFF | 0xF6 | Hex |
| Settings | Alarm | 0x92A2 | PF Alert Mask A | U1 | 0x00 | 0xFF | 0x5F | Hex |

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**Table 105. Data Memory Table (continued)**

| Class | Subclass | Address | Name | Type | Min Value | Max Value | Default | Units |
|---|---|---|---|---|---|---|---|---|
| Settings | Alarm | 0x92A3 | PF Alert Mask B | U1 | 0x00 | 0xFF | 0x9F | Hex |
| Settings | Alarm | 0x92A4 | PF Alert Mask C | U1 | 0x00 | 0xFF | 0x00 | Hex |
| Settings | Alarm | 0x92A5 | PF Alert Mask D | U1 | 0x00 | 0xFF | 0x00 | Hex |
| Settings | Permanent Failure | 0x929E | Enabled PF A | U1 | 0x00 | 0xFF | 0x00 | Hex |
| Settings | Permanent Failure | 0x929F | Enabled PF B | U1 | 0x00 | 0xFF | 0x00 | Hex |
| Settings | Permanent Failure | 0x92A0 | Enabled PF C | U1 | 0x00 | 0xFF | 0x07 | Hex |
| Settings | Permanent Failure | 0x92A1 | Enabled PF D | U1 | 0x00 | 0xFF | 0x00 | Hex |
| Settings | FET | 0x92ED | FET Options | H1 | 0x00 | 0xFF | 0x09 | Hex |
| Settings | FET | 0x92EE | Chg Pump Control | U1 | 0x00 | 0xFF | 0x01 | Hex |
| Settings | FET | 0x92EF | Precharge Start Voltage | I2 | 0 | 32767 | 0 | mV |
| Settings | FET | 0x92F1 | Precharge Stop Voltage | I2 | 0 | 32767 | 0 | mV |
| Settings | FET | 0x92F3 | Predischarge Timeout | U1 | 0 | 255 | 5 | 10 ms |
| Settings | FET | 0x92F4 | Predischarge Stop Delta | U1 | 0 | 255 | 50 | cV |
| Settings | Current Thresholds | 0x92F5 | Dsg Current Threshold | I2 | 0 | 32767 | 100 | userA |
| Settings | Current Thresholds | 0x92F7 | Chg Current Threshold | I2 | 0 | 32767 | 50 | userA |
| Settings | Cell Open-Wire | 0x92F9 | Check Time | U1 | 0 | 255 | 5 | s |
| Settings | Interconnect Resistances | 0x92FA | Cell 1 Interconnect | I2 | 0 | 32767 | 0 | mΩ |
| Settings | Interconnect Resistances | 0x92FC | Cell 2 Interconnect | I2 | 0 | 32767 | 0 | mΩ |
| Settings | Interconnect Resistances | 0x92FE | Cell 3 Interconnect | I2 | 0 | 32767 | 0 | mΩ |
| Settings | Interconnect Resistances | 0x9300 | Cell 4 Interconnect | I2 | 0 | 32767 | 0 | mΩ |
| Settings | Interconnect Resistances | 0x9302 | Cell 5 Interconnect | I2 | 0 | 32767 | 0 | mΩ |
| Settings | Interconnect Resistances | 0x9304 | Cell 6 Interconnect | I2 | 0 | 32767 | 0 | mΩ |
| Settings | Interconnect Resistances | 0x9306 | Cell 7 Interconnect | I2 | 0 | 32767 | 0 | mΩ |
| Settings | Interconnect Resistances | 0x9308 | Cell 8 Interconnect | I2 | 0 | 32767 | 0 | mΩ |
| Settings | Interconnect Resistances | 0x930A | Cell 9 Interconnect | I2 | 0 | 32767 | 0 | mΩ |
| Settings | Interconnect Resistances | 0x930C | Cell 10 Interconnect | I2 | 0 | 32767 | 0 | mΩ |
| Settings | Manufacturing | 0x9324 | Mfg Status Init | H2 | 0x0000 | 0xFFFF | 0x0040 | Hex |
| Settings | Cell Balancing Config | 0x931A | Balancing Configuration | H1 | 0x00 | 0xFF | 0x00 | Hex |
| Settings | Cell Balancing Config | 0x931B | Min Cell Temp | I1 | –128 | 127 | –20 | °C |
| Settings | Cell Balancing Config | 0x931C | Max Cell Temp | I1 | –128 | 127 | 60 | °C |
| Settings | Cell Balancing Config | 0x931D | Cell Balance Interval | U1 | 1 | 255 | 20 | s |
| Settings | Cell Balancing Config | 0x931E | Cell Balance Min Cell V (Charge) | I2 | 0 | 5000 | 3900 | mV |
| Settings | Cell Balancing Config | 0x9320 | Cell Balance Min Delta (Charge) | U1 | 0 | 255 | 40 | mV |
| Settings | Cell Balancing Config | 0x9321 | Cell Balance Min Cell V (Relax) | I2 | 0 | 5000 | 3900 | mV |
| Settings | Cell Balancing Config | 0x9323 | Cell Balance Min Delta (Relax) | U1 | 0 | 255 | 40 | mV |
| Power | Shutdown | 0x9223 | Shutdown Cell Voltage | I2 | 0 | 32767 | 0 | mV |
| Power | Shutdown | 0x9225 | Shutdown Stack Voltage | I2 | 0 | 32767 | 600 | cV |
| Power | Shutdown | 0x9227 | Shutdown Temperature | U1 | 0 | 150 | 85 | °C |
| Power | Shutdown | 0x9228 | Shutdown Temperature Delay | U1 | 0 | 254 | 5 | s |

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**Table 105. Data Memory Table (continued)**

| Class | Subclass | Address | Name | Type | Min Value | Max Value | Default | Units |
|---|---|---|---|---|---|---|---|---|
| Power | Shutdown | 0x9229 | Charger Present Threshold | I2 | 0 | 32767 | 300 | cV |
| Power | Shutdown | 0x9234 | FET Off Delay | U1 | 0 | 127 | 0 | 0.25s |
| Power | Shutdown | 0x9235 | Shutdown Command Delay | U1 | 0 | 254 | 0 | 0.25s |
| Power | Shutdown | 0x9236 | Auto Shutdown Time | U1 | 0 | 250 | 0 | min |
| Power | Shutdown | 0x9237 | RAM Fail Shutdown Time | U1 | 0 | 255 | 5 | s |
| Power | Sleep | 0x922B | Sleep Current | I2 | 0 | 32767 | 20 | mA |
| Power | Sleep | 0x922D | Voltage Time | U1 | 1 | 20 | 5 | s |
| Power | Sleep | 0x922E | Wake Comparator Current | I2 | 500 | 32767 | 500 | mA |
| Power | Sleep | 0x9230 | Sleep Hysteresis Time | U1 | 0 | 255 | 10 | s |
| Power | Sleep | 0x9231 | Sleep Charger Voltage Threshold | I2 | 0 | 32767 | 2000 | cV |
| Power | Sleep | 0x9233 | Sleep Charger PACK-TOS Delta | U1 | 10 | 255 | 10 | cV |
| System Data | Integrity | 0x91C4 | Config RAM Signature | U2 | 0x0000 | 0x7FFF | 0 | Hex |
| Protections | CUV | 0x9257 | Threshold | U1 | 20 | 90 | 50 | 50 mV |
| Protections | CUV | 0x9258 | Delay | U2 | 1 | 2047 | 74 | 3.3 ms |
| Protections | CUV | 0x925D | Recovery Hysteresis | U1 | 2 | 20 | 2 | 50 mV |
| Protections | COV | 0x925A | Threshold | U1 | 20 | 110 | 86 | 50 mV |
| Protections | COV | 0x925B | Delay | U2 | 1 | 2047 | 74 | 3.3 ms |
| Protections | COV | 0x925E | Recovery Hysteresis | U1 | 2 | 20 | 2 | 50 mV |
| Protections | COVL | 0x925F | Latch Limit | U1 | 0 | 255 | 0 | — |
| Protections | COVL | 0x9260 | Counter Dec Delay | U1 | 0 | 255 | 10 | s |
| Protections | COVL | 0x9261 | Recovery Time | U1 | 0 | 255 | 15 | s |
| Protections | OCC | 0x9262 | Threshold | U1 | 2 | 62 | 2 | 2 mV |
| Protections | OCC | 0x9263 | Delay | U1 | 1 | 127 | 4 | 3.3 ms |
| Protections | OCC | 0x926A | Recovery Threshold | I2 | –32768 | 32767 | –200 | mA |
| Protections | OCC | 0x9292 | PACK-TOS Delta | U1 | 10 | 255 | 10 | cV |
| Protections | OCD1 | 0x9264 | Threshold | U1 | 2 | 62 | 4 | 2 mV |
| Protections | OCD1 | 0x9265 | Delay | U1 | 1 | 127 | 1 | 3.3 ms |
| Protections | OCD2 | 0x9266 | Threshold | U1 | 2 | 62 | 3 | 2 mV |
| Protections | OCD2 | 0x9267 | Delay | U1 | 1 | 127 | 7 | 3.3 ms |
| Protections | SCD | 0x9268 | Threshold | U1 | 0 | 15 | 0 | — |
| Protections | SCD | 0x9269 | Delay | U1 | 1 | 31 | 2 | 15 µs |
| Protections | SCD | 0x9276 | Recovery Time | U1 | 0 | 255 | 5 | s |
| Protections | OCD3 | 0x926C | Threshold | I2 | –32768 | 0 | –4000 | userA |
| Protections | OCD3 | 0x926E | Delay | U1 | 0 | 255 | 2 | s |
| Protections | OCD | 0x926F | Recovery Threshold | I2 | –32768 | 32767 | 200 | mA |
| Protections | OCDL | 0x9271 | Latch Limit | U1 | 0 | 255 | 0 | — |
| Protections | OCDL | 0x9272 | Counter Dec Delay | U1 | 0 | 255 | 10 | s |
| Protections | OCDL | 0x9273 | Recovery Time | U1 | 0 | 255 | 15 | s |
| Protections | OCDL | 0x9274 | Recovery Threshold | I2 | –32768 | 32767 | 200 | mA |
| Protections | SCDL | 0x9277 | Latch Limit | U1 | 0 | 255 | 0 | — |
| Protections | SCDL | 0x9278 | Counter Dec Delay | U1 | 0 | 255 | 10 | s |
| Protections | SCDL | 0x9279 | Recovery Time | U1 | 0 | 255 | 15 | s |
| Protections | SCDL | 0x927A | Recovery Threshold | I2 | –32768 | 32767 | 200 | mA |
| Protections | OTC | 0x927C | Threshold | I1 | –40 | 120 | 55 | °C |
| Protections | OTC | 0x927D | Delay | U1 | 0 | 255 | 2 | s |
| Protections | OTC | 0x927E | Recovery | I1 | –40 | 120 | 50 | °C |
| Protections | OTD | 0x927F | Threshold | I1 | –40 | 120 | 60 | °C |
| Protections | OTD | 0x9280 | Delay | U1 | 0 | 255 | 2 | s |
| Protections | OTD | 0x9281 | Recovery | I1 | –40 | 120 | 55 | °C |
| Protections | OTF | 0x9282 | Threshold | U1 | 0 | 150 | 80 | °C |

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**Table 105. Data Memory Table (continued)**

| Class | Subclass | Address | Name | Type | Min Value | Max Value | Default | Units |
|---|---|---|---|---|---|---|---|---|
| Protections | OTF | 0x9283 | Delay | U1 | 0 | 255 | 2 | s |
| Protections | OTF | 0x9284 | Recovery | U1 | 0 | 150 | 65 | °C |
| Protections | OTINT | 0x9285 | Threshold | I1 | –40 | 120 | 85 | °C |
| Protections | OTINT | 0x9286 | Delay | U1 | 0 | 255 | 2 | s |
| Protections | OTINT | 0x9287 | Recovery | I1 | –40 | 120 | 80 | °C |
| Protections | UTC | 0x9288 | Threshold | I1 | –40 | 120 | 0 | °C |
| Protections | UTC | 0x9289 | Delay | U1 | 0 | 255 | 2 | s |
| Protections | UTC | 0x928A | Recovery | I1 | –40 | 120 | 5 | °C |
| Protections | UTD | 0x928B | Threshold | I1 | –40 | 120 | 0 | °C |
| Protections | UTD | 0x928C | Delay | U1 | 0 | 255 | 2 | s |
| Protections | UTD | 0x928D | Recovery | I1 | –40 | 120 | 5 | °C |
| Protections | UTINT | 0x928E | Threshold | I1 | –40 | 120 | –20 | °C |
| Protections | UTINT | 0x928F | Delay | U1 | 0 | 255 | 2 | s |
| Protections | UTINT | 0x9290 | Recovery | I1 | –40 | 120 | –15 | °C |
| Protections | Recovery | 0x9291 | Time | U1 | 0 | 255 | 3 | s |
| Protections | HWD | 0x9293 | Delay | U1 | 0 | 255 | 60 | s |
| Protections | Load Detect | 0x9294 | Active Time | U1 | 0 | 255 | 0 | s |
| Protections | Load Detect | 0x9295 | Retry Delay | U1 | 0 | 255 | 50 | s |
| Protections | Load Detect | 0x9296 | Timeout | U2 | 0 | 65535 | 1 | hrs |
| Protections | PTO | 0x9298 | Charge Threshold | I2 | –32768 | 32767 | 250 | mA |
| Protections | PTO | 0x929A | Delay | U2 | 0 | 65535 | 1800 | s |
| Protections | PTO | 0x929C | Reset | I2 | 0 | 10000 | 2 | userAh |
| Permanent Fail | CUDEP | 0x92A6 | Threshold | I2 | 0 | 32767 | 1500 | mV |
| Permanent Fail | CUDEP | 0x92A8 | Delay | U1 | 0 | 255 | 2 | s |
| Permanent Fail | SUV | 0x92A9 | Threshold | I2 | 0 | 32767 | 2200 | mV |
| Permanent Fail | SUV | 0x92AB | Delay | U1 | 0 | 255 | 5 | s |
| Permanent Fail | SOV | 0x92AC | Threshold | I2 | 0 | 32767 | 4500 | mV |
| Permanent Fail | SOV | 0x92AE | Delay | U1 | 0 | 255 | 5 | s |
| Permanent Fail | TOS | 0x92AF | Threshold | I2 | 0 | 32767 | 100 | mV |
| Permanent Fail | TOS | 0x92B1 | Delay | U1 | 0 | 255 | 5 | s |
| Permanent Fail | SOCC | 0x92B2 | Threshold | I2 | –32768 | 32767 | 10000 | userA |
| Permanent Fail | SOCC | 0x92B4 | Delay | U1 | 0 | 255 | 5 | s |
| Permanent Fail | SOCD | 0x92B5 | Threshold | I2 | –32768 | 32767 | –32000 | userA |
| Permanent Fail | SOCD | 0x92B7 | Delay | U1 | 0 | 255 | 5 | s |
| Permanent Fail | SOT | 0x92B8 | Threshold | I1 | –40 | 120 | 65 | °C |
| Permanent Fail | SOT | 0x92B9 | Delay | U1 | 0 | 255 | 5 | s |
| Permanent Fail | SOTF | 0x92BA | Threshold | U1 | 0 | 150 | 85 | °C |
| Permanent Fail | SOTF | 0x92BB | Delay | U1 | 0 | 255 | 5 | s |
| Permanent Fail | VIMR | 0x92BC | Check Voltage | I2 | 0 | 5500 | 3500 | mV |
| Permanent Fail | VIMR | 0x92BE | Max Relax Current | I2 | 10 | 32767 | 10 | mA |
| Permanent Fail | VIMR | 0x92C0 | Threshold | I2 | 0 | 5500 | 500 | mV |
| Permanent Fail | VIMR | 0x92C2 | Delay | U1 | 0 | 255 | 5 | s |
| Permanent Fail | VIMR | 0x92C3 | Relax Min Duration | U2 | 0 | 65535 | 100 | s |
| Permanent Fail | VIMA | 0x92C5 | Check Voltage | I2 | 0 | 5500 | 3700 | mV |
| Permanent Fail | VIMA | 0x92C7 | Min Active Current | I2 | 10 | 32767 | 50 | mA |
| Permanent Fail | VIMA | 0x92C9 | Threshold | I2 | 0 | 5500 | 200 | mV |
| Permanent Fail | VIMA | 0x92CB | Delay | U1 | 0 | 255 | 5 | s |
| Permanent Fail | CFETF | 0x92CC | OFF Threshold | I2 | 10 | 5000 | 20 | mA |
| Permanent Fail | CFETF | 0x92CE | OFF Delay | U1 | 0 | 255 | 5 | s |
| Permanent Fail | DFETF | 0x92CF | OFF Threshold | I2 | –5000 | –10 | –20 | mA |
| Permanent Fail | DFETF | 0x92D1 | OFF Delay | U1 | 0 | 255 | 5 | s |

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**Table 105. Data Memory Table (continued)**

| Class | Subclass | Address | Name | Type | Min Value | Max Value | Default | Units |
|---|---|---|---|---|---|---|---|---|
| Permanent Fail | VSSF | 0x92D2 | Fail Threshold | I2 | 1 | 32767 | 100 | — |
| Permanent Fail | VSSF | 0x92D4 | Delay | U1 | 0 | 255 | 5 | s |
| Permanent Fail | 2LVL | 0x92D5 | Delay | U1 | 0 | 255 | 5 | s |
| Permanent Fail | LFOF | 0x92D6 | Delay | U1 | 0 | 255 | 5 | s |
| Permanent Fail | HWMX | 0x92D7 | Delay | U1 | 0 | 255 | 5 | s |
| Security | Settings | 0x9238 | Security Settings | H1 | 0x00 | 0x07 | 0x00 | Hex |
| Security | Keys | 0x9239 | Unseal Key Step 1 | U2 | 0x0100 | 0xFFFF | 0x0414 | Hex |
| Security | Keys | 0x923B | Unseal Key Step 2 | U2 | 0x0100 | 0xFFFF | 0x3672 | Hex |
| Security | Keys | 0x923D | Full Access Key Step 1 | U2 | 0x0100 | 0xFFFF | 0xFFFF | Hex |
| Security | Keys | 0x923F | Full Access Key Step 2 | U2 | 0x0100 | 0xFFFF | 0xFFFF | Hex |

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The BQ76942 device can be used with 3-series to 10-series battery packs, supporting a top-of-stack voltage ranging from 5 V up to 55 V. To design and implement a comprehensive set of parameters for a specific battery pack, during development the user can utilize Battery Management Studio (BQSTUDIO), which is a graphical user-interface tool installed on a PC. Using BQSTUDIO, the device can be configured for specific application requirements during development once the system parameters, such as fault trigger thresholds for protection, enable or disable of certain features for operation, configuration of cells, and more are known. This results in a "golden image" of settings, which can then be programmed into the device registers or OTP memory.

## 8.2 Typical Applications

The following is the BQ76942 device application schematic for a 10-series configuration.

**NOTE**

The external NPN BJT used for the REGIN pre-regulator can be configured with its collector routed either to the cell battery stack or the middle of the protection FETs.

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## Typical Applications (continued)

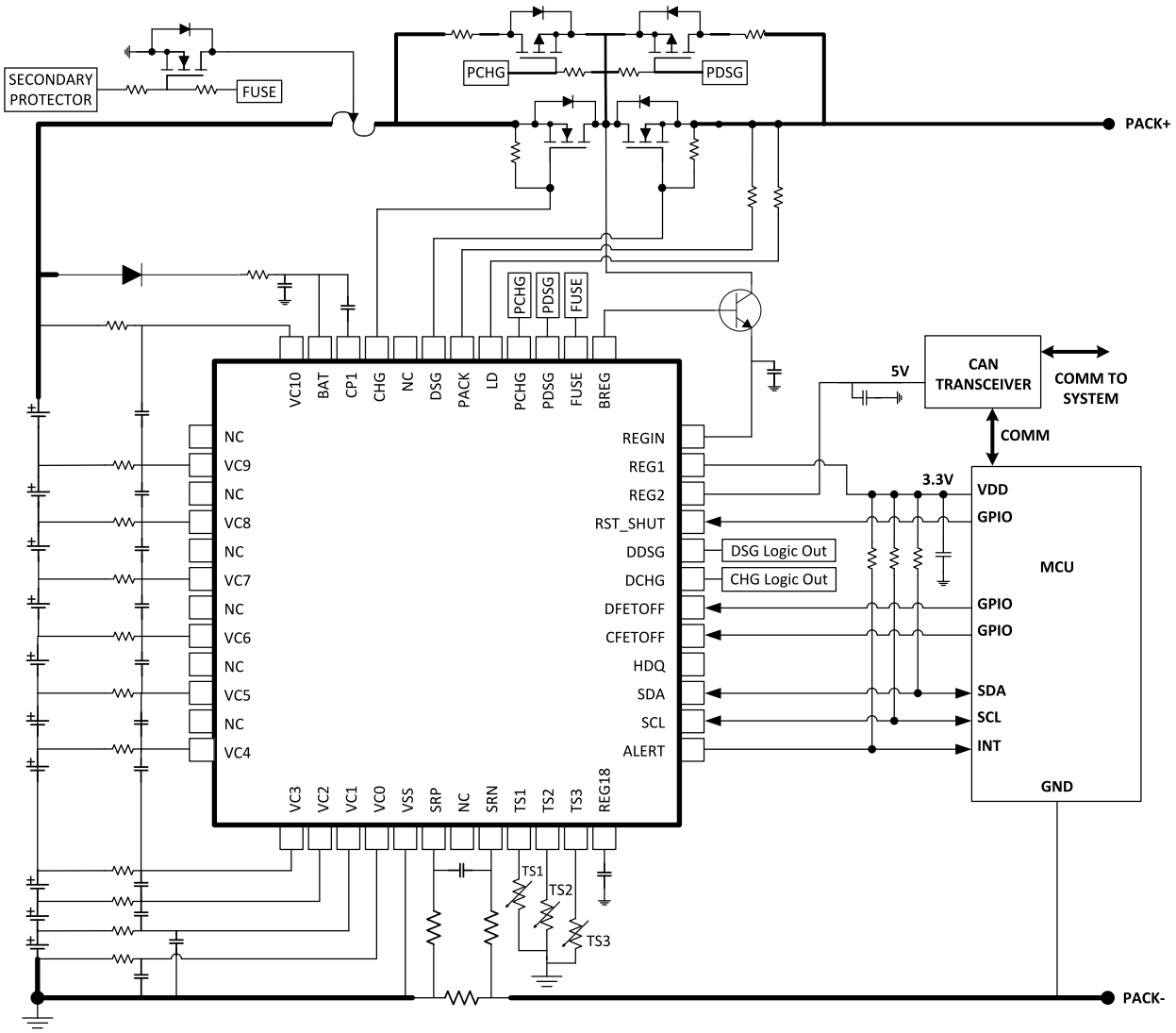


**Figure 20. BQ76942 10-Series Cell Typical Implementation (simplified schematic)**

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## Typical Applications (continued)

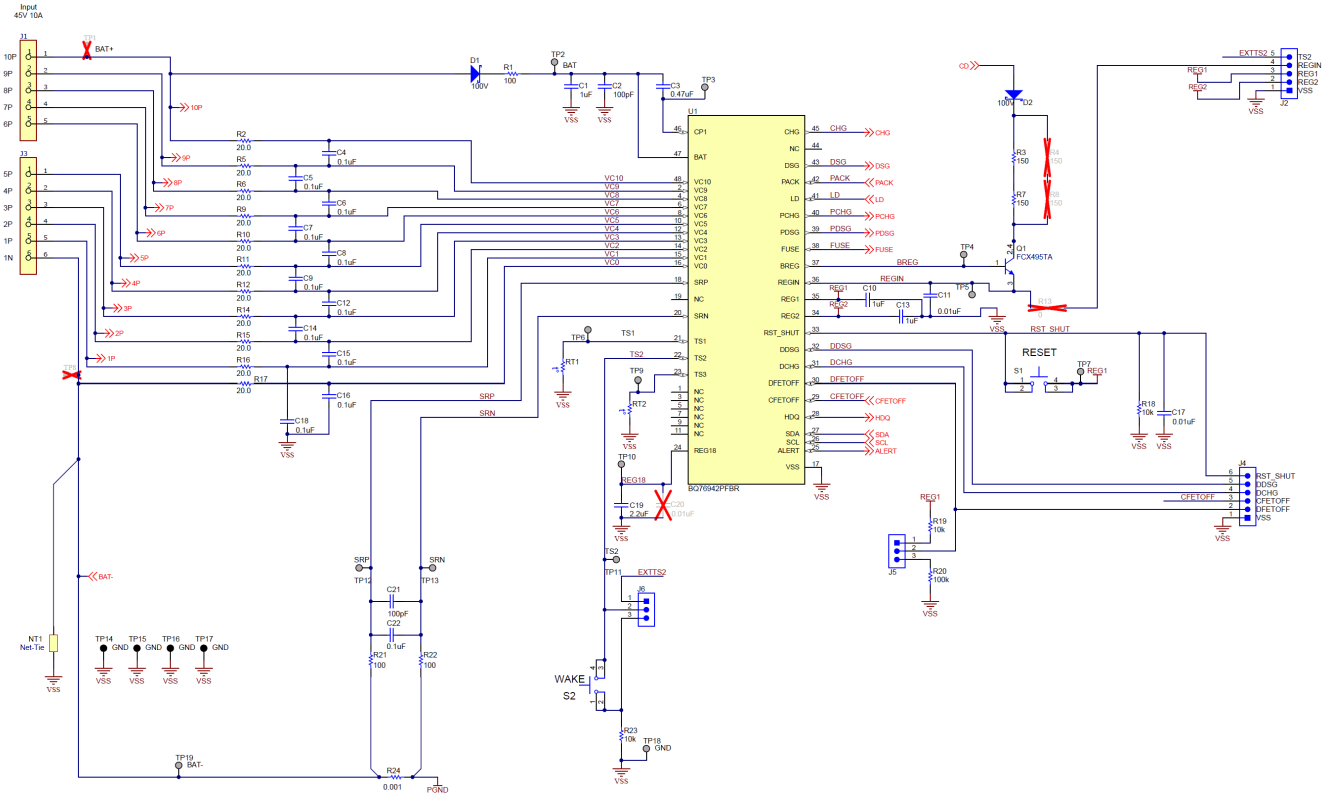


**Figure 21. BQ76942EVM Schematic Diagram - Monitor**

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## Typical Applications (continued)

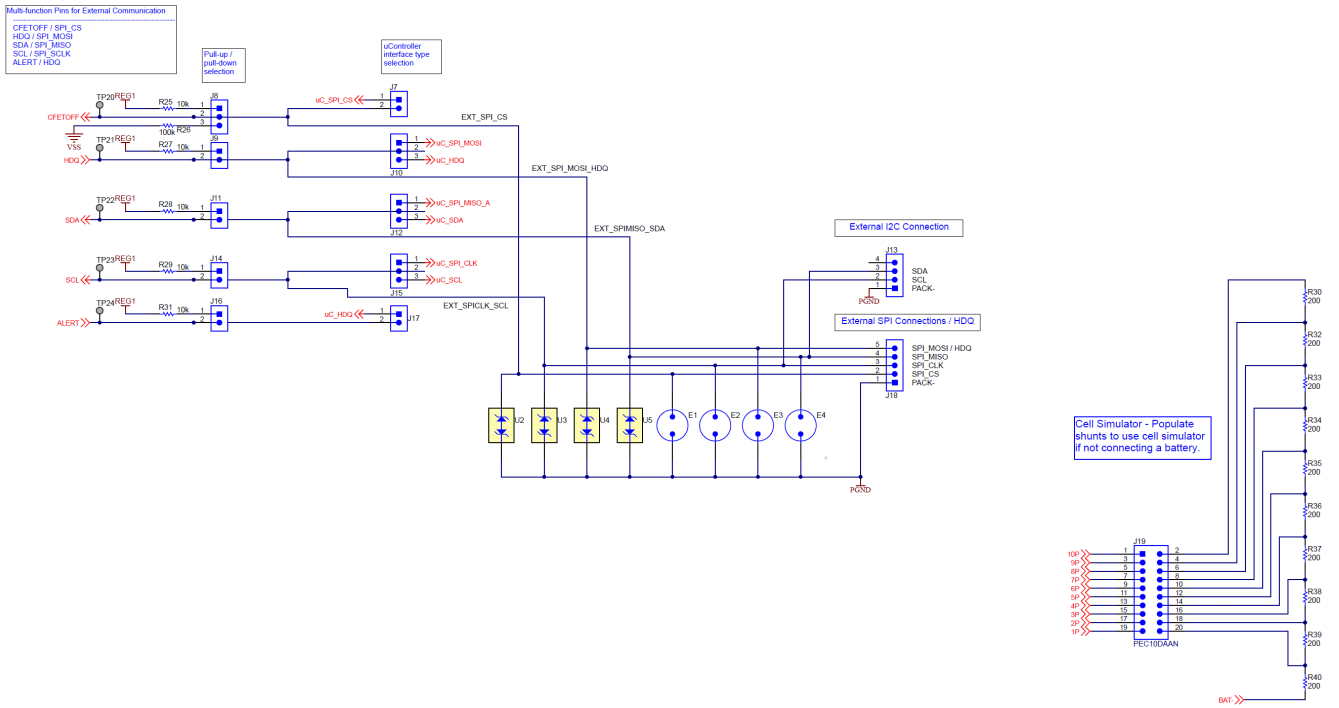


**Figure 22. BQ76942EVM Schematic Diagram - Pin Configuration**

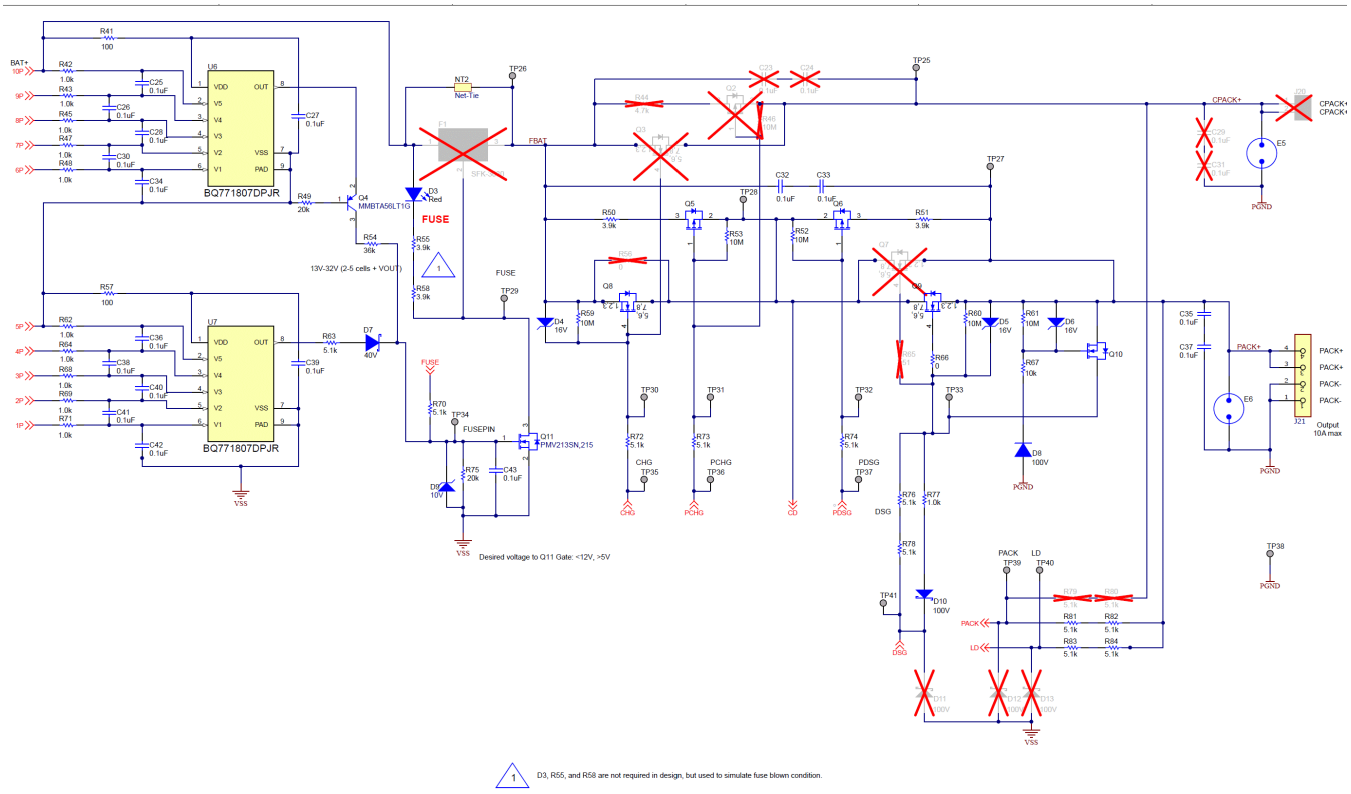


**Figure 23. BQ76942EVM Schematic Diagram - FETs**

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## Typical Applications (continued)

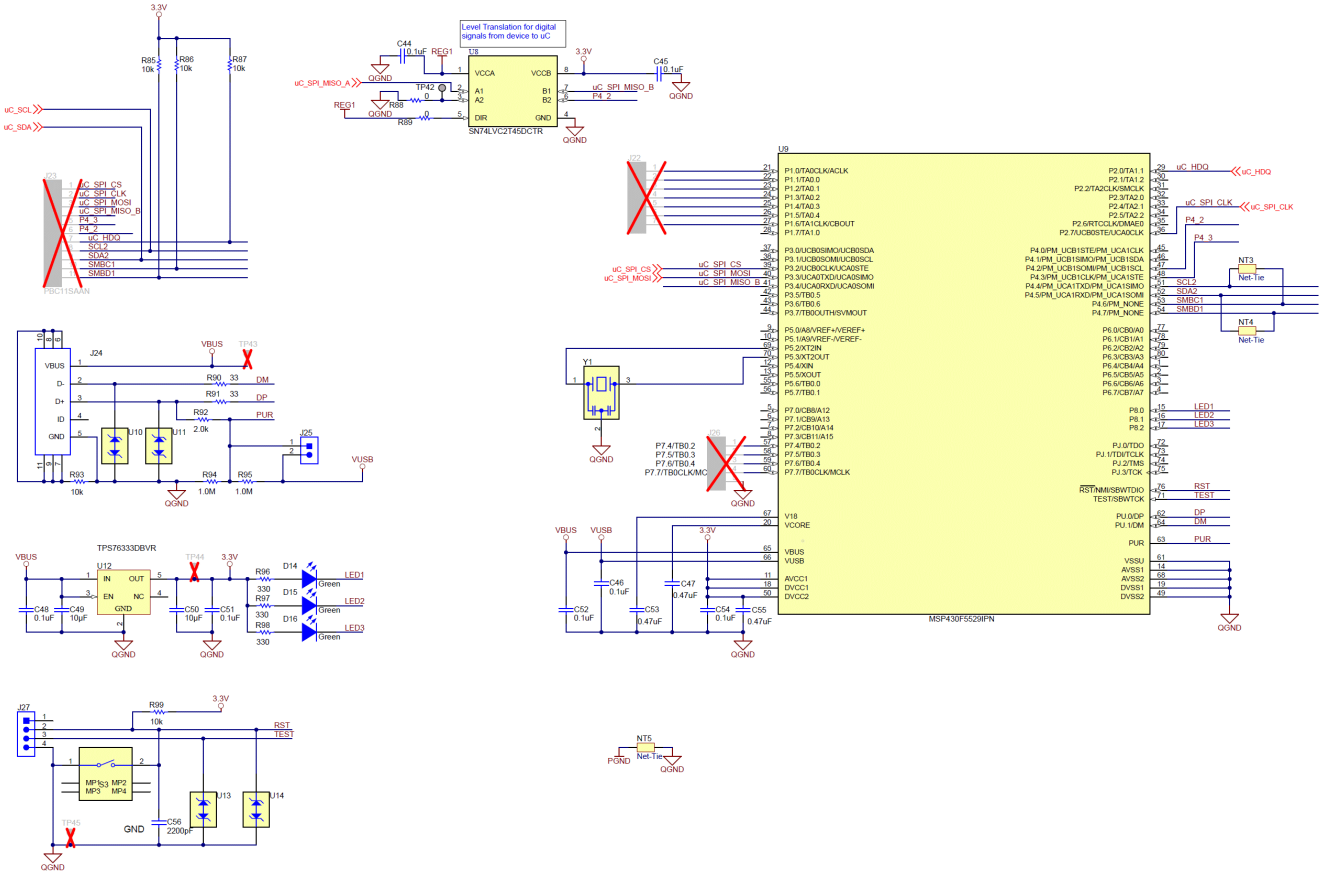


**Figure 24. BQ76942EVM Schematic Diagram - Interface Adapter**

### 8.2.1 Design Requirements (Example)

**Table 106. BQ76942 Design Requirements**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Minimum system operating voltage | 25 V |
| Cell minimum operating voltage | 2.5 V |
| Series cell count | 10 |
| Sense resistor | 1 mΩ |
| Number of thermistors | 3 (using TS1, TS2, and TS3 pins, all for cells) |
| Charge voltage | 42.5 V |
| Maximum charge current | 8.0 A |
| Peak discharge current | 20.0 A |
| Configuration settings | programmed in OTP during customer production |
| Protection subsystem configuration | Series FET configuration, device monitors, disables FETs upon fault, recovers autonomously |
| OV protection threshold | 4.30 V |
| OV protection delay | 500 ms |
| OV protection recovery hysteresis | 100 mV |
| UV protection threshold | 2.5 V |
| UV protection delay | 20 ms |
| UV protection recovery hysteresis | 100 mV |

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## Typical Applications (continued)

**Table 106. BQ76942 Design Requirements (continued)**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| SCD protection threshold | 80 mV (corresponding to a nominal 80 A, based on a 1-mΩ sense resistor) |
| SCD protection delay | 50 µs |
| OCD1 protection threshold | 68 mV (corresponding to a nominal 68 A, based on a 1-mΩ sense resistor) |
| OCD1 protection delay | 10 ms |
| OCD2 protection threshold | 56 mV (corresponding to a nominal 56 A, based on a 1-mΩ sense resistor) |
| OCD2 protection delay | 80 ms |
| OCD3 protection threshold | 28 mV (corresponding to a nominal 28 A, based on a 1-mΩ sense resistor) |
| OCD3 protection delay | 160 ms |
| OCC protection threshold | 8 mV (corresponding to a nominal 8 A, based on a 1-mΩ sense resistor) |
| OCC protection delay | 160 ms |
| OTD protection threshold | 60°C |
| OTD protection delay | 2 s |
| OTC protection threshold | 45°C |
| OTC protection delay | 2 s |
| UTD protection threshold | –20°C |
| UTD protection delay | 10 s |
| UTC protection threshold | 0°C |
| UTC protection delay | 5 s |
| Host watchdog timeout protection delay | 5 s |
| CFETOFF pin functionality | Use as CFETOFF, polarity = normally high, driven low to disable FET |
| DFETOFF pin functionality | Use as DFETOFF, polarity = normally high, driven low to disable FET |
| ALERT pin functionality | Use as ALERT interrupt pin, polarity = driven low when active, hi-Z otherwise |
| REG1 LDO Usage | Use for 3.3-V output |
| Cell balancing | Enabled when imbalance exceeds 100 mV |

### 8.2.2 Detailed Design Procedure

- Determine the number of series cells.
  - This value depends on the cell chemistry and the load requirements of the system. For example, to support a minimum battery voltage of 25 V using Li-CO2 type cells with a cell minimum voltage of 2.5 V, there needs to be at least 10-series cells.
  - For the correct cell connections, see Usage of VC Pins for Cells Versus Interconnect.
- Protection FET selection and configuration
  - The BQ76942 device is designed for use with high-side NFET protection
  - The configuration should be selected for series versus parallel FETs, which may lead to different FET selection for charge versus discharge direction.
  - These FETs should be rated for the maximum:
    - Voltage, which should be approximately 5 V (DC) to 10 V (peak) per series cell.
    - Current, which should be calculated based on both the maximum DC current and the maximum transient current with some margin.
    - Power Dissipation, which can be a factor of the RDS(ON) rating of the FET, the FET package, and the PCB design.
  - The overdrive level of the BQ76942 device charge pump should be selected based on RDS(ON) requirements for the protection FETs and their voltage handling requirements. If the FETs are selected with a maximum gate-to-source voltage of 15 V, then the 11 V overdrive mode within the BQ76942 device can be used. If the FETs are not specified to withstand this level, or there is a concern over gate leakage current on the FETs, the lower overdrive level of 5.5 V can be selected.
- Sense resistor selection.

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  - The resistance value should be selected to maximize the input range of the coulomb counter but not exceed the absolute maximum ratings, and avoid excessive heat generation within the resistor.
    - Using the normal maximum charge or discharge current, the sense resistor = 200 mV / 20.0 A = 10 mΩ maximum.
    - However, considering a short circuit discharge current of 80 A, the Abs Max SRP, SRN of ≈2.1 V, and the maximum SCD threshold of 500 mV, the sense resistor should be below 500 mV / 80 A= 6.25 mΩ maximum.
  - Further tolerance analysis (value tolerance, temperature variation, and so on) and PCB design margin should also be considered, so a sense resistor of 1 mΩ is suitable with a 75-ppm temperature coefficient and power rating of 1 W.
- The REG1 is selected to provide the supply for an external host processor, with output voltage selected for 3.3 V.
  - The NPN BJT used for the REG0 pre-regulator should be selected to support the maximum collector-to-emitter voltage of the maximum charging voltage of 68 V. The gain of the BJT should be chosen so it can provide the required maximum output current with a base current level that can be provided from the BQ76942 device.
  - The BJT should support the maximum current expected from the REG1 (maximum of 50 mA, with short circuit current limit of up to 80 mA).

### 8.2.3 Calibration Process

The BQ76942 device includes the ability for the user to calibrate the current, voltage, and temperature measurements on the customer production line. Detailed procedures are included in Voltage Calibration (ADC Measurements), Current Calibration, and Temperature Calibration . The device provides capability to calibrate individual cell voltage measurements, stack voltage, PACK pin voltage, LD pin voltage, current measurement, and individual temperature measurements.

## 8.3 Unused Pins

Some device pins may not be needed in a particular application. The manner in which each should be terminated in this case is describe below.

**Table 107. Terminating Unused Pins**

| Pin | Name | Recommendation |
|---|---|---|
| 2, 4, 6, 8, 10, 12 - 16, 48 | VC0 – VC10 | Cell inputs 1, 2, and 10 should always be connected to actual cells, with cells connected between VC1 and VC0, between VC2 and VC1, and VC10 and VC9. VC0 should be connected through a resistor and capacitor on the pcb to pin 17 (VSS). Pins related to any unused cells (which may be cell 3 - cell 9) can be connected to the cell stack to measure interconnect resistance or provide a Kelvin-connection to actual cells, in which case they should include a series resistor and parallel capacitor, in similar fashion to pins connected to actual cells (see Usage of VC Pins for Cells Versus Interconnect). Another option is to short unused VC pins directly to an adjacent VC pin. All VC pins should be connected to either an adjacent VC pin, an actual cell (through R and C) or stack interconnect resistance (through R and C). |
| 18, 20 | SRP, SRN | If not used, these pins should be connected to pin 17 (VSS). |
| 1, 3, 5, 7, 9, 11, 19, 44 | NC | These pins are not connected to silicon. They can be left floating or connected to an adjacent pin or connected to VSS. |
| 21, 23, 25, 28, 29, 30, 31, 32 | TS1, TS3, ALERT, HDQ, CFETOFF, DFETOFF, DCHG, DDSG | If not used, these pins can be left floating or connected to pin 17 (VSS). They may be configured with the weak pulldown resistance enabled during operation, although this is not necessary. |
| 22 | TS2 | If this pin is not used for thermistor or ADCIN measurement, the pin should be configured with the weak pulldown resistance enabled during operation. If the device is intended to enter SHUTDOWN mode, the TS2 pin should be left floating. If SHUTDOWN mode will not be used in the application, the TS2 pin can be left floating or connected to pin 17 (VSS). |
| 33 | RST_SHUT | If not used, this pin should be connected to pin 17 (VSS). |
| 34, 35 | REG1, REG2 | If not used, these pins can be left floating or connected to pin 17 (VSS). |
| 36 | REGIN | If not used, this pin should be connected to pin 17 (VSS) |
| 37 | BREG | If not used, this pin should be connected to pin 17 (VSS) |

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## Unused Pins (continued)

**Table 107. Terminating Unused Pins (continued)**

| Pin | Name | Recommendation |
|---|---|---|
| 38 | FUSE | If not used, this pin can be left floating or connected to pin 17 (VSS) |
| 39 | PDSG | If not used, this pin should be left floating. |
| 40 | PCHG | If not used, this pin should be left floating. |
| 43 | DSG | If not used, this pin should be left floating. |
| 45 | CHG | If not used, this pin should be left floating. |
| 46 | CP1 | If not used, this pin should be connected to pin 47 (BAT). Note: if the charge pump is enabled with CP1 connected to BAT, the device will consume an additional ≈200 µA. |

## 8.4 Device Event Timing

The timing of events in the BQ76942 device varies based on the specific event. Several events and their associated timing are described below. Timings described below do not include the delays related to individual protections, as described in their respective sections.

**Table 108. Timing of Events**

| Event Description | Timing |
|---|---|
| *Alarm Status()[SSA]* asserted, ALERT pin asserted due to *Alarm Status()[SSA]* | Fast response, in NORMAL or SLEEP modes |
| Data (including cell voltages and *CC2 Current()*) calculated after measurements complete (except for temperature calculations based on thermistor voltage measurements) | Fast response, in NORMAL or SLEEP modes |
| FET turn-off based on enabled protection fault, with ***Settings:Protection:CHG FET Protections A*** set to 0x98 or 0x18, and ***Settings:Protection:DSG FET Protections A*** set to 0x80 or 0xE4. | Fast response, in NORMAL or SLEEP modes |
| CHG FET turn-on, and DSG FET changing from source follower mode to charge pump mode, based on current wake detector triggered while in SLEEP mode. | Fast response, in SLEEP mode |
| FET turn-off based on enabled protection fault, with ***Settings:Protection:CHG FET Protections A*** not set to 0x98 or 0x18, and ***Settings:Protection:DSG FET Protections A*** not set to 0x80 or 0xE4. | Evaluated every 250 ms in NORMAL mode, or every 1 second in SLEEP mode |
| Evaluation if SHUTDOWN mode should be entered (due to RST_SHUT held high, temperature beyond ***Power:Shutdown:Shutdown Temperature***, or stack voltage below ***Power:Shutdown:Shutdown Stack Voltage***, | Evaluated every 250 ms in NORMAL mode, or every 1 second in SLEEP mode |
| *CC1 Current()* is calculated | Evaluated every 250 ms in NORMAL mode, or every 1 second in SLEEP mode |
| Minimum, maximum, and average voltages calculated | Evaluated every 250 ms in NORMAL mode, or every 1 second in SLEEP mode |
| Temperatures calculated based on measured thermistor voltages | Evaluated every 250 ms in NORMAL mode, or every 1 second in SLEEP mode |
| Precharge mode updated | Evaluated every 250 ms in NORMAL mode, or every 1 second in SLEEP mode |
| *Alarm Status()* other than *[SSA]* is updated, and ALERT pin asserted accordingly | Evaluated every 250 ms in NORMAL mode, or every 1 second in SLEEP mode |
| Evaluate whether OTP programming can proceed, in response to Permanent Failure status needing to be written, or *MANU_DATA()* write subcommand sent. | Evaluated every 250 ms in NORMAL mode, or every 1 second in SLEEP mode |
| Firmware safety checks (such as OCD3, temperature protections) and protection recovery checks | Evaluated every 1 second in NORMAL or SLEEP modes |
| Firmware Permanent Failure checks | Evaluated every 1 second in NORMAL or SLEEP modes |
| Evaluating entering or exiting SLEEP mode. This is separate from the FETs changing state when current is detected in SLEEP mode (fast response, as described above). This refers to the NORMAL mode measurement loop resuming. | Evaluated every 1 second in NORMAL or SLEEP modes |

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## Device Event Timing (continued)

**Table 108. Timing of Events (continued)**

| Event Description | Timing |
|---|---|
| Cell balancing checks | Evaluated every 1 second in NORMAL or SLEEP modes |
| RAM integrity check | Evaluated every 1 second in NORMAL or SLEEP modes |
| Internal watchdog timer | Generates reset if firmware does not respond every 2 seconds in NORMAL and SLEEP modes, and in DEEPSLEEP mode when the LFO is operating. |

# 9 Power Supply Requirements

The BQ76942 device draws its supply current from the BAT pin, which is typically connected to the top of stack point through a series diode, to protect against any fault within the device resulting in unintended charging of the pack. A series resistor and capacitor is included to lowpass filter fast variations on the stack voltage. During a short circuit event, the stack voltage may be momentarily pulled to a very low voltage before the protection FETs are disabled. In this case, the charge on the BAT pin capacitor will temporarily support the BQ76942 device supply current, to avoid the device losing power.

# 10 Layout

## 10.1 Layout Guidelines

- The quality of the Kelvin connections at the sense resistor is critical. The sense resistor must have a temperature coefficient no greater than 50 ppm in order to minimize current measurement drift with temperature. Choose the value of the sense resistor to correspond to the available overcurrent and short-circuit ranges of the BQ76942 device. Parallel resistors can be used as long as good Kelvin sensing is ensured. The device is designed to support a 1-mΩ sense resistor.
- In reference to the system circuitry, the following features require attention for component placement and layout: Differential Low-Pass Filter, and $I^2C$ communication.
- The BQ76942 device uses an integrating delta-sigma ADC for current measurements. For best performance, 100-Ω resistors should be included from the sense resistor terminals to the SRP and SRN inputs of the device, with a 0.1-µF filter capacitor placed across the SRP and SRN pins. Optional 0.1-µF filter capacitors can be added for additional noise filtering at each sense input pin to ground. All filter components should be placed as close as possible to the device, rather than close to the sense resistor, and the traces from the sense resistor routed in parallel to the filter circuit. A ground plane can also be included around the filter network to add additional noise immunity.
- The BQ76942 device internal REG18 LDO requires an external decoupling capacitor, which should be placed as close to the REG18 pin as possible, with minimized trace inductance, and connected to a ground plane electrically connected to VSS.
- The $I^2C$ clock and data pins have integrated ESD protection circuits; however, adding a Zener diode and series resistor on each pin provides more robust ESD performance. The $I^2C$ clock and data lines include a weak internal pull-down, so if the pack is removed from a system, the pins will discharge to VSS.

## 10.2 Layout Example

The BQ76942 EVM provides an example circuit implementation using the BQ76942 device. The EVM is a 4.0-inch × 5.0-inch 4-layer circuit card assembly and is designed for easy assembly, with cell connections at a terminal block on the left edge, and pack connections using a second terminal block on the top edge of the board. Wide trace areas are used, reducing voltage drops on the high current paths. Optional connections for hardware feature pins are on a separate terminal block on the top edge of the board. An on-board microcontroller is included for interfacing with a computer, with the accompanying USB connector located in the lower right corner. Configuration headers are included toward the right side of the board, and pushbutton switches for wake up and reset of the BQ76942 device are located near the bottom edge of the board.

The board layout includes spark gaps with the reference designator prefix *E*. These spark gaps are fabricated with the board and no component is installed.

Figure 25 to Figure 32 show the board layout.

## Layout Example (continued)

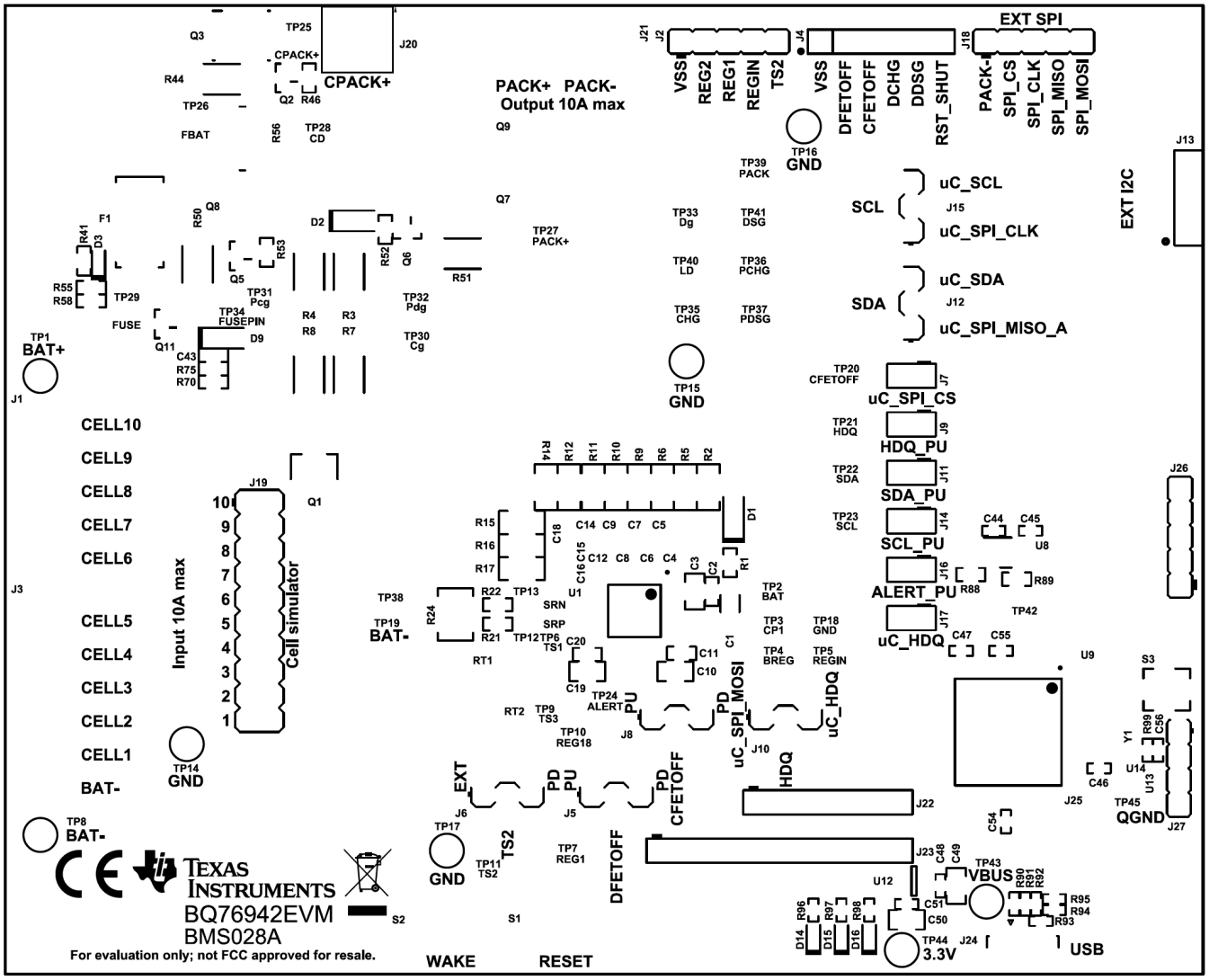


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**Figure 25. BQ76942 EVM Top Silk Screen**

## Layout Example (continued)

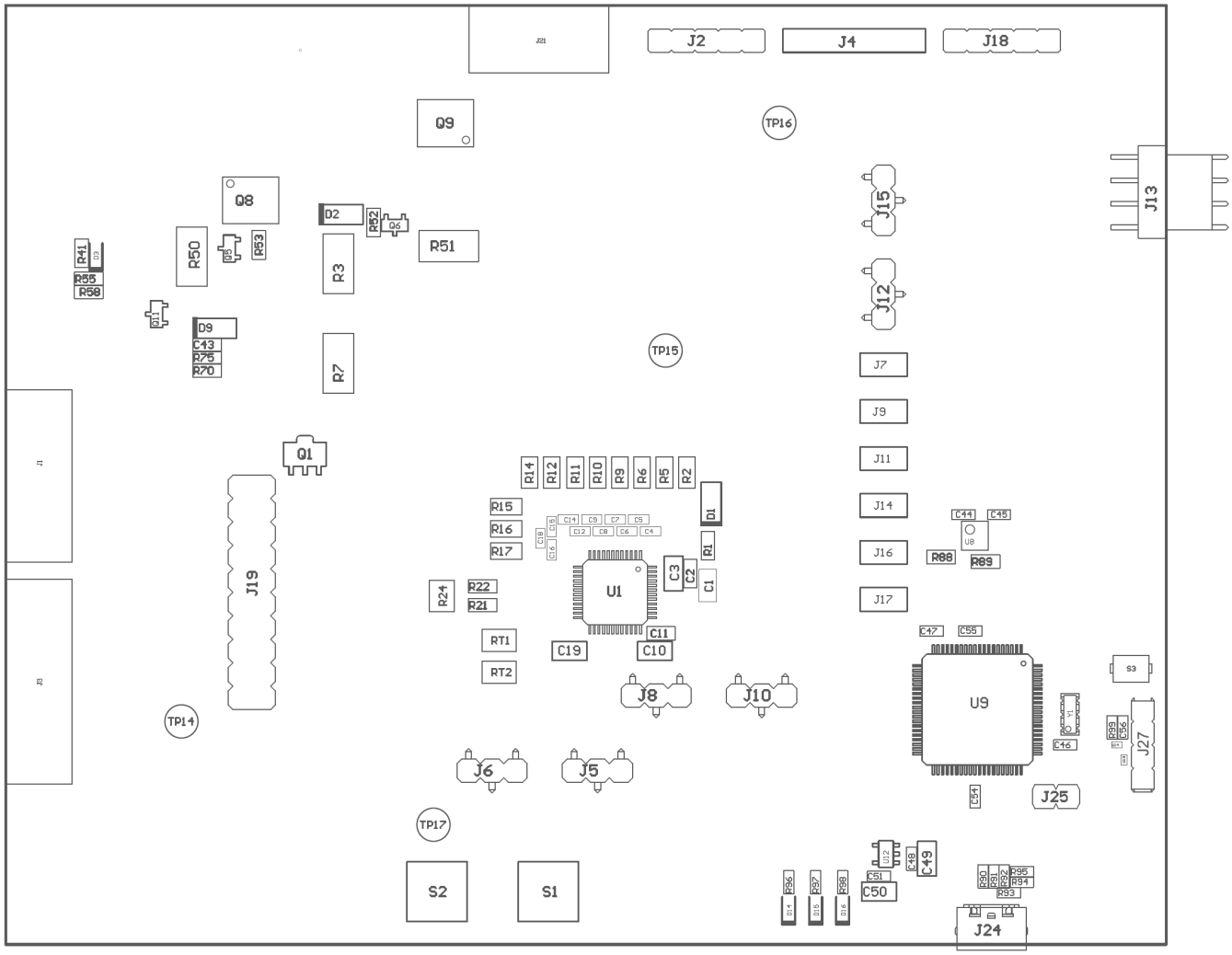


**Figure 26. BQ76942 EVM Top Assembly**

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## Layout Example (continued)

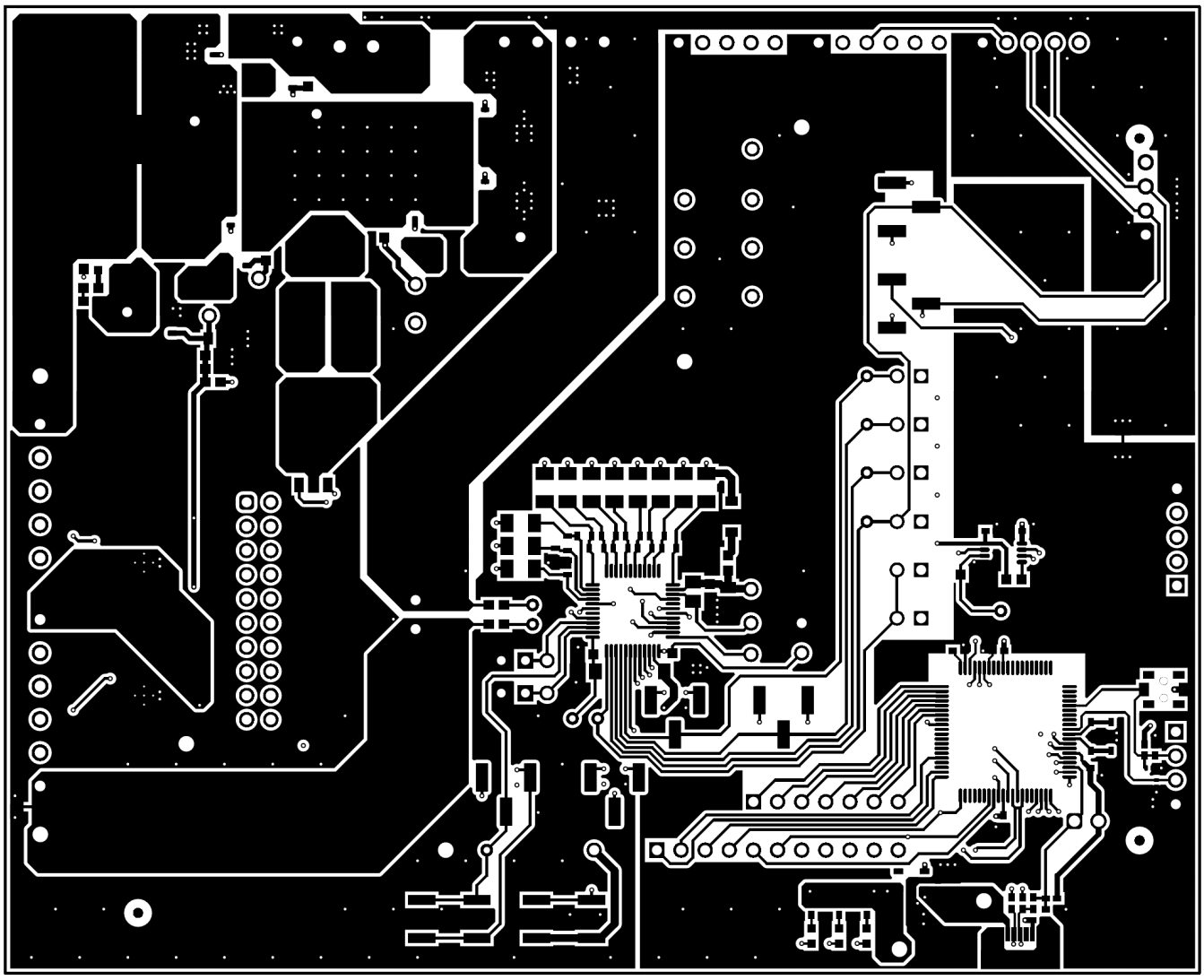

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**Figure 27. BQ76942 EVM Top Layer**

## Layout Example (continued)

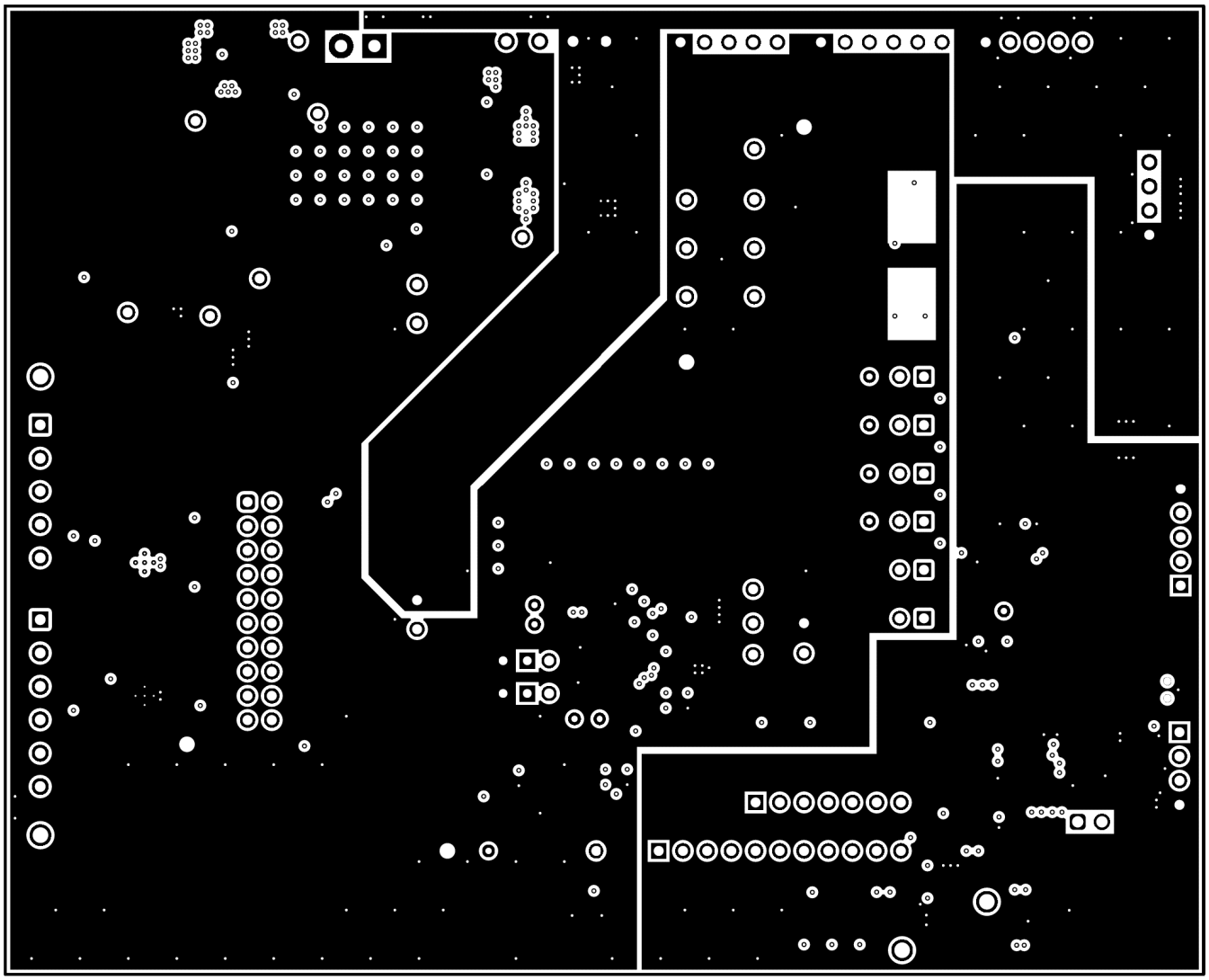

**Figure 28. BQ76942 EVM Layer 2**

## Layout Example (continued)

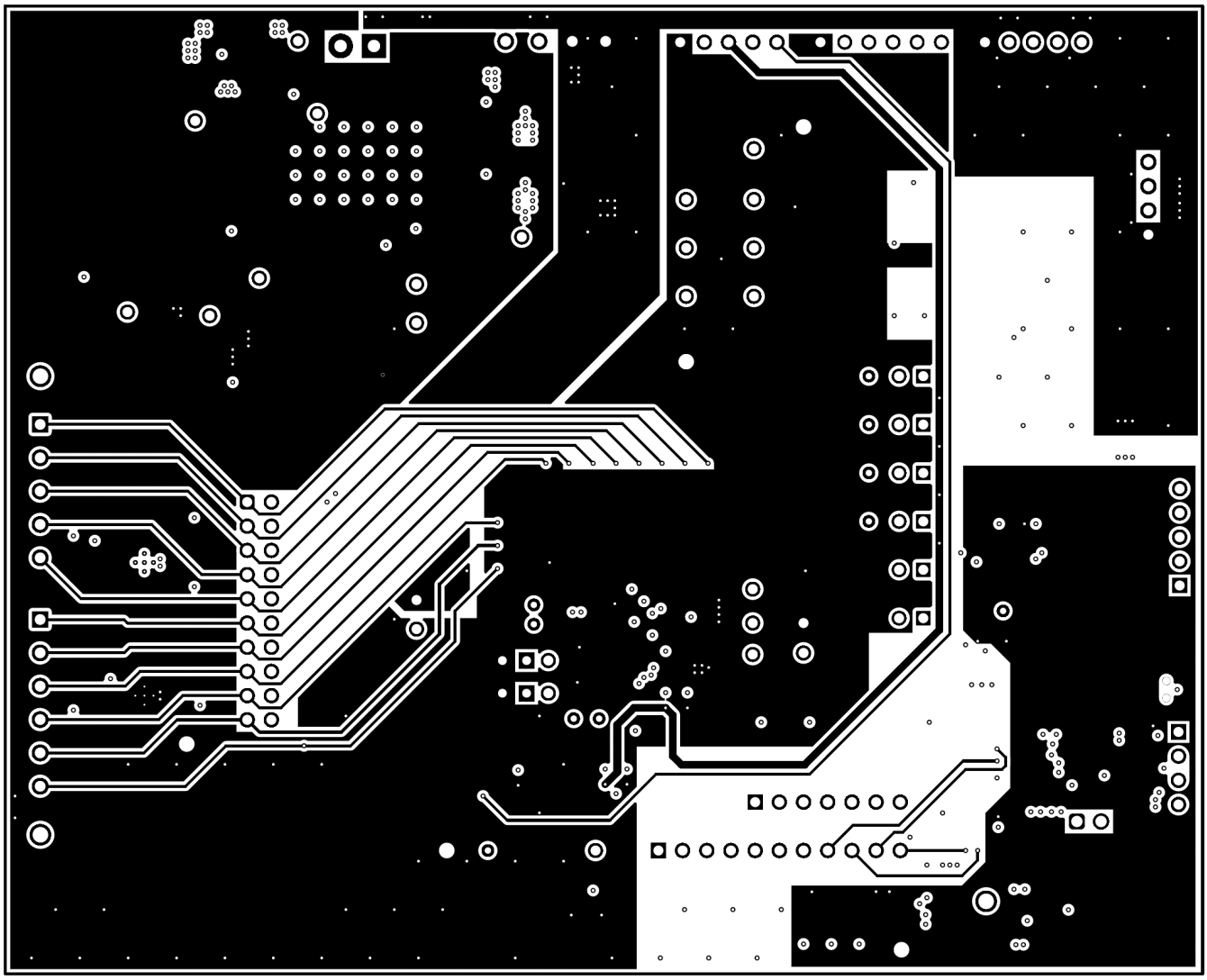

**Figure 29. BQ76942 EVM Layer 3**

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## Layout Example (continued)

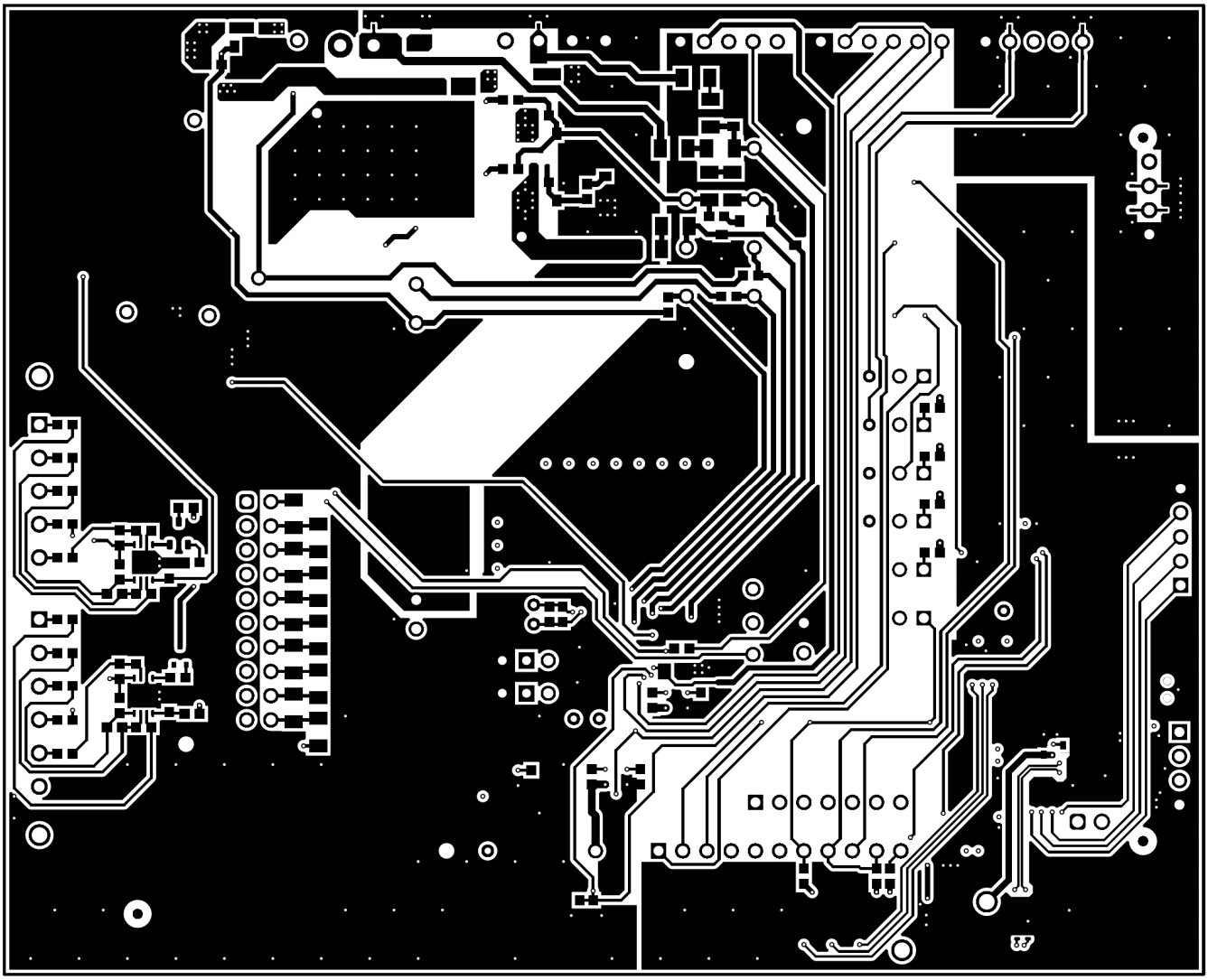

**Figure 30. BQ76942 EVM Bottom Layer**

## Layout Example (continued)

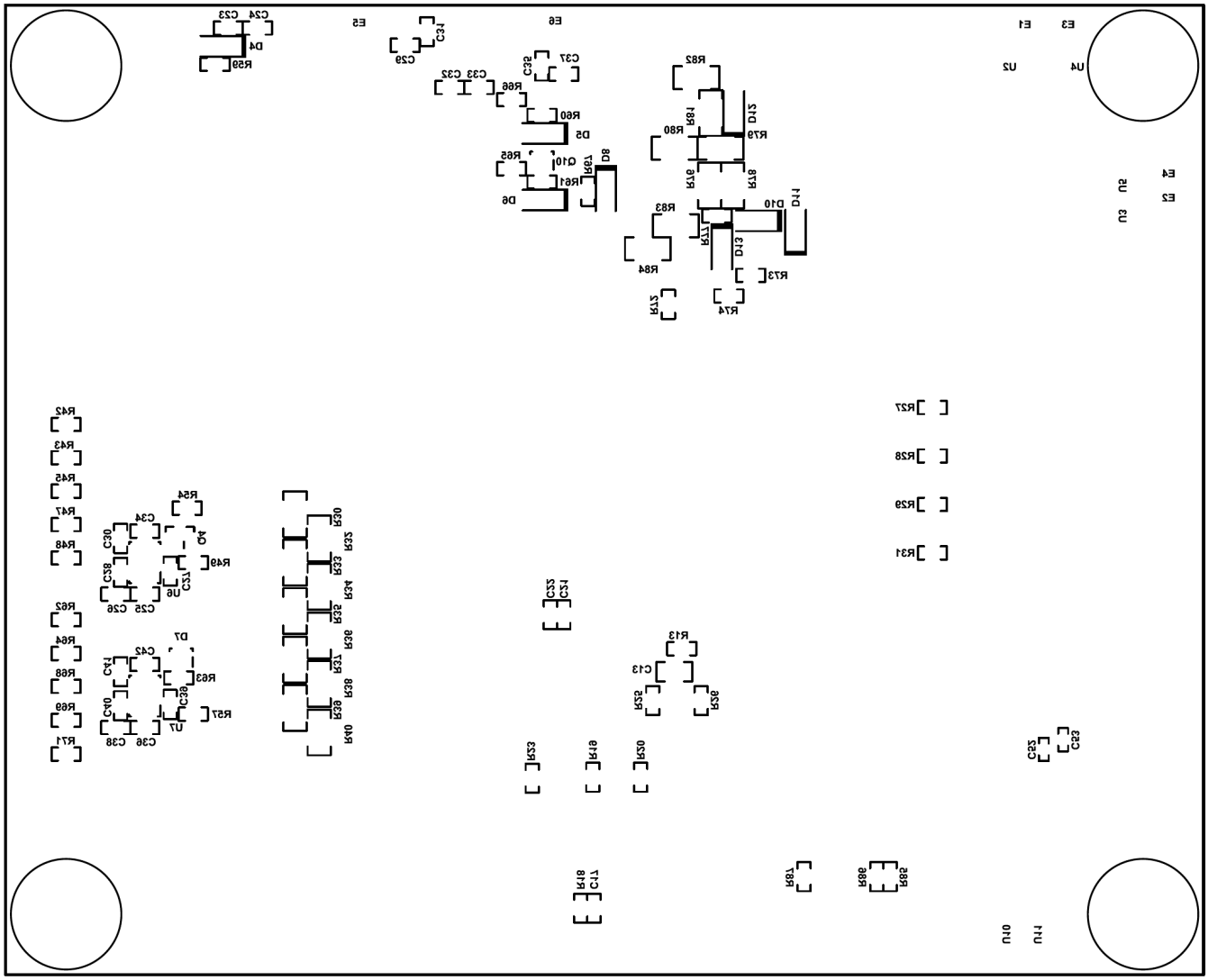

**Figure 31. BQ76942 EVM Bottom Silk Screen**

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## Layout Example (continued)

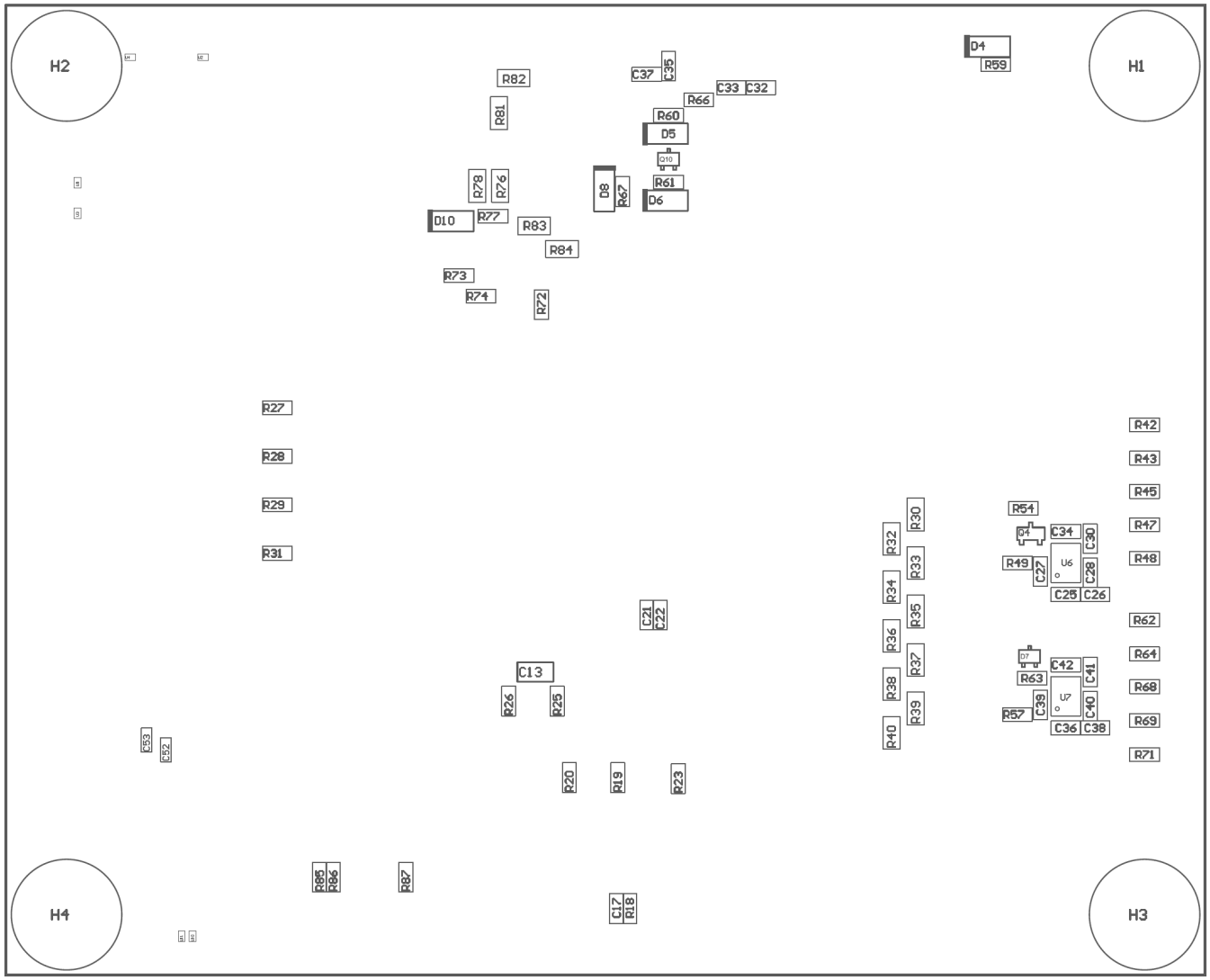


**Figure 32. BQ76942 EVM Bottom Assembly**

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# 11 Device and Documentation Support

## 11.1 Device Support

The early samples of BQ76942 include several issues, which are described below. A new revision of the silicon is planned before production release to address these issues.

### 11.1.1 Factory Trim Optimization

The factory trim of the device measurement system is not fully optimized in early samples, so voltage, current, and temperature measurements, and protection thresholds may be out of specification. This will be corrected before production release.

### 11.1.2 Circuit Operation Instability

The internal HFO oscillator powers up as needed for internal operations, as well as during serial communications. Each time the HFO powers up in the early samples of the device, there is a slight possibility to experience a transient error at the HFO turn-on which may cause unstable device operation, including causing the $I^2C$ bus to miss a clock and NACK a transaction if the bus speed is above 20 kHz.

This device instability can be avoided by keeping the HFO powered continuously during operation, preventing it from regularly cycling power. This is accomplished by setting the ***Settings:Configuration:Comm Idle Time*** value to 0xFF (255-sec). which causes the HFO to stay on for 255-s after any valid serial communications event. The host should then ensure there is a valid serial communications event occurring at least every 255-s, to prevent the HFO from powering down. The first transaction that occurs to initially power the HFO may still have a possibility to cause error (including an $I^2C$ NACK), but additional transactions should be successful as the HFO remains powered. The ***Comm Idle Time*** parameter has already been programmed in OTP to 255-s in early samples.

The ***Comm Idle Time*** workaround will cause a higher power dissipation (~30 µA) than normal due to the HFO running continuously. If a customer wants to measure the power the device would consume without the ***Comm Idle Time*** workaround, they can program ***Comm Idle Time*** = 0 and restrict the $I^2C$ bus speed to < 20 kHz, but they will still have risk of unstable device operation.

### 11.1.3 Unexpected Watchdog Resets

To work around an issue that can result in occasional unexpected watchdog resets, the ***Settings:Configuration:Comm Idle Time*** should be set to 255, and $I^2C$ communication should occur with the device at least once every 255 seconds. This workaround keeps the HFO running continuously, which has the side effect of dissipating ~30-µA additional current.

A watchdog reset is also possible upon exiting from CONFIG_UPDATE mode. This can be avoided by the host first sending the 0x009A *SLEEP_DISABLE()* subcommand, which causes the device to change to NORMAL mode, then wait at least one second before entering CONFIG_UPDATE mode. After exiting CONFIG_UPDATE mode, the device will read and use the updated data memory settings, so SLEEP mode will again be allowed based on the settings.

### 11.1.4 Cell Balancing Not Working Properly

The cell balancing component within the device has been disabled in early samples.

### 11.1.5 Thermistor Pin Stays Biased After Measurement

In early samples, an issue can cause a thermistor pin to stay biased after measurement is complete; thus, drawing additional system current. A workaround for this is to select TS1 for use as a thermistor, and TS2 for use as ADCIN (no pull-up), and no other pins selected for thermistor operation.

### 11.1.6 Occasional Watchdog Reset when Exiting CONFIG_UPDATE Mode

In early samples, the device will occasionally experience an internal processor watchdog fault (which causes a reset) upon exiting from CONFIG_UPDATE mode.

This issue only occurs when the device was in SLEEP Mode before entering CONFIG_UPDATE mode.

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### Device Support (continued)

The workaround for this issue is for the host to first send the *0x009A SLEEP_DISABLE()* subcommand, which causes the device to change to NORMAL mode, before entering CONFIG_UPDATE mode. After exiting CONFIG_UPDATE mode, the device will read and use the updated data memory settings, so SLEEP mode will again be allowed based on the settings.

## 11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 11.3 Trademarks

E2E is a trademark of Texas Instruments.

## 11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PBQ76942PFBT | ACTIVE | TQFP | PFB | 48 | 250 | TBD | Call TI | Call TI | -40 to 85 | | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

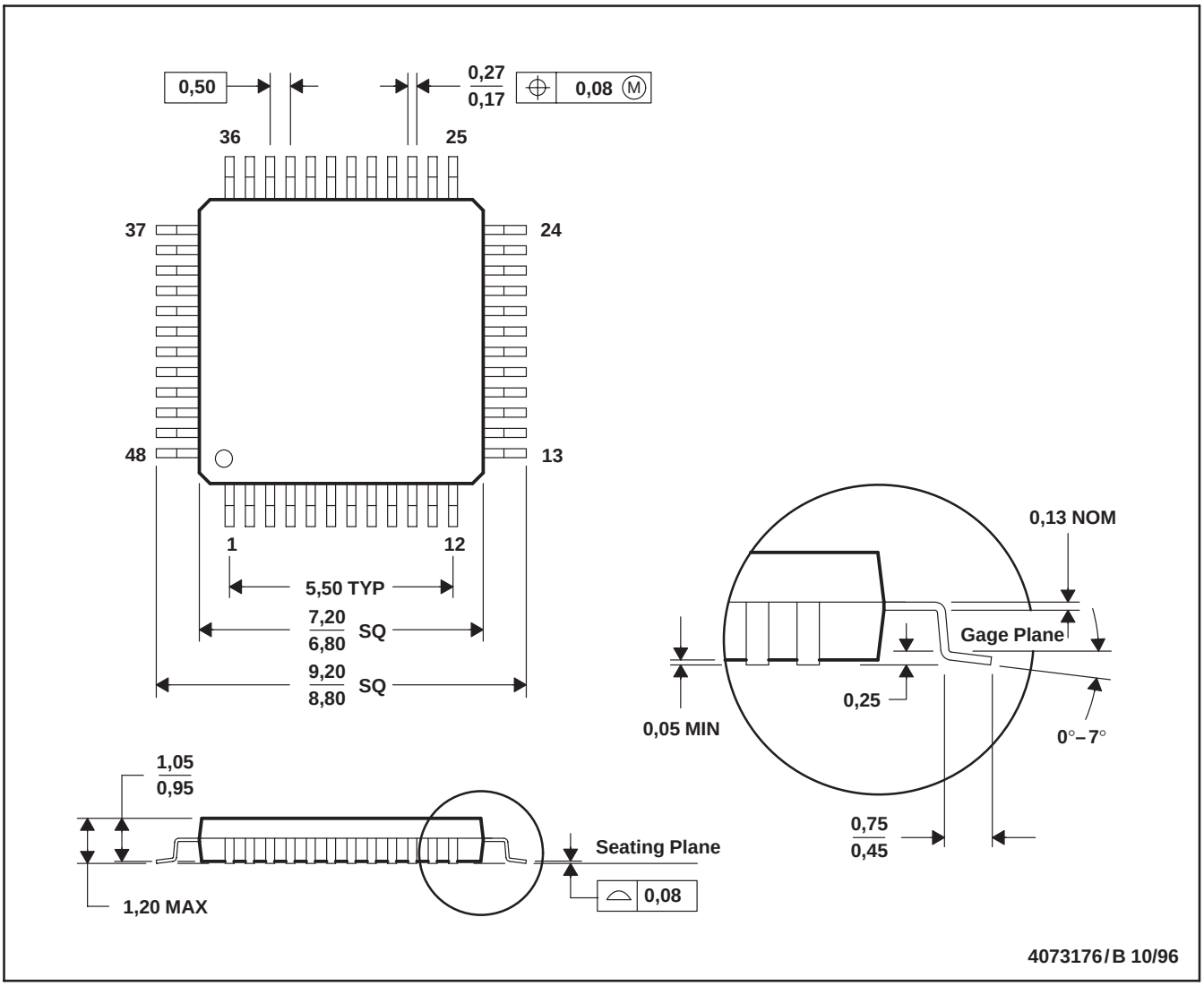
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

MTQF019A – JANUARY 1995 – REVISED JANUARY 1998

**PFB (S-PQFP-G48)** **PLASTIC QUAD FLATPACK**




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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