Dual Channel PWM Controller for IMVP9.1 CPU Core Power Supply

General Description

The RT3624BE is a synchronous buck controller which supports 2 output rails and can fully meet Intel IMVP9.1 requirements. The RT3624BE adopts G-NAVP™ (Green Native AVP) which is Richtek's proprietary topology derived from finite DC gain of EA amplifier with current mode control, making it easy to set the droop to meet all Intel CPU requirements of AVP (Adaptive Voltage Positioning). Based on the G-NAVP™ topology, the RT3624BE features a new generation of quick response mechanism (Adaptive Quick Response, AQR) to optimize AVP performance during load transient and reduce output capacitors. The RT3624BE integrates a high accuracy ADC for platform and function settings, such as ICCMAX, switching frequency, over-current threshold or AQR trigger level. The RT3624BE provides VR Ready and thermal indicators. It also features complete fault protection functions including over-voltage (OV), under-voltage (UV), over-current (OC) and under-voltage lockout (UVLO).

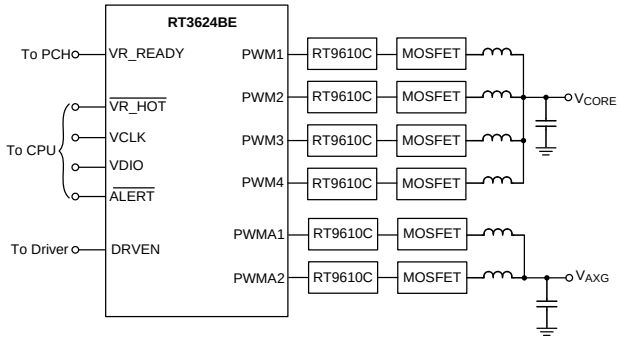
Applications

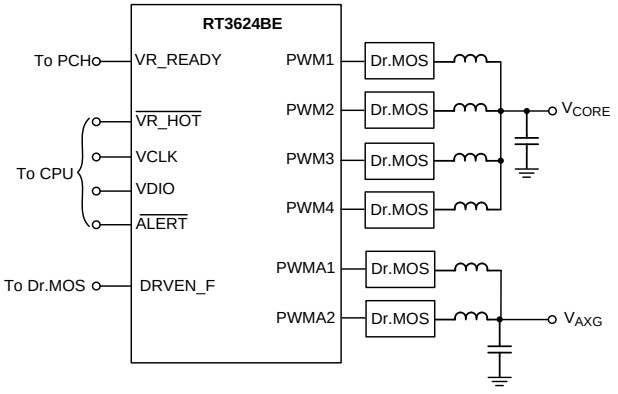
- IMVP9.1 Intel CORE/AXG Supply
- Desktop and Notebook Computer
- AVP Step-Down Converter

Features

- **Intel IMVP9.1 Compliant**
- **4/3/2/1 Phase (CORE VR) + 2/1 Phase (AXG VR) PWM Controller**
- **G-NAVP™ (Green Native Adaptive Voltage Positioning) Topology**
- **0.5% DAC Accuracy**
- **Differential Remote Voltage Sensing**
- **Built-in ADC for Platform Programming and Reporting**
- **Accurate Current Balance**
- **Diode Emulation Mode at Light Load Condition**
- **Fast Transient Response-Adaptive Quick Response (AQR)**
- **VR Ready Indicator**
- **OVP,OCP, UVP with Flag**
- **Switching Frequency Range Setting**
- **DVID Enhancement**
- **Acoustic Noise Suppression**
- **Zero Load-line**
- **Rail Disable**
- **Support Phase Doubler RT9637 for CORE rail Up to 6-Phase Operation (optional)**
- **Support SPS Application (optional)**
- **Soldering Good Detection**
- **RT3624BE : Support Address 00 and 01**
- **Small 52-Lead WQFN Package**

Simplified Application Circuit





Ordering Information

RT3624BE□□

Package Type
QW : WQFN-52L 6x6 (W-Type)

Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

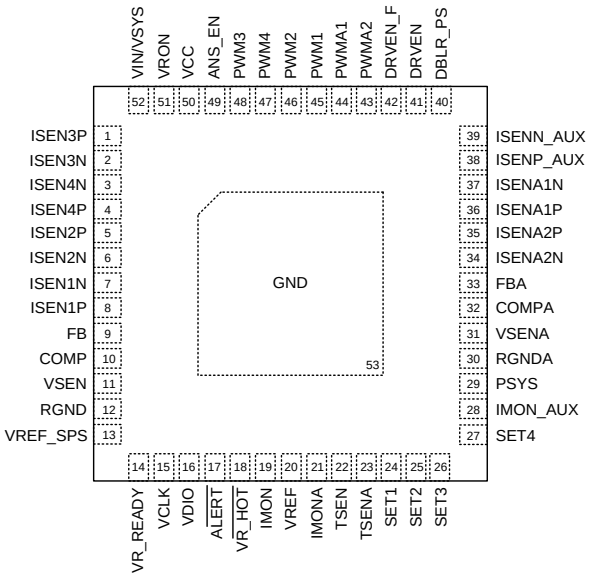
- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes..

Marking Information

RT3624BEGQW : Product Number
YMDNN : Date Code

Pin Configuration

(TOP VIEW)



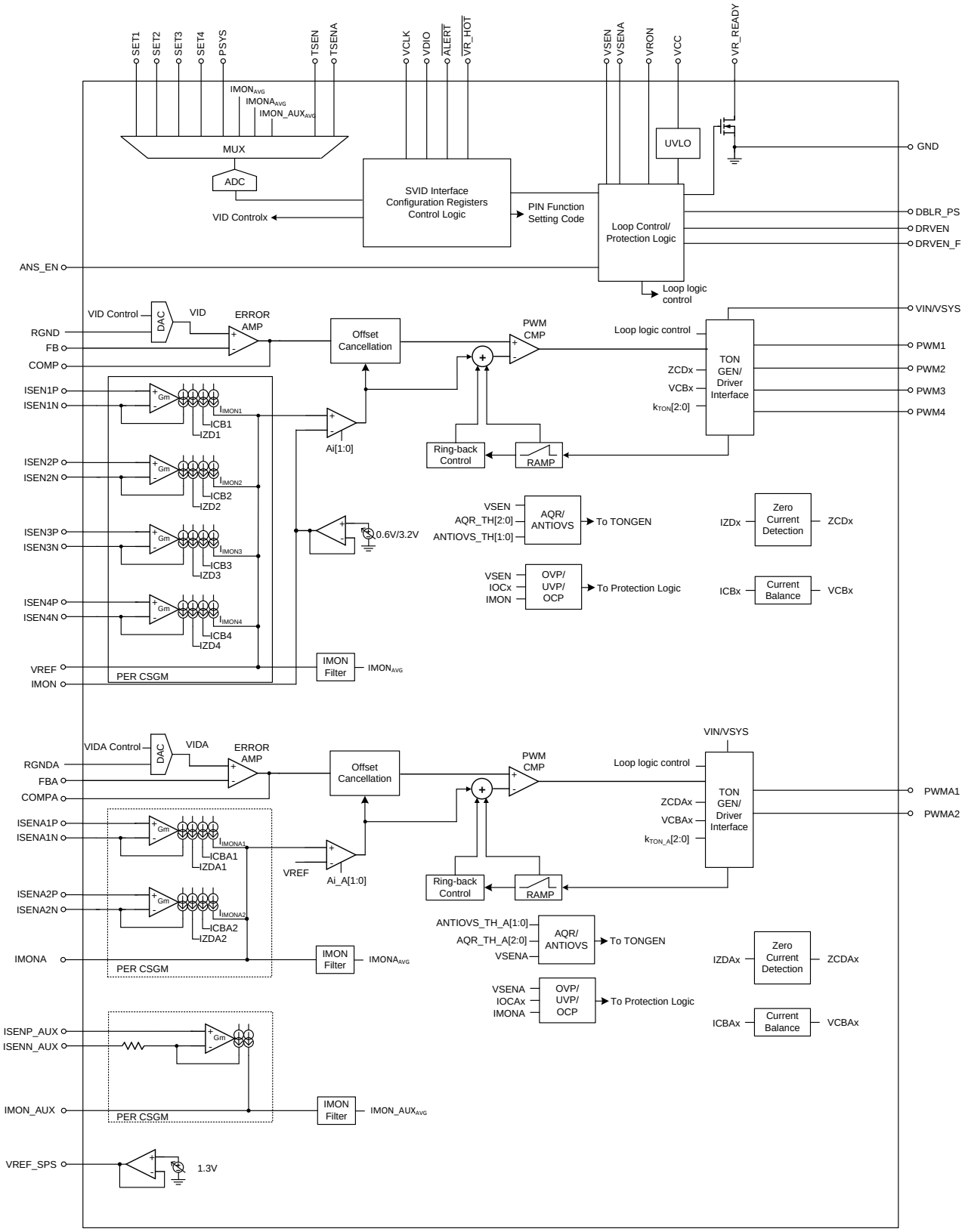
WQFN-52L 6x6

Functional Pin Description

Pin No.	Pin Name	Pin Function
8, 5, 1, 4	ISEN[1:4]P	Positive inputs to current-sense amplifier for Phase 1 to 4 of VR CORE rail.
7, 6, 2, 3	ISEN[1:4]N	Negative inputs to current-sense amplifier for Phase 1 to 4 of VR CORE rail.
9	FB	Negative input of the error amplifier. This pin is for CORE rail VR output voltage feedback to controller.
10	COMP	CORE rail VR compensation. This pin is an error amplifier output pin.
11	VSEN	CORE rail VR voltage sense input. This pin is connected to the terminal of CORE rail VR output voltage.
12	RGND	Return ground for CORE rail VR. This pin is the negative node of the differential remote voltage sensing.
13	VREF_SPS	Fixed 1.3V output reference voltage. This voltage is used to offset the smart power stage. Between this pin and GND must be placed an exact 0.22μF decoupling capacitor.
14	VR_READY	VR ready indicator.
15	VCLK	Synchronous clock from the CPU.
16	VDIO	VR and CPU data transmission interface.
17	$\overline{\text{ALERT}}$	SVID alert. (Active low)
18	$\overline{\text{VR\_HOT}}$	Thermal monitor output. (Active low)
19	IMON	CORE rail VR current monitor output. This pin outputs a voltage proportional to the output current.
20	VREF	Fixed 0.6V output reference voltage. This voltage is used to offset the output voltage of all IMON pins. While controller shut down or set all rail in PS4, voltage source shuts down. An exact 0.47μF decoupling capacitor and a 3.9Ω resistor must be place between this pin and GND.
21	IMONA	AXG rail VR current monitor output. This pin outputs a voltage proportional to the output current.
22	TSEN	Thermal sense input for CORE rail VR and function for current gain (Ai) and adaptive quick response trigger level for CORE rail VR
23	TSENA	Thermal sense input for AXG rail VR and function for current gain (Ai) and adaptive quick response trigger level for AXG rail VR.
24	SET1	Function setting for ICCMAX and VBOOT of CORE rail and ICCMAX of AXG rail. Connect the SET1 pin and SET3 pin to 5V and pull the VRON high. If the soldering is good, both rail outputs are non-zero VBOOT.
25	SET2	Function setting for VBOOT of AXG rail and on-time width setting (switching frequency) of CORE rail, selectable VID table, zero load line and ICCMAX of AUX rail.
26	SET3	Function setting for undershoot suppression, DVID fast slew rate, DVID voltage compensation and $\overline{\text{VR\_HOT}}$ assertion during DVID current limit.
27	SET4	Function setting for phase number with RT9637 of CORE rail, on-time width setting (switching frequency) of AXG rail and anti-overshoot trigger level.
28	IMON_AUX	AUX rail VR current monitor output. This pin outputs a voltage proportional to the output current.

Pin No.	Pin Name	Pin Function
29	PSYS	System input power monitor. Place the PSYS resistor as close to the IC as possible. The input power domain (SVID Address 0x0Dh) rail can be disabled by pulling the voltage at the PSYS pin > (VCC – 0.5V). RT3624BE will reject any commands to the input power domain rail. If the platform doesn't support PSYS function, It is recommended to connect PSYS pin to GND to avoid affecting system performance.
30	RGNDA	Return ground for AXG rail VR. This pin is the negative node of the differential remote voltage sensing.
31	VSENA	AXG rail VR voltage sense input. This pin is connected to the terminal of AXG rail VR output voltage.
32	COMPA	AXG rail VR compensation. This pin is an error amplifier output pin.
33	FBA	Negative input of the error amplifier. This pin is for AXG rail VR output voltage feedback to controller.
37, 34	ISENA[1:2]N	Negative inputs to current-sense amplifier for Phase 1 to 2 of VR AXG rail.
36, 35	ISENA[1:2]P	Positive inputs to current-sense amplifier for Phase 1 to 2 of VR AXG rail.
38	ISENP_AUX	Positive input to current-sense amplifier of VR AUX rail.
39	ISENN_AUX	Negative input to current-sense amplifier of VR AUX rail.
40	DBLR_PS	External driver mode control. As received PS4 command, this pin will be high state. This pin can work with RT9637 on 1 PWM drive 2 power stage. As PS0 command is received, this pin will be low state. As PS1 command is received, this pin will be floating state. As PS2/3 command is received, this pin will be high state.
41	DRVEN	External driver mode control. As PS4 command is received, this pin will be low state. The output high level is VCC.
42	DRVEN_F	External driver mode control. As PS4 command is received, this pin will be floating state. The output high level is VCC.
44, 43	PWMA[1:2]	PWM outputs for AXG rail VR. The tri-state window = 1.6V to 2.2V.
45, 46, 48, 47	PWM[1:4]	PWM outputs for CORE rail VR. The tri-state window = 1.6V to 2.2V.
49	ANS_EN	Acoustic Noise Suppression function setting. When the pin is pulled to VCC, this function can be enabled. This pin is not allowed to be floating.
50	VCC	Controller power supply. Connect this pin to 5V and place a RC filter, R = 2.2Ω and C = 4.7μF. The decoupling capacitor should be placed as close to PWM controller as possible. The recommended size of R_{VCC} is 0603.
51	VRON	VR enable control input.
52	VIN/VSYS	VIN/VSYS input pin. Connect a low pass filter to this pin to set on-time.
53 (Exposed Pad)	GND	Ground. The Exposed Pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Functional Block Diagram



Operation

G-NAVP™ Control Mode

The RT3624BE adopts G-NAVP™ (Green Native AVP) which is Richtek's proprietary topology. It is derived from current mode constant on-time control with finite DC gain of error amplifier and DC offset cancellation. The topology can achieve easy load-line design and provide high DC accuracy and fast transient response. When sensed current signal reaches sensed voltage signal, the RT3624BE generates a PWM pulse to achieve loop modulation. Figure 1 shows the basic G-NAVP™ behavior waveforms. The COMP signal is the sensed voltage that is inverted and amplified signal of output voltage. While current loading is increasing, referring to Figure 1, COMP basic G-NAVP™ behavior waveforms. The COMP rises due to output voltage droop. Then rising COMP forces PWM turn on earlier and closely. While inductor current reaches loading current, COMP enters another steady state of higher voltage and the corresponding output voltage is in the steady state of lower voltage. The load-line, output voltage drooping by an amount which is proportional to loading current, is achieved.

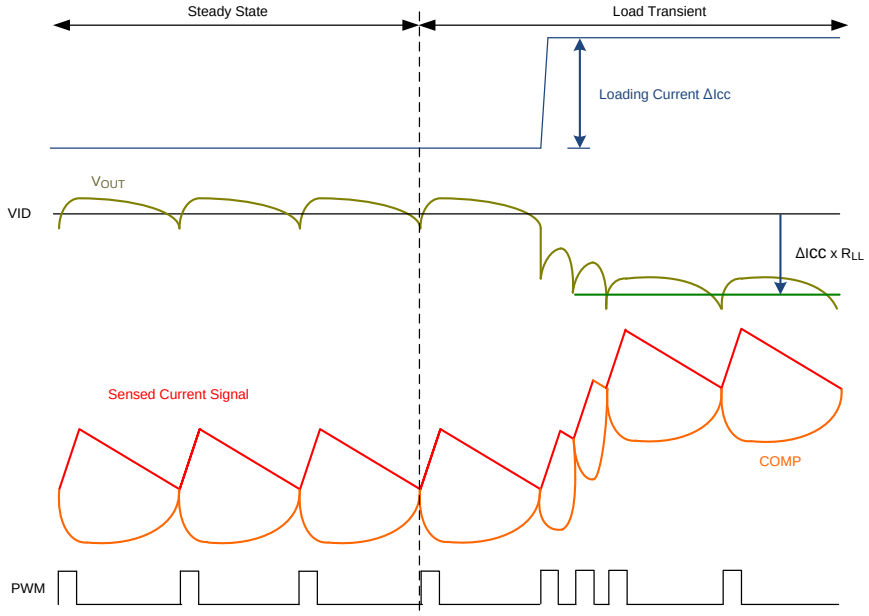


Figure 1. G-NAVP™ Behavior Waveform

SVID Interface/Control Logic/Configuration Registers

SVID Interface receives or transmits SVID signal with CPU. Control Logic executes command (Read/Write registers, setVID, setPS) and sends related signals to control VR. Configuration Registers include function setting registers and CPU required registers.

IMON Filter

IMON Filter is used to average current signal by an analog low-pass filter. It outputs $IMON_{AVG}$ to the MUX of ADC for current reporting.

MUX and ADC

The MUX supports the inputs of SET1, SET2, SET3, SET4, TSEN, TSENA, PSYS, $IMON_{AVG}$, $IMONA_{AVG}$ and $IMON\_AUX_{AVG}$. The ADC converts these analog signals to digital codes for reporting or function settings.

UVLO

The UVLO detects the VCC voltage. As VCC exceeds threshold, controller issues POR = high and waits VRON. After both POR and VRON are ready, then controller is enabled.

Loop Control/Protection Logic

It controls power-on/off sequence, protections, power state transition, and PWM sequence.

DAC

The DAC generates a reference VID voltage according to the VID code sent by Control Logic. According to setVID command, Control Logic dynamically changes VID voltage to target with required slew rate.

ERROR AMP

The ERROR AMP inverts and amplifies the difference between output voltage and VID with externally setting finite DC gain. The output signal is COMP for PWM trigger.

PER CSGM

The PER CSGM senses per-phase inductor current. The outputs are used for loop response, Current Balance, Zero Current Detection, current reporting and over-current protection.

SUM CSGM

The SUM CSGM senses total inductor current with RIMON gain adjustment. SUM CSGM output current ratio can also be set by PIN-SETTING(Ai[1:0]). It helps wider application range of DCR and load line. SUM CSGM output is used for PWM trigger.

RAMP

The RAMP helps loop stability and transient response.

PWM CMP

The PWM comparator compares COMP signal and sum current signal based on RAMP to trigger PWM.

Offset Cancellation

The offset cancellation is based on VID, COMP voltage and current signal from SUM CSGM to control output voltage accuracy.

Current Balance

Per-phase current sense signal is compared with sensed average current. The comparison result will adjust each phase PWM width to optimize current and thermal balance.

Zero Current Detection

Detect whether each phase current crosses zero current. The result is used for DEM power saving and overshoot reduction (Anti-overshoot Function).

AQR/ANTIOVS

The AQR is a new generation of quick response mechanism (Adaptive Quick Response, AQR) which detects loading rising edge and allows all PWM to turn on. The PWM pulse width triggered by AQR is adaptive to loading level. The AQR trigger level can be set by PINSETTING. ANTIOVS can help overshoot reduction which detects loading falling edge and forces all PWM in tri-state until the zero current is detected.

OCP

The RT3624BE has two over-current protection mechanisms, sum OCP and OC limit.

OVP

The over-voltage protection threshold is linked to VID, please refer to classification table and waveform in Table 17, Figure 23 and Figure 24.

UVP

When the output voltage is lower than VID-650mV with 3μs filter time, UVP will be triggered and all PWM will be in tri-state to turn off high-side power MOSFETs.

Absolute Maximum Ratings (Note 1)

- VIN/VSYS to GND ---------- –0.3V to 28V
- VCC to GND ---------- –0.3V to 6.5V
- RGND to GND ---------- –0.3V to 0.3V
- Other Pins ---------- –0.3V to 6.8V
- Power Dissipation, P_D @ T_A = 25°C

  WQFN-52L 6x6 ---------- 3.77W
- Package Thermal Resistance (Note 2)

  WQFN-52L 6x6, θ_{JA} ---------- 26.5°C/W

  WQFN-52L 6x6, θ_{JC} ---------- 6.5°C/
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)

  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- VIN/VSYS to GND ---------- 4.5V to 24V
- Supply Input Voltage, VCC ---------- 4.5V to 5.5V
- Junction Temperature Range ---------- –10°C to 105°C

Electrical Characteristics

(V_{CC} = 5V, typical values are referenced to T_J = 25°C, Min and Max values are referenced to T_J from –10°C to 105°C, unless other noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Supply Voltage	V_{CC}		4.5	5	5.5	V
Supply Current	I_{VCC}	VRON = H, not switching	--	14	--	mA
Supply Current at PS4	I_{VCC_PS4}	VRON = H, not switching	--	85	--	μA
Shutdown Current	I_{SHDN}	VRON = L	--	--	15	μA
EA Amplifier						
DC Gain	A_{DC}	R_L = 47kΩ	70	--	--	dB
Gain-Bandwidth Product	G_{BW}	C_{LOAD} = 5pF	--	10	--	MHz
Slew Rate	SR_{EA}	C_{LOAD} = 10pF (Gain = –4, Rf = 47kΩ, VOUT = 0.5V to 3V)	--	5	--	V/μs
Output Voltage Range	V_{COMP}	R_L = 47kΩ	0.3	--	3.6	V
Maximum Source/Sink Current	I_{OUTEA}	V_{COMP} = 2V	--	5	--	mA
Current Sensing Amplifier (CORE/AXG/AUX)						
Impedance at Positive Input	R_{ISENxP}		1	--	--	MΩ

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
CS Input Voltage		V_{CSIN}	Differential voltage range of DCR sense. (V_{CSIN}= Inductor current x DCR x DCR divider)	–10	--	80	mV
Current Sense Gain Error		A_{MIRROR}	Internal current mirror gain of per phase current sense I_{IMON} / $I_{CS,PERx}$	0.97	1	1.03	A/A
TON Setting							
On-Time Setting		t_{ON}	VIN = 19V, VID = 0.9V, k_{TON} = 1.36	--	93	--	ns
Minimum Off-Time		t_{OFF}	VID = 1V under PS1 condition	--	130	300	ns
Minimum On-Time		$t_{ON(MIN)}$		--	50	--	ns
Protections							
Under-Voltage Lockout Threshold		$V_{UVLO,rise}$	Rising edge	4.1	--	4.45	V
		V_{UVLO}	Falling edge	3.9	--	4.2	V
		ΔV_{UVLO}	Rising edge hysteresis	100	170	250	mV
Over-Voltage Protection Threshold		V_{OV}	Respect to VID voltage,	VID	VID	VID	mV
			VID >1V	+320	+350	+380	
			VID ≤1V	1.3	1.35	1.4	V
Under-Voltage Protection Threshold		V_{UV}	Respect to VID voltage	–680	–650	–620	mV
VRON and VR_READY							
VRON Threshold	Logic-High	V_{IH}		0.7	--	--	
	Logic-Low	V_{IL}		--	--	0.3	V
Leakage Current of VRON				–1	--	1	µA
VR_READY Pull Low Voltage		V_{VR_READY}	I_{VR_READY} = 10mA	--	--	0.13	V
Serial VID and $\overline{\text{VR\_HOT}}$							
VCLK, VDIO Input Voltage	Logic-High	V_{IH}		0.65	--	--	V
	Logic-Low	V_{IL}		--	--	0.45	
Leakage Current of VCLK and VDIO		I_{LEAK_IN}		–1	--	1	µA
Pull Low Voltage		V_{VDIO}	I_{VDIO} = 10mA	--	--	0.13	V
		$V_{\overline{ALERT}}$	$I_{\overline{ALERT}}$ = 10mA	--	--	0.13	
		$V_{\overline{VR\_HOT}}$	$I_{\overline{VR\_HOT}}$ = 10mA	--	--	0.13	
Leakage Current of $\overline{\text{ALERT}}$, $\overline{\text{VR\_HOT}}$		I_{LEAK_OUT}		–1	--	1	µA
ANS_EN							
ANS_EN Input Voltage	Logic-High	V_{IH}		VCC – 0.5	--	--	V
	Logic-Low	V_{IL}		--	--	1	V

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
V_{REF}							
VREF Voltage		V_{VREF}	Normal operation	0.59	0.6	0.61	V
VREF SPS Voltage		V_{VREF_SPS}	Normal operation	1.2	1.3	1.4	V
ADC							
Digital IMON Set	CORE	d_{VIMON_ICCMAX}	$V_{IMON} - V_{REF}$ = 0.8V @ ICCMAX >=80A $V_{IMON} - V_{REF}$ = 0.4V @ ICCMAX >=40A $V_{IMON} - V_{REF}$ = 0.2V @ ICCMAX <40A	--	255	--	Decimal
	AXG	d_{VIMONA_ICCMAX}	$V_{IMONA} - V_{REF}$ = 0.4V @ ICCMAX >=40A $V_{IMONA} - V_{REF}$ = 0.2V @ ICCMAX <40A	--	255	--	Decimal
	AUX	$d_{VIMON\_AUX\_ICCMAX}$	V_{IMON_AUX}-V_{REF}=1.6V	--	255	--	Decimal
PSYS Maximum Input Voltage		PSYS	V_{PSYS} = 1.6V	--	255	--	Decimal
VSYS Maximum Input Voltage		VSYS	VIN/VSYS=24V	--	255	--	Decimal
Average Period of IMON		t_{IMON}		--	150	--	µs
Average Period of TSEN		t_{TSEN}		--	600	--	µs
TSEN Voltage Threshold to Pull Low $\overline{VR\_HOT}$ (Asserts $\overline{VR\_HOT}$)		$V_{TSEN\_\overline{VR\_HOT}\_L}$	Within the range, $\overline{VR\_HOT}$ = L.	1.105	1.112	1.119	V
TSEN Voltage Threshold to Pull High $\overline{VR\_HOT}$ (De-Asserts $\overline{VR\_HOT}$)		$V_{TSEN\_\overline{VR\_HOT}\_H}$	Within the range, $\overline{VR\_HOT}$ = H	1.147	1.154	1.161	V
TSEN Rises to Pull Low $\overline{ALERT}$		$V_{TSEN\_Status\_H}$	$\overline{ALERT}$ =Low	1.147	1.154	1.161	V
TSEN Down to Pull Low $\overline{ALERT}$		$V_{TSEN\_Status\_L}$	$\overline{ALERT}$ =Low	1.196	1.201	1.208	V
ITSEN							
TSEN Source Current		I_{TSEN}	V_{TSEN} = 1.6V	79.2	80	80.8	µA
Power DoCORE Disable Voltage		V_{PSYS}		VCC – 0.5	--	--	V

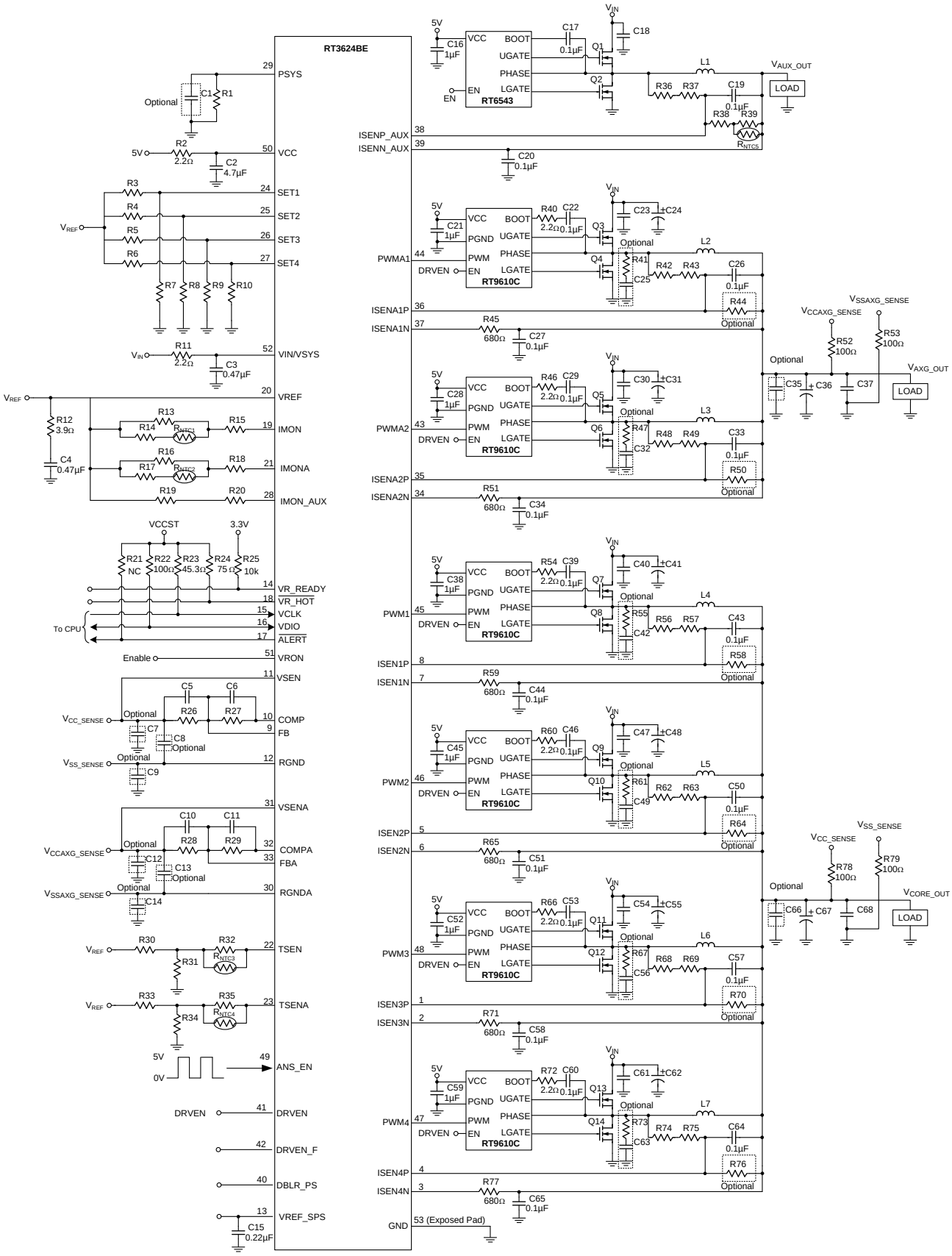
Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit



Application Information

The RT3624BE includes two voltage rails: a 4/3/2/1 phase synchronous buck controller, the CORE VR, and a 2/1 phase synchronous buck controller, the AXG VR, designed to meet Intel IMVP9.1 compatible CPUs specification with a serial SVID control interface. The controller uses an ADC to implement all kinds of settings to save total pin number for easy use and increasing PCB space utilization. The RT3624BE is used in desktop computers or notebook computers.

Power-ON Sequence

In order to confirm sufficient power supply for proper operation, the VR triggers UVLO if VCC pin drops below 4.2V (max). UVLO protection shuts down controller and forces high-side MOSFET and low-side MOSFET off. When VCC > 4.45, RT3624BE issues POR=high and waits for VRON signal. After POR=high and VRON > 0.7V, controller powers on (Chip Enable = H) and starts VR internal settings, which include internal circuit offset correction and function settings (PIN-SETTING). Users can set multi-functions through SETx, TSEN and TSENA pins. Figure 2 shows the typical timing of controller power-on. The pull-high power of VRON pin is recommended as 1.05V, the same power as SVID interface. That can ensure SVID power is ready while VRON = H. Driver power (PVCC) is strongly suggested to be ready after VCC. This can prevent current flow back to VCC from PVCC through PWMx pin or DRVEN pin.

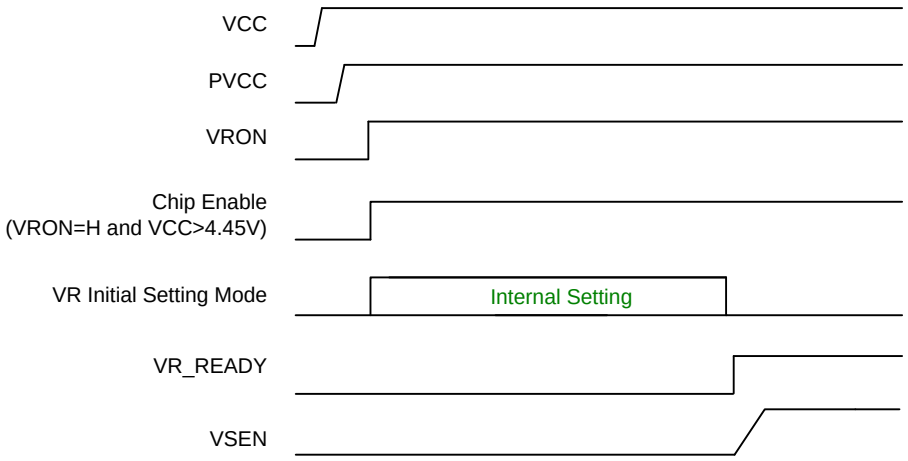


Figure 2. Typical Timing of Controller Power-ON.

Maximum Active phases Number Setting

The number of active phases is determined by ISENxN voltages. The detection is only active and latched at Chip Enable rising edge (VRON = H and VCC > 4.45V). While voltage at ISENxN > (VCC − 0.5V), maximum active phase number is (x-1). For example, pulling ISEN4N to VCC programs a 3-phase operation, while pulling ISEN3N to VCC programs a 2-phase operation. The unused ISENxP pins are recommended to connect to VCC and the unused PWM pins can be floating. Figure 3 is a 3-phase operation example.

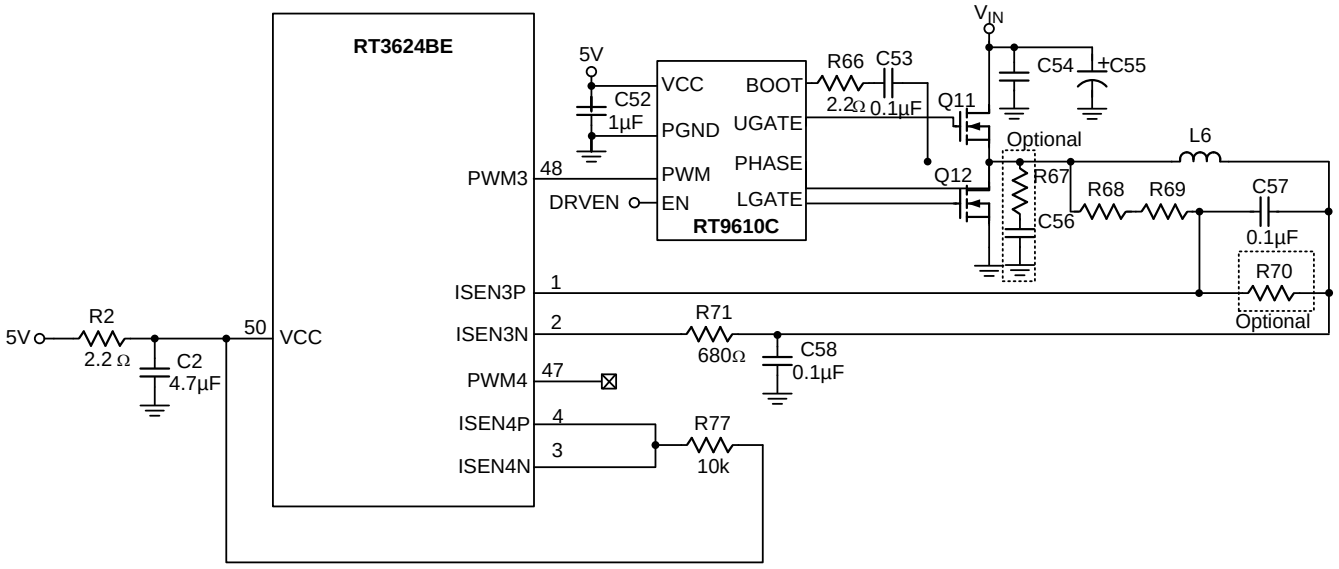


Figure 3. 3-Phases Operation Setting

Rail Disable

Pulling ISEN1N to VCC programs CORE rail disable. The unused ISENxP pins are recommended to connect to VCC and the unused PWMx pins can be floating. Pulling ISENA1N to VCC programs AXG rail disable. The unused ISENAxP pins are recommended to connect to VCC and the unused PWMAx pins can be floating. Pulling the PSYS pin to (VCC – 0.5V) programs input power domain rail disable. RT3624BE will reject any commands to the input power domain rail. The unused ISENP_AUX pin and ISENN_AUX pin are recommended to connect to VCC.

Acoustic Noise Suppression

The RT3624BE supports acoustic noise suppression function for reducing acoustic noise induced by piezoelectric effect from MLCC. As output voltage transition, especially in dynamic VID, the vibrating MLCC produces acoustic noise if the vibrating frequency falls into audible band and the noise level is related to the output voltage transition amplitude ΔV. Therefore, the RT3624BE adopts acoustic noise suppression function which is enabled by pulling ANS pin to VCC to reduce ΔV when SetVID down and SetVID Decay down in DEM mode.

PIN-SETTING Mechanism

The RT3624BE provides multiple parameters for platform setting and BOM optimization. These parameters can be set through SETx and TSEN pins. The RT3624BE adopts two-step PIN-SETTING mechanism to maximize IC pin utilization. Figure 4 illustrates this operating mechanism for SETx.

The Vdivider and Vcurrent can be represented as follows:

$$V_{divider} = \frac{R2}{R1+R2} \times 3.2V$$

$$V_{current} = \frac{R2}{R1+R2} \times 3.2V + 80uA \times \frac{R1 \times R2}{R1+R2}$$

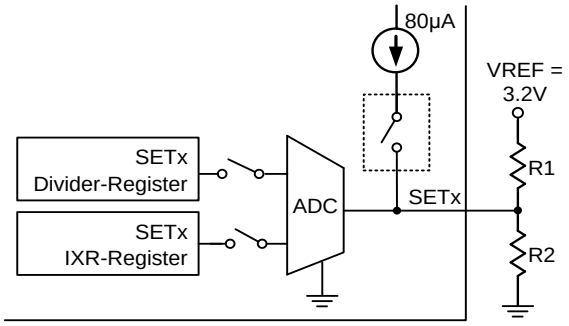


Figure 4. Operating Mechanism for SETx

Divider-Register and IXR-Register set specified functions. For example, Divider-Register of SET1 sets VBOOT and ICCMAX of CORE rail; IXR-Register of SET1 sets AXG rail ICCMAX. All setting functions are summarized in Table 1.

Table 1. Summary of Pin Setting Functions

		Function Setting	Symbol	Description
SET1	Divider Register [4]	Setting VBOOT of CORE rail	VBOOT[4]	VBOOT[4]=0, 0V VBOOT[4]=1, non-zero
	Divider Register[3:0]	CORE VR ICCMAX	ICCMAX[3:0]	According to Platform, set CORE VR corrsponding ICCMAX.
	IXR Register[4:1]	AXG VR ICCMAX	ICCMAX_A[4:1]	According to Platform, set AXG VR corrsponding ICCMAX.
SET2	Divider Register[4]	Setting VBOOT olf AXG rail	VBOOT_A[4]	VBOOT_A[4]=0, 0V VBOOT_A[4]=1, non-zero
	Divider Register[3]	Selectable VID table	VIDT[3]	VIDT[3]=0, VID1(0V~1.52V) VIDT[3]=1, VID2(0V~2.74V)
	Divider Register[2:0]	CORE VR TON width setting (Switching frequency)	k_{TON}[2:0]	According to required frequency, select adaptive k_{TON} parameter
	IXR Register[4:2]	AUX VR ICCMAX	ICCMAX_AUX[4:2]	According to Platform, set AUX VR corrsponding ICCMAX.
	IXR Register[1]	Enable zero load-line for CORE and AXG VR	0LL[1]	0LL[1]=0: Disable zero load line 0LL[1]=1: Enable zero load line
SET3	Divider Register[4:3]	CORE VR undershoot suppression	UDS[4:3]	To improve undershoot by applying a positive offset at loading edge. Set trigger level.
	Divider Register[2]	DVID Fast slew rate	DVID fast_SR[2]	DVID fast_SR[2][0] = 00, 1/2*Fast_P DVID fast_SR[2][0] = 01, 3/4*Fast_P DVID fast_SR[2][0] = 10, Fast_P DVID fast_SR[2][0]= 11, Fast_S
	Divider Register[1]	CORE VR DVID voltage-compensation level	DVID_LIFT[1]	DVID_LIFT[1] = 0: 10uA DVID_LIFT[1] = 1: 20uA current source sink from FB pin
	Divider Register[0]	DVID Fast slew rate	DVID fast_SR[0]	DVID fast_SR[2][0] = 00, 1/2*Fast_P DVID fast_SR[2][0] = 01, 3/4*Fast_P DVID fast_SR[2][0] = 10, Fast_P DVID fast_SR[2][0]= 11, Fast_S
	IXR Register[4:3]	AXG VR undershoot suppression	UDS_A[4:3]	To improve undershoot by applying a positive offset at loading edge. Set trigger level.
	IXR Register[2]	$\overline{\text{VR\_HOT}}$ assertion during DVID current limit	$\overline{\text{VR\_HOT}}$ _DVID[2]	$\overline{\text{VR\_HOT}}$ _DVID[2] = 0,Enable $\overline{\text{VR\_HOT}}$ _DVID[2] = 1,Disable
	IXR Register[1]	AXG VR DVID voltage-compesation level	DVID_LIFT_A[1]	DVID_LIFT_A[1] = 0: 10uA DVID_LIFT_A[1] = 1: 20uA current source sink from FB pin
SET4	Divider Register[4:3]	CORE VR Phase Extension	DBLR[4:3]	DBLR[4:3] = 00 : Enable, Phase=8 DBLR[4:3] = 01 : Disable, Phase=1~4, DBLR[4:3] = 10 : Enable, Phase=5, DBLR[4:3] = 11 : Enable, Phase=6,
	Divider Register[2:0]	AXG VR TON width setting (switching frequency)	k_{TON_A}[2:0]	According to required frequency, select adaptive k_{TON_A} parameter
	IXR Register[4:3]	CORE VR Anti-overshoot trigger level	ANTIOVS_TH[4:3]	ANTIOVS for reduction of overshoot at loading falling edge. Set trigger level.
	IXR Register[2:1]	AXG VR Anti-overshoot trigger level	ANTIOVS_TH_A[2:1]	ANTIOVS for reduction of overshoot at loading falling edge. Set trigger level.

		Function Setting	Symbol	Description
TSEN	Divider Register[4:3]	CORE VR Current Gain	Ai[4:3]	Current gain setting
	Divider Register[2:1]	CORE VR Adaptive Quick Response(AQR) trigger level	AQR_TH[2:1]	AQR for loop response speed-up of loading rising edge. Set trigger level.
TSENA	Divider Register[4:3]	AXG VR Current Gain	Ai_A[4:3]	Current gain setting
	Divider Register[2:1]	AXG VR Adaptive Quick Response(AQR) trigger level	AQR_TH_A[2:1]	AQR for loop response speed-up of loading rising edge. Set trigger level.

Referring to PIN-SETTING tables, Table 2 to 11, users can search corresponding $V_{divider}$ or V_{IXR} according to the desired function setting combinations. Then SETx external resistors can be calculated as follows:

$$R1 = \frac{3.2V \times V_{IXR}}{80\mu A \times V_{divider}}$$

$$R2 = \frac{R1 \times V_{divider}}{3.2V - V_{divider}}$$

Richtek provides a Microsoft Excel-based design tool to calculate the desired PIN-SETTING resisters.

TSEN and TSENA pins also have function settings except for thermal monitoring function. They only utilize divider part of PIN-SETTING mechanism. The functions of TSEN and TSENA include current gain and quick response triggle level. The detailed operation is described in Thermal Monitoring and Indicator section.

Table 2. SET1 Pin Setting for VBOOT and ICCMAX

$V_{divider\_SET1}$ (mV)	VBOOT	ICCMAX(A)						
		8 phase	6 phase	5 Phase	4 Phase	3 Phase	2 Phase	1 Phase
25	0V	232	170	134	85	60	35	10
75		238	176	140	90	64	38	12
125		244	182	146	95	68	41	14
175		250	188	152	100	72	44	16
225		256	194	158	105	76	47	18
275		262	200	164	110	80	50	20
325		268	206	170	115	84	53	22
375		274	212	176	120	88	56	24
425		280	218	182	125	92	59	26
475		286	224	188	130	96	62	28
525		292	230	194	135	100	65	30
575		298	236	200	140	104	68	32
625		304	242	206	145	108	71	34
675		310	248	212	150	112	74	36
725		316	254	218	155	116	77	38
775		322	260	224	160	120	80	40
825	non-zero	232	170	134	85	60	35	10
875		238	176	140	90	64	38	12
925		244	182	146	95	68	41	14
975		250	188	152	100	72	44	16
1025		256	194	158	105	76	47	18
1075		262	200	164	110	80	50	20
1125		268	206	170	115	84	53	22
1175		274	212	176	120	88	56	24
1225		280	218	182	125	92	59	26
1275		286	224	188	130	96	62	28
1325		292	230	194	135	100	65	30
1375		298	236	200	140	104	68	32
1425		304	242	206	145	108	71	34
1475		310	248	212	150	112	74	36
1525		316	254	218	155	116	77	38
1575		322	260	224	160	120	80	40

Table 3. SET1 Pin Setting for ICCMAX_A

V_{IXR_SET1} (mV)	ICCMAX_A (A)	
	2 Phase	1 Phase
50	35	10
150	38	12
250	41	14
350	44	16
450	47	18
550	50	20
650	53	22
750	56	24
850	59	26
950	62	28
1050	65	30
1150	68	32
1250	71	34
1350	74	36
1450	77	38
1550	80	40

Table 4. SET2 Pin Setting for VBOOT_A, VIDT and k_{TON}

$V_{divider\_SET2}$ (mV)	VBOOT_A	VIDT	k_{TON}
25	0V	VID1	0.64
75			0.82
125			1
175			1.18
225			1.36
275			1.55
325			1.73
375			2.27
425		VID2	0.64
475			0.82
525			1
575			1.18
625			1.36
675			1.55
725			1.73
775			2.27
825	non-zero	VID1	0.64
875			0.82
925			1
975			1.18
1025			1.36
1075			1.55
1125			1.73
1175			2.27
1225		VID2	0.64
1275			0.82
1325			1
1375			1.18
1425			1.36
1475			1.55
1525			1.73
1575			2.27

Table 5. SET2 Pin Setting for ICCMAX_AUX and 0LL

V_{IXR_SET2} (mV)	ICCMAX_AUX(A)	0LL
50	10	Disable
150		Enable
250	15	Disable
350		Enable
450	20	Disable
550		Enable
650	25	Disable
750		Enable
850	30	Disable
950		Enable
1050	35	Disable
1150		Enable
1250	40	Disable
1350		Enable
1450	55	Disable
1550		Enable

Table 6. SET3 Pin Setting for UDS, DVID_LIFT and DVID fast_SR

$V_{divider\_SET3}$ (mV)	UDS		DVID_LIFT	DVID fast_SR
	PS0	PS1		
25	Disable	Disable	10uA	1/2*Fast_P
75				3/4*Fast_P
125			20uA	1/2*Fast_P
175				3/4*Fast_P
225			10uA	Fast_P
275				Fast_S
325			20uA	Fast_P
375				Fast_S
425	200	125	10uA	1/2*Fast_P
475				3/4*Fast_P
525			20uA	1/2*Fast_P
575				3/4*Fast_P
625			10uA	Fast_P
675				Fast_S
725			20uA	Fast_P
775				Fast_S
825	200	175	10uA	1/2*Fast_P
875				3/4*Fast_P
925			20uA	1/2*Fast_P
975				3/4*Fast_P
1025			10uA	Fast_P
1075				Fast_S
1125			20uA	Fast_P
1175				Fast_S
1225	250	150	10uA	1/2*Fast_P
1275				3/4*Fast_P
1325			20uA	1/2*Fast_P
1375				3/4*Fast_P
1425			10uA	Fast_P
1475				Fast_S
1525			20uA	Fast_P
1575				Fast_S

Table 7. SET3 Pin Setting for UDS_A, $\overline{\text{VR\_HOT}}$ _DVID and DVID_LIFT_ A

V_{IXR_SET3} (mV)	UDS_A		$\overline{\text{VR\_HOT}}$ _DVID	DVID_LIFT_A
	PS0	PS1		
50	Disable	Disable	Enable	10uA
150				20uA
250			Disable	10uA
350				20uA
450	200	125	Enable	10uA
550				20uA
650			Disable	10uA
750				20uA
850	200	175	Enable	10uA
950				20uA
1050			Disable	10uA
1150				20uA
1250	250	150	Enable	10uA
1350				20uA
1450			Disable	10uA
1550				20uA

Table 8. SET4 Pin Setting for DBLR and k_{TON_A}

$V_{divider\_SET4}$ (mV)	DBLR	k_{TON_A}
25	Eable DBLR 8phase	0.64
75		0.82
125		1
175		1.18
225		1.36
275		1.55
325		1.73
375		2.27
425	Disable DBLR	0.64
475		0.82
525		1
575		1.18
625		1.36
675		1.55
725		1.73
775		2.27
825	Enable DBLR 5 phase	0.64
875		0.82
925		1
975		1.18
1025		1.36
1075		1.55
1125		1.73
1175		2.27
1225	Enable DBLR 6 phase	0.64
1275		0.82
1325		1
1375		1.18
1425		1.36
1475		1.55
1525		1.73
1575		2.27

Table 9. SET4 Pin Setting for ANTIOVS_TH and ANTIOVS_TH_A

V_{IXR_SET4} (mV)	ANTIOVS_TH	ANTIOVS_TH_A
50	90mV	90mV
150		150mV
250		210mV
350		Disable
450	150mV	90mV
550		150mV
650		210mV
750		Disable
850	210mV	90mV
950		150mV
1050		210mV
1150		Disable
1250	Disable	90mV
1350		150mV
1450		210mV
1550		Disable

Table 10. TSEN Pin Setting for Ai and AQR_TH

V_{TSEN} (mV)	Ai	AQR_TH
50	0.25	720
150		880
250		1040
350		1200
450		1360
550		1520
650		1680
750		Disable
850	0.5	720
950		880
1050		1040
1150		1200
1250		1360
1350		1520
1450		1680
1550		Disable
1650	0.75	720
1750		880
1850		1040
1950		1200
2050		1360
2150		1520
2250		1680
2350		Disable
2450	1	720
2550		880
2650		1040
2750		1200
2850		1360
2950		1520
3050		1680
3150		Disable

Table 11. TSENA Pin Setting for Ai_A and AQR_TH_A

V_{TSENA} (mV)	Ai_A	AQR_TH_A
50	0.25	720
150		880
250		1040
350		1200
450		1360
550		1520
650		1680
750		Disable
850	0.5	720
950		880
1050		1040
1150		1200
1250		1360
1350		1520
1450		1680
1550		Disable
1650	0.75	720
1750		880
1850		1040
1950		1200
2050		1360
2150		1520
2250		1680
2350		Disable
2450	1	720
2550		880
2650		1040
2750		1200
2850		1360
2950		1520
3050		1680
3150		Disable

Thermal Monitoring and Indicator

TSEN pin processes two functions of PIN-SETTING (function setting) and thermal monitoring. After power on, TSEN has three operation modes: PIN-SETTING, Pre-thermal Sense and Thermal Sense Mode. The corresponding function blocks of the three modes are shown in Figure 5. In PIN-SETTING Mode, TSEN pin voltage = 3.2V x R2 / (R1+R2) with VREF = 3.2V and is coded by ADC and stored in PIN-SETTING register. In Pre-Thermal Sense Mode, TSEN pin voltage = 0.6V x R2 / (R1+R2) with VREF = 0.6V and is coded and stored in Pre-Thermal Register. This part helps Thermal Sense Mode calculation. In Thermal Sense Mode, TSEN pin voltage = 0.6V x R2 / (R1+R2) + 80uA x [(R1//R2)+R3] with VREF = 0.6V and is coded. The result will subtract Pre-Thermal Register code and stored in Thermal Register (The corresponding TSEN voltage = 80μA x [(R1//R2)+R3] that's defined as Thermal Voltage. R3 is the NTC thermistor network to sense temperature.) NTC thermistor is recommended to be placed near the MOSFET, the hottest area in the PCB. Higher temperature causes smaller R3 and lower TSEN. According to NTC thermistor temperature curve, design Thermal Voltage v.s Temperature with proper R3 network to meet Intel temperature zone. 100°C Thermal Voltage = 80μA x [(R1//R2)+R3(100°C)] = 1.105V must be required. Controller processes the TSEN pin voltage to report temperature zone register. While the TSEN pin voltage is less than 1.105V, the VR_HOT will be pulled low to indicate thermal alert. The signal is an open-drain signal. Thermal Register data is updated every 75μs and average interval is 600μs. The resistance accuracy of TSEN network is recommended to be less than 1% error.

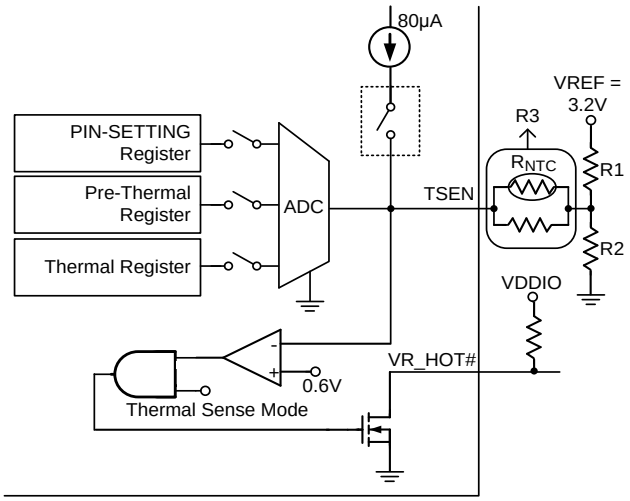


Figure 5. Multi-Function Pin Setting Mechanism for TSEN

System Input Power Monitoring (PSYS)

The RT3624BE provides PSYS function to monitor total platform system power and report to the CPU via SVID interface. The PSYS function can be illustrated as in Figure 6. PSYS meter measures system input current and outputs a proportional current signal I_{PSYS}. R_{PSYS} is designed for the P_{SYS} voltage = 1.6V with maximum IPSYS for 100% system input power. 1.6V is a full-scale analog signal for FFh digitized code.

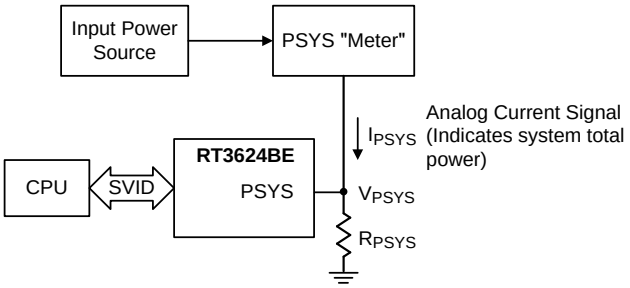


Figure 6. PSYS Function Block Diagram

System Input Voltage Monitoring (VSYS)

The RT3624BE provides optional VSYS function to monitor system input voltage. The threshold can be set through SVID interface and FFh digitized code indicates for 24V input voltage (24V/255 pre code).If input voltage is lower than critical threshold, controller will assert $\overline{\text{VR\_HOT}}$.

Zero Load-line

The RT3624BE also can support enable zero load-line function. When zero load-line function is enabled, the output voltage is determined only by VID and does not vary with the loading current like load-line system behavior. The RT3624BE adopts AC-droop to effectively suppress load transient ring back and control overshoot for zero load-line application. Figure 7 shows the condition without AC-droop control. The output voltage without AC-droop control has extra ring back ΔV2 due to C area charge. Figure 8 shows the condition with AC-droop control. While loading occurs, controller will temporarily change VID target to short-term voltage target. Short-term voltage target is related to transient loading current ΔI_{CC} and can be represented as the following:

$$Short\_Term\_Voltage\_Target=VID-\Delta I_{CC}\times R_{LL}$$

The setting method of R_{LL} is the same as loadline system. The short-term voltage target reverts to VID target slowly after a period of time. The short-term voltage target can help inductor current not to exceed loading current too much and then the ring back ΔV2 can be suppressed. The overshoot amplitude is reduced to only ΔV3.

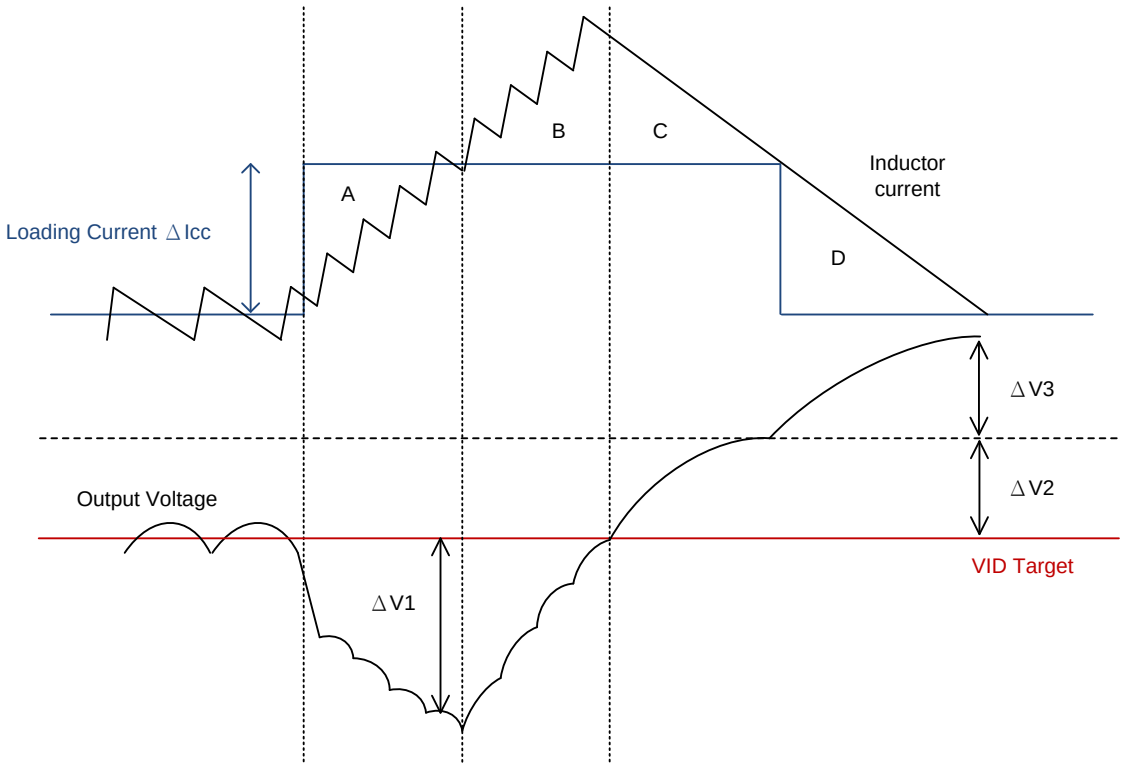


Figure 7. Zero Load-line without AC-droop Control

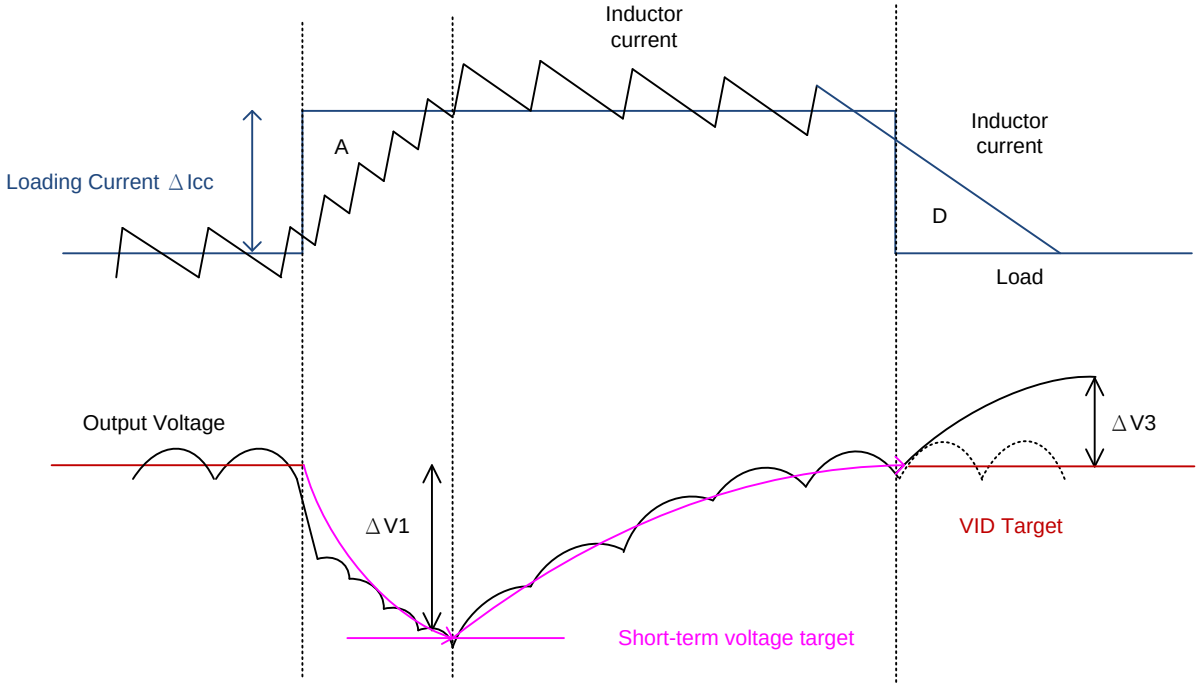


Figure 8. Zero Load-line with AC-droop Control

Per Phase Current Sense

To achieve higher efficiency, the RT3624BE adopts inductor DCR current sensing to get each phase current signal, as illustrated in Figure 9. An external low-pass filter R_{X1} and C_X reconstruct the current signal. The low-pass filter time constant $R_{X1} \times C_X$ should match time constant $\frac{L_X}{DCR}$ of Inductance and DCR. It's fine to fine tune R_{X1} and C_X for transient performance and current reporting. If RC network time constant matches inductor time constant $\frac{L_X}{DCR}$, an ideal load transient waveform can be designed. If RC network time constant is larger than inductor time constant $\frac{L_X}{DCR}$, VCORE waveform has a sluggish droop during load transient. If RC network is smaller than inductor time constant $\frac{L_X}{DCR}$, VCORE waveform sags to create an undershooting to fail the specification and mis-trigger over-current protections (sum OCP). Figure 11 shows the output waveforms according to the RC network time constant.

The R_{X1} is highly recommended as two 0603 size resistors in series to enhance the Iout reporting accuracy. C_X is suggested to be 0.1μF X7R/0603 for low de-rating value of high frequency.

$$I_{CS,PERx} = \frac{V_{CSIN}}{680\Omega} = \frac{I_{Lx} \times DCR}{680\Omega}$$

R_{X2} is optional for preventing V_{CSIN} from exceeding current sense amplifier input range. The time constant of $(R_{X1}//R_{X2}) \times C_X$ should match $\frac{L_X}{DCR}$.

$$I_{CS,PERx} = \frac{V_{CSIN}}{680\Omega} = \frac{I_{Lx} \times DCR}{680\Omega} \times \frac{R_{X2}}{R_{X1}+R_{X2}}$$

The current signal $I_{CS,PERx}$ is mirrored for loadline control/current reporting, current balance and zero current. The mirrored current to IMON pin is one time of $I_{CS,PER}$,

($I_{IMON} = A_{MIRROR} \times I_{CS,PERx}$, $A_{MIRROR}=1$)

The current sense lines must be routed as differential pair from the inductor to the controller on the same layer.

The AUX current sense is demonstrated in Figure 10. In this design, the R_{CS} is equal to 1kΩ and the mirror-gain is 1.25 time of $I_{CS,PER}$. ($I_{IMON} = A_{MIRROR} \times I_{CS,PERx}$, $A_{MIRROR}=1.25$)

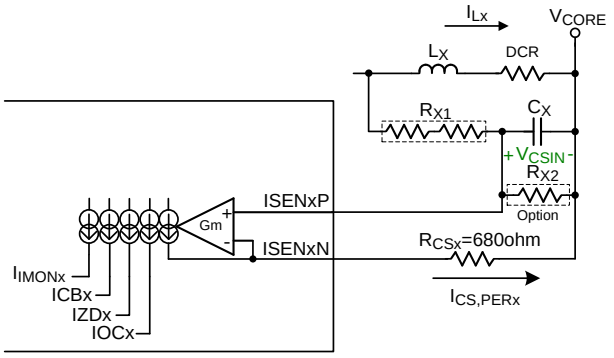


Figure 9. Inductor DCR Current Sensing Method for CORE/AXG

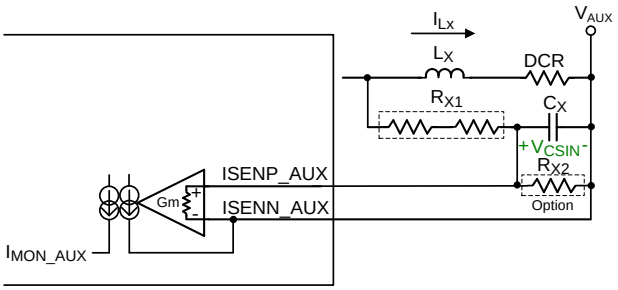


Figure 10. Inductor DCR Current Sensing Method for AUX

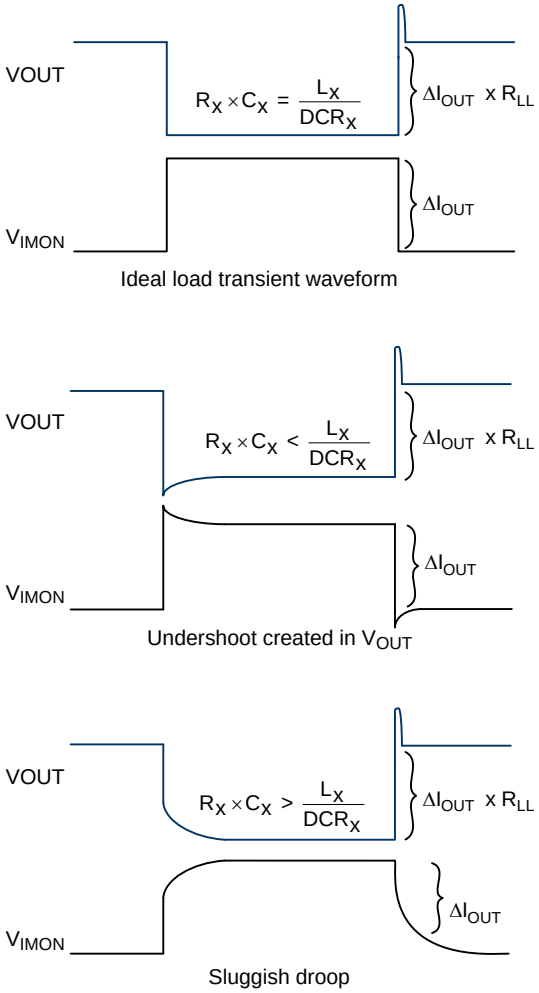


Figure 11. All Kinds of RC Network Time Constant

Total Current Sense/ICCMAX Setting/Current Monitoring

To compensate DCR positive temperature coefficient, conventional current sense method needs an NTC resistor for per phase current loop. The RT3624BE adopts a patented total current sense method that requires only one NTC resistor for thermal compensation. The NTC resistor is designed within I_{MON} resistor network on IMON pin. It is suggested to be placed near the inductor of the first phase. Figure 12 shows the configuration. All phase current signals are gathered to IMON pin and converted to a voltage signal V_{IMON} by $R_{IMON, EQ}$ based on VREF pin. The VREF pin provides 0.6V voltage source (as presented as V_{VREF}) while normal operation. The relationship between V_{IMON} and inductor current I_{Lx} is:

$$V_{IMON}-V_{VREF}=(I_{L1}+I_{L2}+\ldots)\times\frac{DCR}{680\Omega}\times R_{IMON,EQ}$$

V_{IMON}-V_{VREF} is proportional to output current. V_{IMON}-V_{VREF} is used for output current reporting and loadline loop-control and Sum over-current protection. For the former, V_{IMON}-V_{VREF} is averaged by analog low-pass filter and then outputs to 8-bit ADC. The digitized reporting value is scaled such that FFh = ICCMAX. The $R_{IMON,\ EQ}$ should be designed that V_{IMON}-V_{VREF}=V_{ICCMAX} while $(I_{L1}+I_{L2}+\ldots)=ICCMAX_{CORE}=CORE$ ICC_MAX register value, where V_{ICCMAX} setting for each rail is shown below :

For CORE rail,

V_{ICCMAX}=0.8V, when ICCMAX>80A

V_{ICCMAX}=0.4V, when 80A≥ICCMAX≥40A

V_{ICCMAX}=0.2V, when 40A>ICCMAX

For AXG rail,

V_{ICCMAX}=0.4V, when ICCMAX≥40A

V_{ICCMAX}=0.2V, when 40A>ICCMAX

For AUX,

V_{ICCMAX}=1.6V for all ICCMAX setting

The behavior is masked during DVID. For load-line loop control, V_{IMON} − V_{VREF} is scaled by a percentage of Ai, that can be selected by Ai[1:0] of PIN-SETTING. The detailed application is described in the load-line setting section.

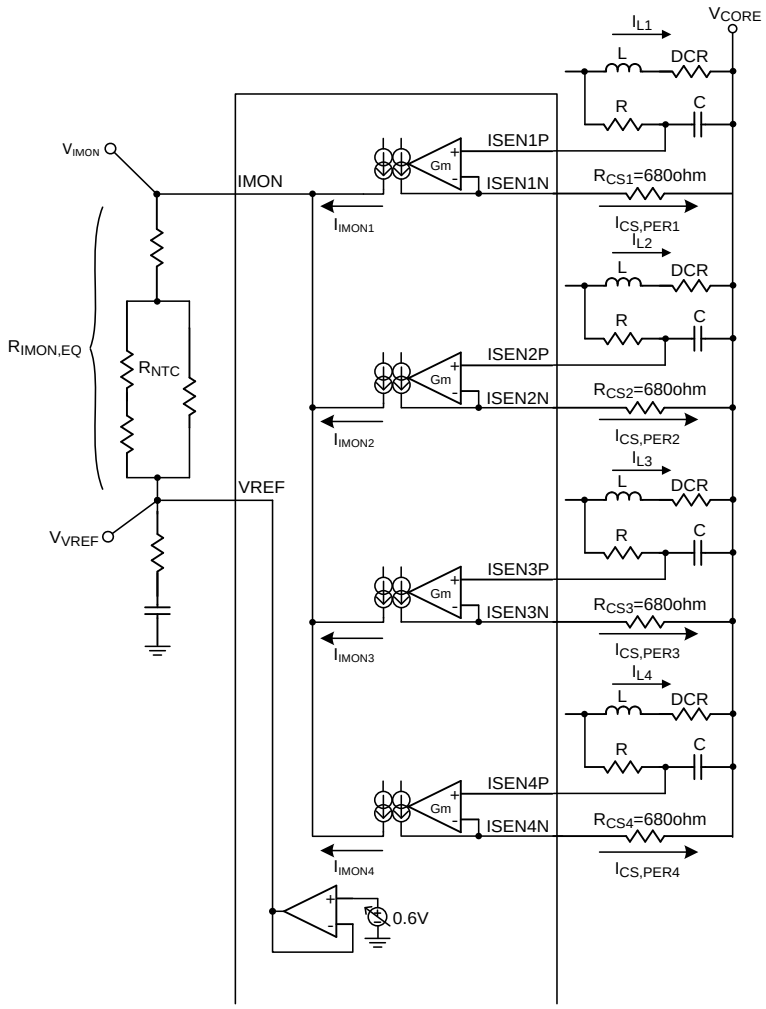


Figure 12. Total Current Sense Method

Load-line Setting (R_{LL})

An output voltage load-line (Adaptive Voltage Positioning) is specified in CPU VR for power saving and output capacitance reduction. The characteristic of load-line is that the output voltage decreases by an amount proportional to the increasing loading current, i.e. the slope between output voltage and loading current (R_{LL}) is shown in Figure 13. Figure 14 shows how the voltage and current loop parameters of RT3624BE to achieve load-line. The detailed equation is described as below :

$$R_{LL} = \frac{\text{Current Loop Gain}}{\text{Voltage Loop Gain}} = \frac{DCR}{680\Omega} \times R_{IMON,EQ} \times \frac{A_i}{\frac{R_{EA2}}{R_{EA1}}} \times \frac{3}{2}$$

Ai is current gain. $\frac{R_{EA2}}{R_{EA1}}$ is ERROR AMP gain and suggested to be greater than 2 for better transient response. R_{LL} can be programmed by Ai and $\frac{R_{EA2}}{R_{EA1}}$. Ai can be selected by PIN-SETTING of Ai[1:0] as listed in Table 12.

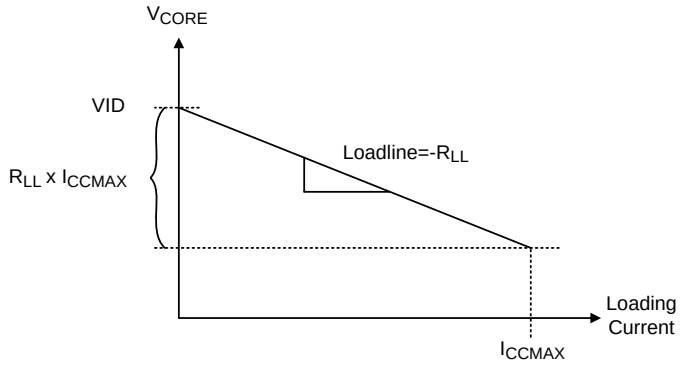


Figure 13. Load-Line (Droop)

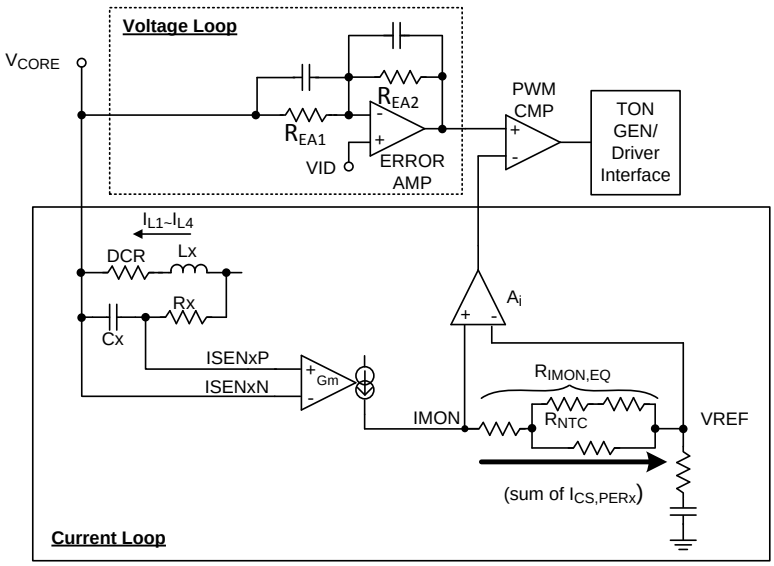


Figure 14. Voltage Loop and Current Loop for Loadline

Table 12. PIN-SETTING of Ai

Ai[1:0]	Current Gain Setting
00	0.25
01	0.50
10	0.75
11	1.00

Dynamic VID (DVID) Compensation

During DVID transition, an extra current is required to charge output capacitors for increasing voltage. The charging current approximates to the product of the DVID slew rate and output capacitance. For droop system, the extra charging current induces extra voltage droop so that the output voltage cannot reach target within the specified time. The extra voltage drop approximates to DVID Slew Rate x Output Capacitance x R_{LL} (R_{LL} is the loadline slope, Ω) This phenomenon is called droop effect. How charging current affects loop is illustrated in Figure 15. The RT3624BE provides one DVID compensation function as shown in Figure 16. An internal current I_{DVID_LIFT} is sinking internally from FB pin to generate DVID compensation, $I_{DVID\_LIFT} \times R_{EA1}$. I_{DVID_LIFT} for fast DVID SR can be set from SET3 PIN-SETTING of DVID_LIFT[1], 10μA and 20μA. For different scale of DVID SR, I_{DVID_LIFT} is internally adjusted. Compensating magnitude can also be adjusted by R_{EA1}. While DAC just arrives target ($\overline{\text{ALERT}}$ issue timing), inductor current is still high and needs a time to settle down to the DC loading current. In the settling time, the falling down current keeps to charge output capacitor (The magnitude is related with inductor, capacitance and VID). Thus, DVID compensation can be less than DVID Slew Rate x Output Capacitance (Capacitance degeneration should be considered). While output capacitance is so large that DVID compensation cannot cover, adding a resistor and capacitor from FB to GND also can provide similar function. The ERROR AMP compensation (resistance and capacitance network among VSEN, FB and COMP) also affects DVID behavior. The final setting should be based on actual measurement.

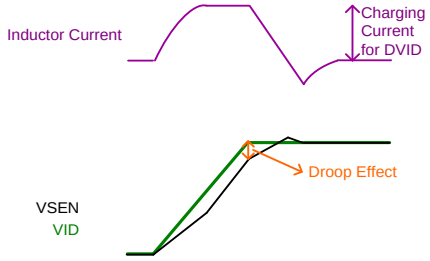


Figure 15. Droop Effect in VID Transition

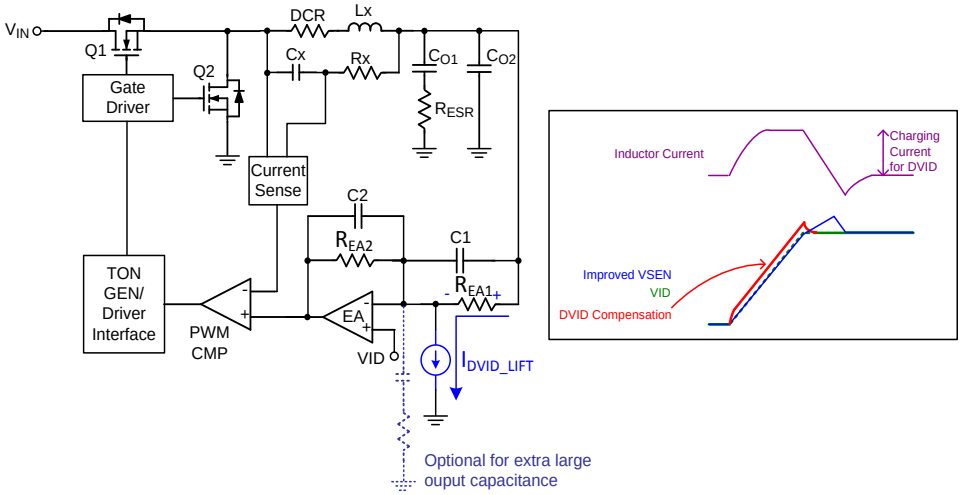


Figure 16. DVID Compensation

Compensator Design

The compensator of the RT3624BE doesn't need a complex type II or type III compensator to optimize control loop performance. It can adopt a simple type I compensator (one pole, one zero) in the G-NAVP^{TM} topology to fine tune ACLL performance. The one pole and one zero compensator is shown in Figure 17. For IMVP9.1 ACLL specification, it is recommended to adjust compensator according to load transient ring back level. Default compensator values are referred to the design tool.

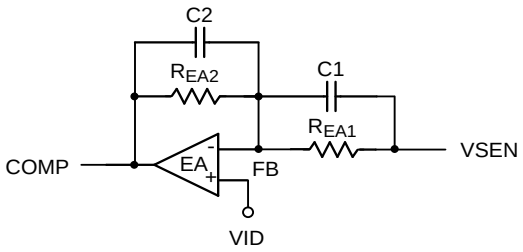


Figure 17. Type I Compensator

Differential Remote Sense Setting

The VR provides differential remote-sense inputs to eliminate the effects of voltage drops along the PC board traces, CPU internal power routes and socket contacts. The CPU contains on-die sense pins, V_{CC_SENSE} and V_{SS_SENSE}. The related connection is shown in Figure 18. The VID voltage (DAC) is referred to RGND to provide accurate voltage at remote CPU side. While CPU is not mounted on the system, two resistors of typical 100Ω are required to provide output voltage feedback.

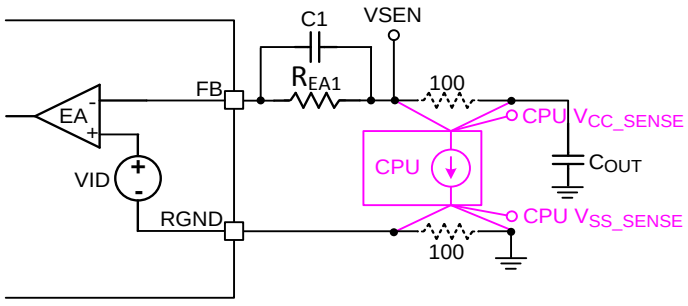


Figure 18. Remote Sensing Circuit

Switching Frequency Setting

The RT3624BE topology G-NAVP^{TM} (Green Native AVP) is one kind of current-mode constant on-time control. It generates an adaptive T_{ON} (PWM) with input voltage (VIN) for better line regulation. The T_{ON} is also adaptive to VID voltage to achieve constant frequency concept. The constant frequency will let switching thermal easier to estimate. The RT3624BE provides a parameter setting of k_{TON} to design T_{ON} width. k_{TON} is set by PIN-SETTING of k_{TON}[2:0]. The related setting table is listed in Table 13.

The equations of T_{ON} are listed as below :

VID ≥ 0.93V

$$Ton=2.206u\times\frac{VID}{k_{Ton}\cdot(VIN)}+14ns$$

VID < 0.93V

$$Ton=2.05158u\times\frac{1}{k_{TON}\cdot(VIN)}+14ns$$

Table 13. PIN-SETTING of k_{TON}

k_{TON}[2:0]	k_{TON}
000	0.64
001	0.82
010	1
011	1.18
100	1.36
101	1.55
110	1.73
111	2.27

The switching frequency can be derived from T_{ON} as shown as below. The losses in the CORE power stage and driver characteristics are considered.

$$Freq=\frac{VID+\frac{I_{CC}}{N}\times(DCR+\frac{R_{ON_{LS,max}}}{n_{LS}}-N\times R_{LL})}{\left[V_{IN}+\frac{I_{CC}}{N}\times\left(\frac{R_{ON_{LS,max}}}{n_{LS}}-\frac{R_{ON_{HS,max}}}{n_{HS}}\right)\right]\times(T_{ON}-T_D+T_{ON,\,VAR})+\frac{I_{CC}}{N}\times\frac{R_{ON_{LS,max}}}{n_{LS}}\times T_D}$$

VID: VID voltage

VIN: input voltage

I_{CC}: loading current

N: total phase number

$R_{ON_{HS,max}}$: maximum equivalent high-side $R_{DS(ON)}$

n_{HS}: number of high-side MOSFETs

$R_{ON_{LS,max}}$: maximum equivalent low-side $R_{DS(ON)}$

n_{LS}: number of low-side MOSFETs.

T_D: summation of the high-side MOSFET delay time and rising time

$T_{ON,\,VAR}$: on-time variation value

DCR: inductor DCR

R_{LL}: loadline setting (Ω).

Adaptive Quick Response (AQR)

The RT3624BE adopts Adaptive Quick Response (AQR) to optimize transient response. The mechanism concept is illustrated in Figure 19. Controller detects output voltage drop slew rate. While the slew rate exceeds the AQR threshold, all PWM will turn on an 53.3% constant on time. The RT3624BE provides various AQR threshold through PIN-SETTING of AQR_TH. The following equation can initially decide the AQR starting trigger threshold. Note that the threshold should be larger than steady-state output voltage ripple falling slew rate and also the overshoot falling slew rate to avoid miss trigger AQR.

$$\text{AQR Starting Trigger Threshold} = -4\mu \times \frac{dVSEN}{dt}$$

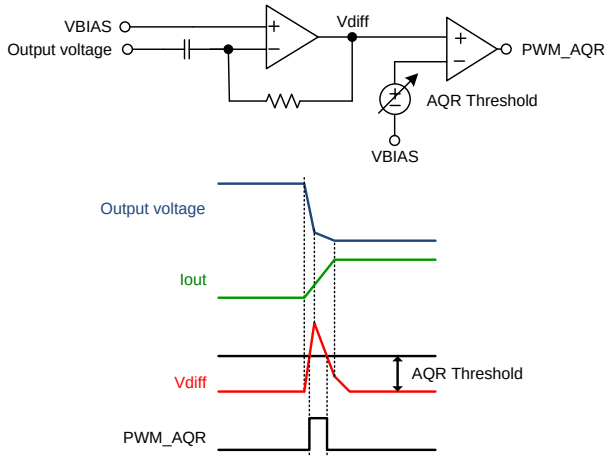


Figure 19. Adaptive Quick Response Mechanism

Table 14. PIN-SETTING of AQR_TH

AQR_TH[2:0]	AQR Starting Trigger Threshold (mV)
000	720
001	880
010	1040
011	1200
100	1360
101	1520
110	1680
111	Disable

Anti-overshoot (ANTI-OVS)

The RT3624BE provides anti-overshoot function to depress output voltage overshoot. Controller detects overshoot by signals related to output voltage. The overshoot trigger level can be adjusted by PIN-SETTING as listed in Table 15. The CORE detecting signal comes from COMP. However, COMP varies with compensation. Initial trigger level setting is based on the following equation :

$$\Delta COMP \times \frac{4}{3} = \Delta VSEN \times \frac{R_{EA2}}{R_{EA1}} \times \frac{4}{3} >$$

Antiovershoot Threshold of ANTIOVS_TH[1:0]

The final setting should be according to actual Error AMP compensator design and measurement.

While overshoot exceeds the setting trigger level, all PWMs keep in tri-state until the zero current is detected or VSEN back to normal level. Turning off LGs forces positive current flow through body diode to cause diode forward voltage. The extra forward voltage can speed up inductor current discharge and decrease overshoot.

Table 15. PIN-SETTING of Anti-Overshoot Threshold

ANTIOVS_TH[1:0]	Anti-overshoot Threshold (mV)
00	90
01	150
10	210
11	Disable

ACLL Performance Enhancement

The RT3624BE provides another optional function to improve undershoot by applying a positive offset at loading edge. Controller detects the COMP signal and compares it with steady state. While VCOMP variation exceeds a threshold, an additional positive offset will apply to the output voltage. The threshold can be set through PINSETTING and separately for PS0 and PS1 as listed in Table 16. The smaller index indicates the easier detection being triggered. The positive offset is related to the compensation.

The ACLL performance enhancement threshold can approximate to $60mV/\frac{V_{EA2}}{V_{EA1}}$. In PS0, the slew rate of VRAMP will increase when the VCOMP intersects the positive offset. In order to send out another on-time earlier to improve undershoot. In PS1, except for the positive offset, an additional 10mV is applied to the DAC and one pulse of PWM is also forced to turn on while the function is triggered. The positive offset is released gradually with about hundred micro-second. Figure 20 and Figure 21 show undershoot suppression behavior in PS0 and PS1. For different platform, the optimized setting is different. The final setting must be based on actual measurement

Table 16. PIN-SETTING of Undershoot Suppression

UDS[1:0]	PS0 (Index)	PS1 (Index)
00	Disable	Disable
01	200	125
10	200	175
11	250	150

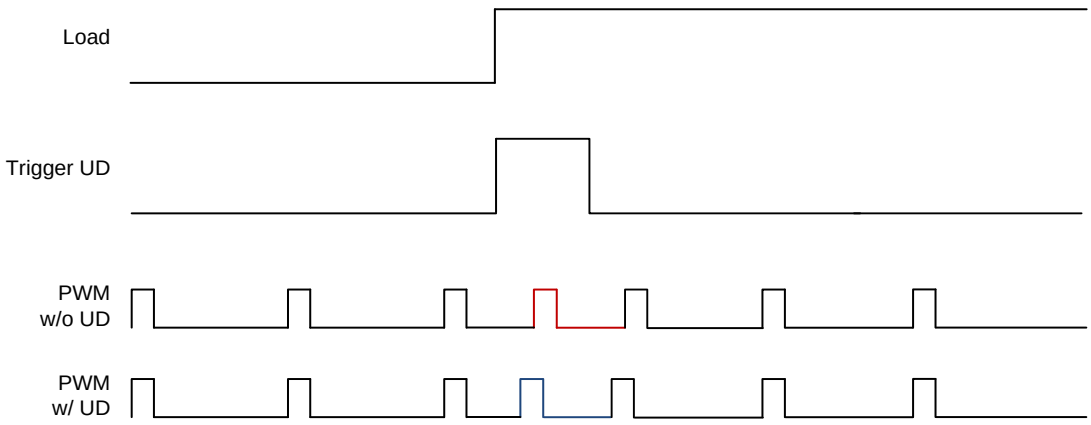


Figure 20. Undershoot Suppression Behavior in Multi Phase.

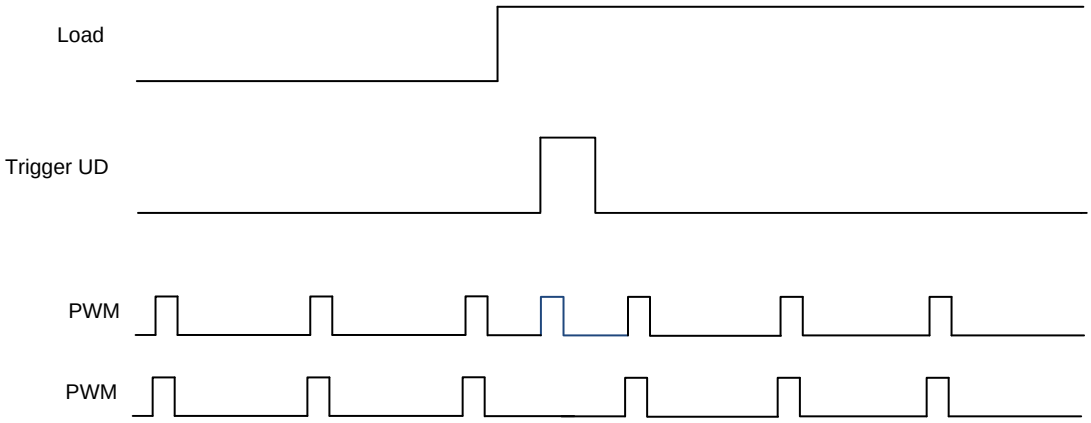


Figure 21. Undershoot Suppression Behavior in Single Phase

Over-Current Protection (OCP)

The RT3624BE has sum OCP mechanisms, the threshold of sum OCP for PS0 is defined as

$$I_{SUM_{OC},PS0}=K_{SOCP}\times VIMON_{ICCMAX}\times\frac{R_{CS}}{DCR}\times\frac{1}{R_{IMON,EQ}}$$

$$I_{SUM_{OC},PS1,2,3}=\frac{1}{\text{phase number}}\times K_{SOCP}\times VIMON_{ICCMAX}\times\frac{R_{CS}}{DCR}\times\frac{1}{R_{IMON,EQ}}$$

ICCMAX<40, KSOCP=1.6

ICCMAX>=40, KSOCP=1.3

While $R_{IMON,EQ}$ is designed exactly for $VIMON_{ICCMAX}$=ICCMAX register value$\times\frac{DCR}{680\Omega}\times R_{IMON,EQ}$, ICCMAX register value=ICCMAX, and $VIMON_{ICCMAX}$=0.2V, 0.4V or 0.8V according to ICCMAX.

Sum OCP threshold can be simplified as $I_{SUM\_OC,PS0}=K_{SOCP}\times ICCMAX$ and $I_{SUM\_OC,PS1,2,3}=\frac{1}{\text{phase number}}\times K_{SOCP}\times ICCMAX$. Note that the modification of ICCMAX register value cannot change sum OCP threshold.

While inductor current above sum OCP threshold lasts 40μs or 0.5μs during the first DVID up plus 80μs, controller de-asserts VR_READY and latches PWM in tri-state to turn off high-side and low-side power MOSFETs. Sum OCP is masked during DVID period and 80μs after VID settles except for the first DVID up plus 80μs. It's also masked while VID = 0V condition.

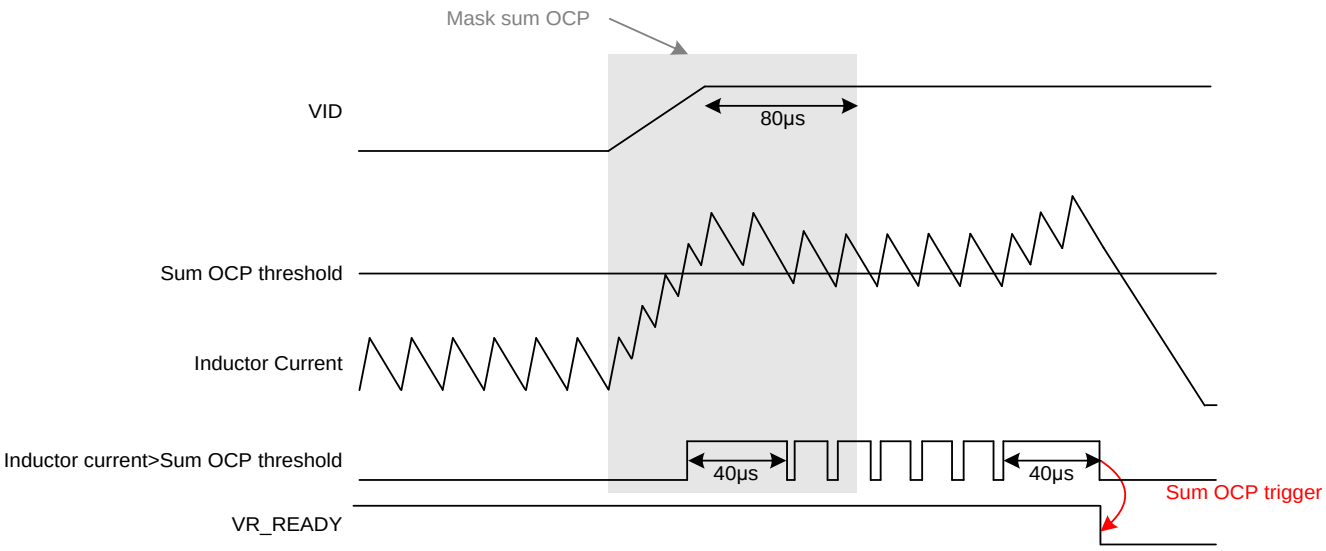


Figure 22. SUM OC Protection Mechanism

Over-Voltage Protection (OVP)

The OVP threshold is linked with VID. The classification table is illustrated in Table 17. While VID = 0V, in case of VR internal setting mode or DACOFF or PS4, OVP is masked. When VID ramps up from VID = 0V till the first PWM after VID settles, OVP threshold is 2.45V to allow not-fully-discharged VSEN. Otherwise, the OVP threshold is relative to VID and equals to VID+350mV with minimum limit = 1.35V. While VID ≤ 1.0V, the OVP threshold is limited at 1.35V.

The OV protection mechanism is illustrated in Figure 23 and Figure 24. When OVP is triggered with 0.5µs filter time, controller de-asserts VR_READY and forces all PWMs low to turn on low-side power MOSFETs. PWM remains low until the output voltage is pulled down below 2.1V for DVID from 0V and VID for other conditions. After 60µs from OVP trigger, VID starts to ramp down to 0V with slow slew rate. During the period, PWM is not allowed to turn on. Controller controls PWM to be low or tri-state to pull down the output voltage along with VID.

Table 17. Summary of Over Voltage Protection

VID Condition	OVP Threshold	Example	Protection Flag	Protection Action	Protection Reset
VID=0 (EN=L or VR internal setting mode or DACOFF or PS4)	OVP is masked		VREF=1V		VCC/VRON Toggle
DVID up period from 0V to 1st PWM pulse after VID settles	2.45V.			VR_READY latched low. Actively pulls the output voltage to below 2.1V, then ramp down to 0V	
DVID period from non-zero VID	VID+350mV if VID >1.0V, 1.35V if VID ≤1.0V	VID = 1.2V, OVP threshold = 1.55V. VID = 0.9V, OVP threshold = 1.35V.		VR_READY latched low. Actively pulls the output voltage to below VID, then ramp down to 0V	
VID≠0	VID+350mV if VID >1.0V, 1.35V if VID ≤1.0V	VID = 1.2V, OVP threshold = 1.55V. VID = 0.9V, OVP threshold = 1.35V.			

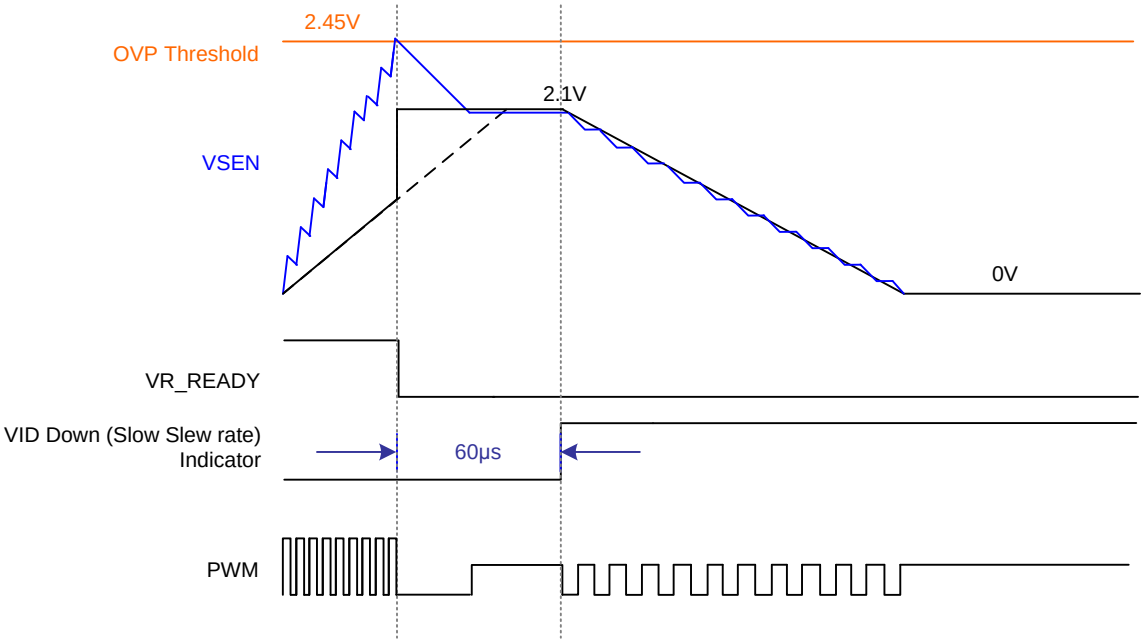


Figure 23. Over-Voltage Protection Mechanism for DVID up from 0V

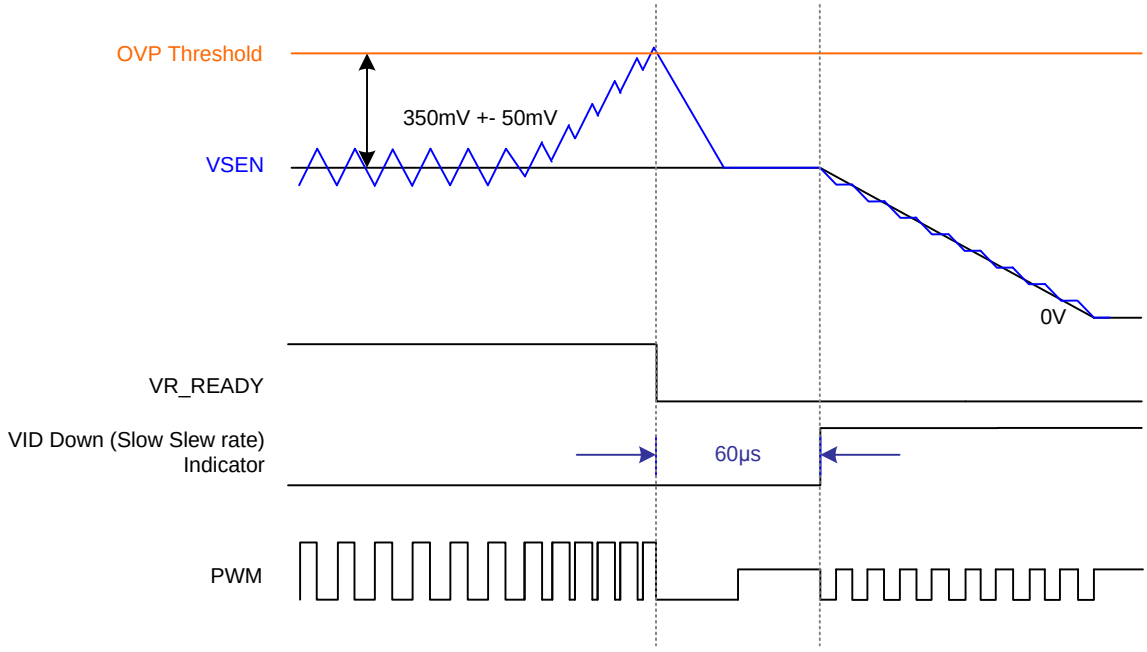


Figure 24. Over-Voltage Protection Mechanism

Under-Voltage Protection

When the output voltage is lower than VID-650mV with 3µs filter time, UVP is triggered and all PWM are in tri-state to turn off high-side and low-side power MOSFETs. UVP is masked during DVID period and 80µs after VID settles. The mechanism is illustrated in Figure 25.

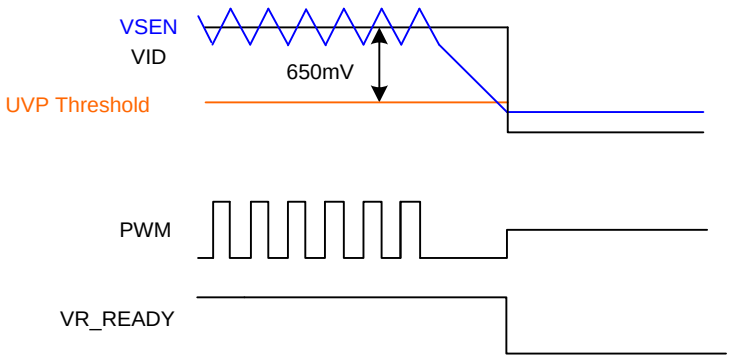


Figure 25. Under-Voltage Mechanism

All protections are reset only by VCC/VRON toggle. UVP and OCP protections are listed in Table 18. Note that the real filter time also depends on the magnitude of detected signal. The signal magnitude will affect analog comparator's overdrive voltage and output slew rate. For user friendly, RT3624BE provides protection flag to promptly determine which kind of protections is triggered. As protection happens, VREF will be forced to 1V/1.5V/2V for OVP/UVP/SUM_OCP, respectively.

Table 18. Summary of UVP and OCP Protection

Protection Type	Protection Threshold	Protection Flag	Protection Action	DVID mask time	Protection Reset
Sum OCP for PS0	$I_{SUM\_OC,PS0}=K_{SOCP}\times VIMON_{ICCMAX}\times\frac{R_{INT.}}{DCR}\times\frac{1}{R_{IMON,EQ}}$	VREF=2V	PWM tri-state, VR_READY latched low	DVID+ 80us	VCC/ VRON Toggle
Sum OCP for non PS0	$I_{SUM\_OC,PS0}=\frac{1}{K}\times VIMON_{ICCMAX}\times\frac{R_{INT.}}{DCR}\times\frac{1}{R_{IMON,EQ}}$	VREF=2V			
UVP	VID-650mV	VREF=1.5V			

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-52L 6x6 package, the thermal resistance, θ_{JA}, is 26.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C − 25°C) / (26.5°C/W) = 3.77W for a WQFN-52L 6x6 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 26 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

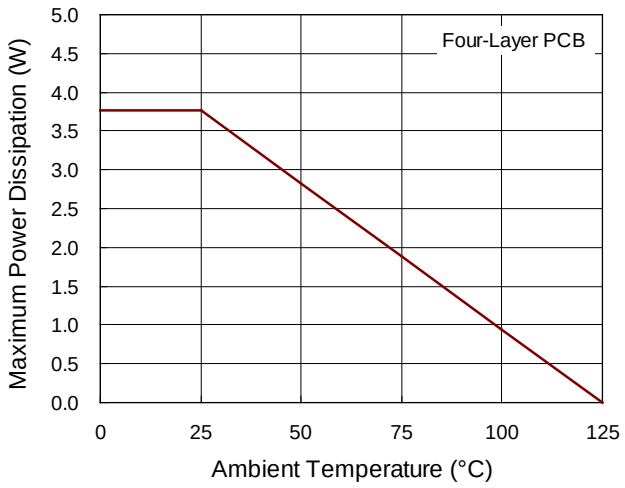
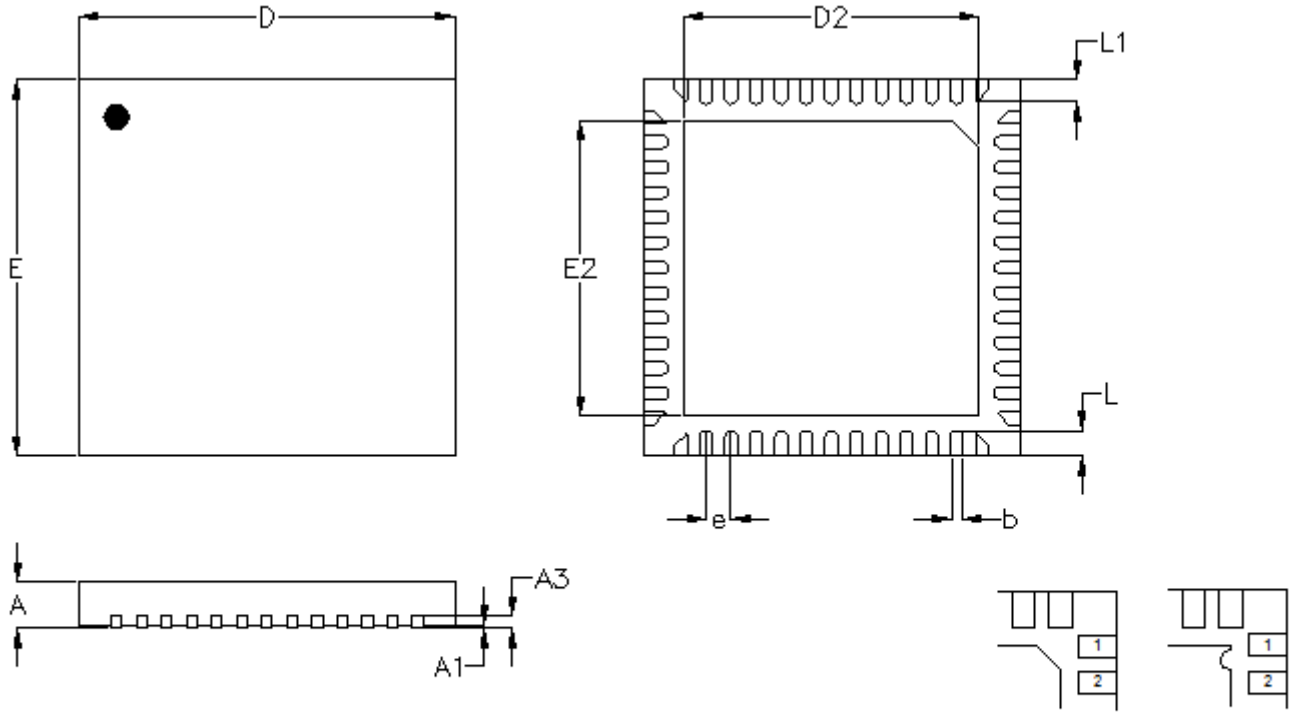


Figure 26. Derating Curve of Maximum Power Dissipation

Outline Dimension



DETAIL A

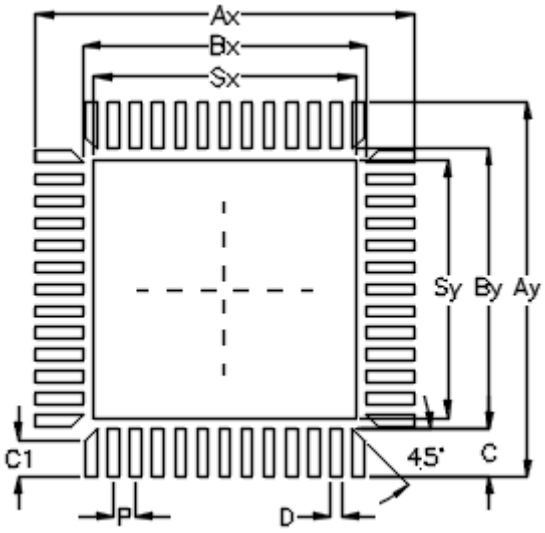
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	5.950	6.050	0.234	0.238
D2	4.650	4.750	0.183	0.187
E	5.950	6.050	0.234	0.238
E2	4.650	4.750	0.183	0.187
e	0.400		0.016	
L	0.350	0.450	0.014	0.018
L1	0.300	0.400	0.012	0.016

W-Type 52L QFN 6x6 Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)										Tolerance
		P	Ax	Ay	Bx	By	C*52	C1*8	D	Sx	Sy	
V/W/U/XQFN6*6-52	52	0.40	6.80	6.80	5.10	5.10	0.85	0.65	0.20	4.70	4.70	±0.05

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Datasheet Revision History

Version	Date	Item	Description
P00	2020/4/8		First Edition
P01	2020/8/3	Pin Configuration Functional Pin Description	Modify
P02	2020/11/23	General Description Features Simplified Application Circuit Functional Pin Description Functional Block Diagram Operation Absolute Maximum Ratings Electrical Characteristics Typical Application Circuit Application Information	Modify
P03	2021/2/1	Simplified Application Circuit Functional Pin Description Application Information	Modify