Cost-Effective, 1.8A Sink/Source Bus Termination Regulator

General Description

The RT9045 is a simple, cost-effective and high-speed linear regulator designed to generate termination voltage in Double Data Rate (DDR) memory system to comply with the devices requirements. The regulator is capable of actively sinking or sourcing up to 1.8A while regulating an output voltage to within 20mV. The output termination voltage can be tightly regulated to track V_{DDQ} / 2 by two external voltage divider resistors or the desired output voltage can be programmed by externally forcing the REFEN pin voltage.

The RT9045 also incorporates a high-speed differential amplifier to provide ultra-fast response in line/load transient. Other features include extremely low initial offset voltage, excellent load regulation, current limiting in bi-directions and on-chip thermal shutdown protection.

Ordering Information

RT9045□□

- Package Type
  SP : SOP-8 (Exposed Pad-Option 2)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
  Z : ECO (Ecological Element with Halogen Free and Pb free)

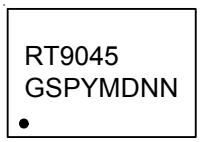
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

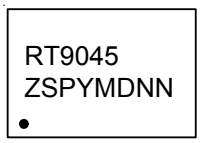
Marking Information

RT9045GSP



RT9045GSP : Product Number
YMDNN : Date Code

RT9045ZSP



RT9045ZSP : Product Number
YMDNN : Date Code

Features

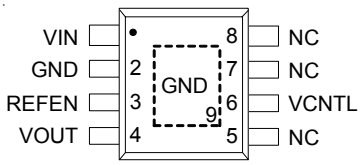
- **Ideal for DDR V_{TT} Applications**
- **Sink and Source Current :**
  - **DDRII 1.8A Sink/Source @ V_{IN} = 1.8V**
  - **DDRIII 1.5A Sink/Source @ V_{IN} = 1.5V**
  - **LPDDRIII 1.2A Sink/Source @ V_{IN} = 1.35V**
  - **DDRIV 1.2A Sink/Source @ V_{IN} = 1.2V**
- **Integrated Power MOSFETs**
- **Generate Termination Voltage for DDR Memory Interfaces**
- **Stable with Output Ceramic Capacitor**
- **High Accuracy Output Voltage at Full-Load**
- **Output Adjustment by Two External Resistors**
- **Low External Component Count**
- **Shutdown for Suspend to RAM (STR) Functionality with High Impedance Output**
- **Current Limiting Protection**
- **On-Chip Thermal Protection**
- **RoHS Compliant**

Applications

- Desktop PCs, Notebooks, and Workstations
- Graphics Card Memory Termination
- Set Top Boxes, Digital TVs, Printers
- Embedded Systems
- Active Termination Buses
- DDR Memory Systems

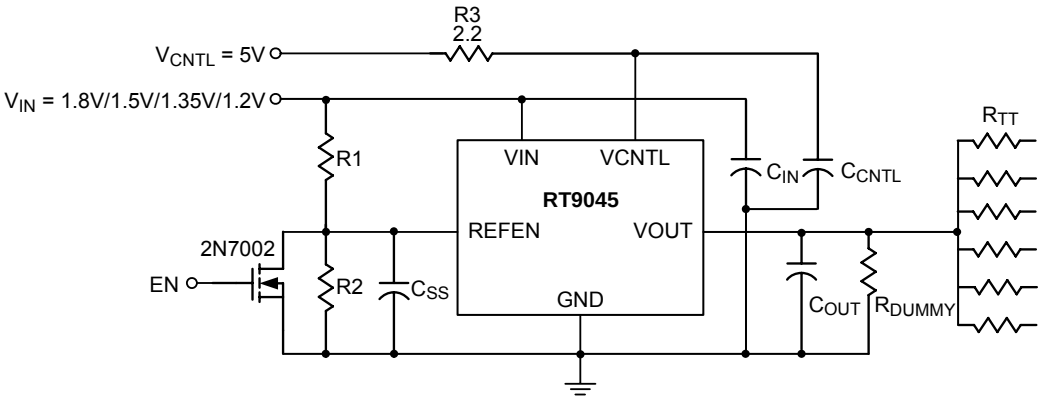
Pin Configurations

(TOP VIEW)



SOP-8 (Exposed Pad)

Typical Application Circuit



$R_1 = R_2 = 100k\Omega$, $R_{TT} = 50\Omega$ / 33Ω / 25Ω

$R_{DUMMY} = 1k\Omega$ as for V_{OUT} discharge when V_{IN} is not presented but V_{CNTL} is presented

$C_{OUT} = 10\mu F$ (Ceramic) under the worst case testing condition

$C_{IN} = 10\mu F$, $C_{CNTL} = 1\mu F$, $C_{SS} = 1nF$ to $0.1\mu F$

Test Circuit

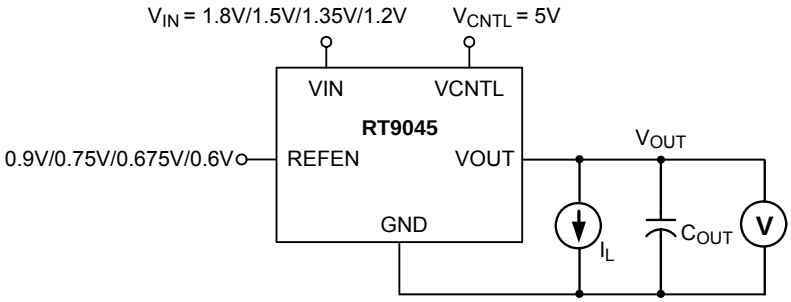


Figure 1. Output Voltage Tolerance, ΔV_{LOAD}

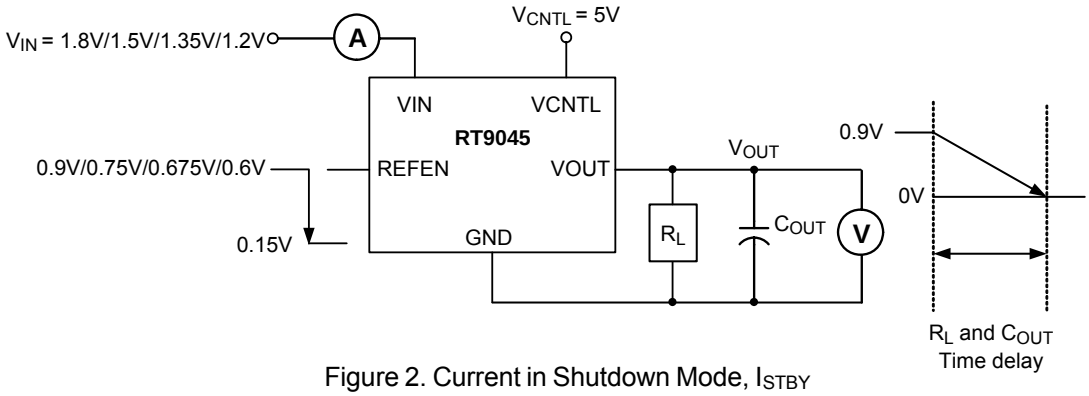


Figure 2. Current in Shutdown Mode, I_{STBY}

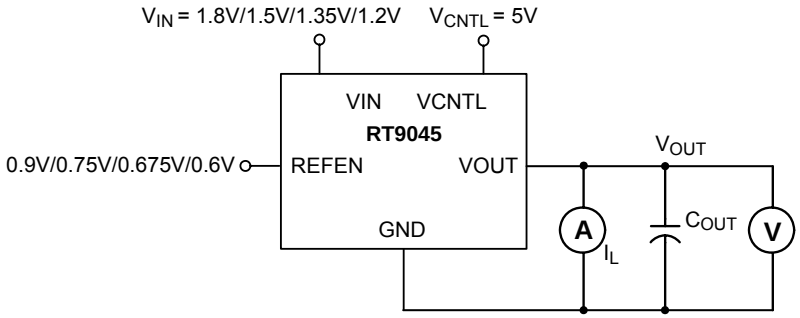


Figure 3. Current Limit for High Side, I_{LIM}

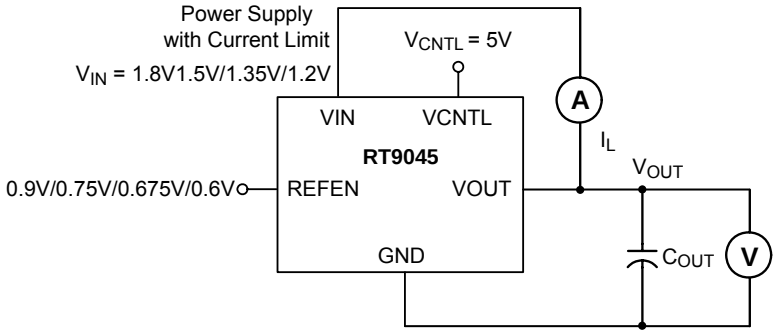


Figure 4. Current Limit for Low Side, I_{LIM}

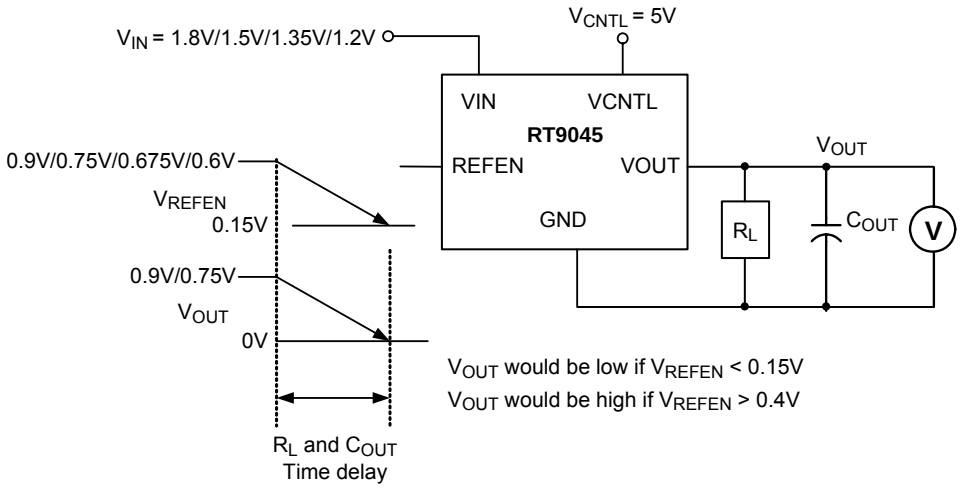
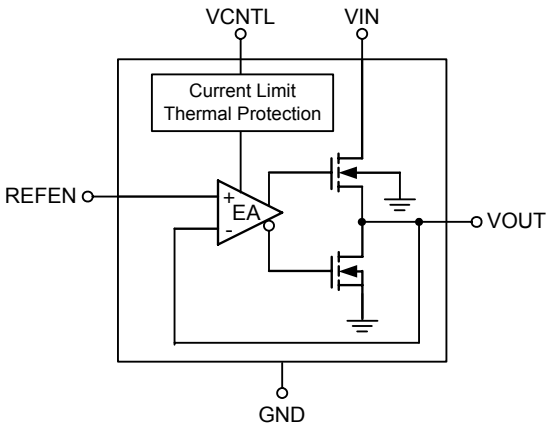


Figure 5. REFEN Pin Shutdown Threshold, V_{IH} & V_{IL}

Function Block Diagram



Functional Pin Description

VIN

Input voltage which supplies current to the output pin. Connect this pin to a well-decoupled supply voltage. To prevent the input rail from dropping during large load transient, a large, low ESR capacitor is recommended to use. The capacitor should be placed as close as possible to the VIN pin.

GND (Exposed Pad)

Common Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

VCNTL

VCNTL supplies the internal control circuitry and provides the drive voltage. The driving capability of output current is proportioned to the VCNTL. Connect this pin to 5V bias supply to handle large output current with at least 1μF capacitor from this pin to GND. An important note is that VIN should be kept lower or equal to VCNTL.

REFEN

Reference voltage input and active low shutdown control pin. Two resistors dividing down the VIN voltage on this pin to create the regulated output voltage. Pulling this pin to ground turns off the device by an open-drain, such as 2N7002, signal N-MOSFET.

VOUT

Regulator output. VOUT is regulated to REFEN voltage that is used to terminate the bus resistors. It is capable of sinking and sourcing current while regulating the output rail. To maintain adequate large signal transient response, typical value of 10μF ceramic capacitors are recommended to reduce the effects of current transients on VOUT.

Absolute Maximum Ratings (Note 1)

- Input Voltage, V_{IN} ---------- –0.3V to 6V
- Control Voltage, V_{CNTL} ---------- –0.3V to 6V
- Reference Input Voltage, V_{REFEN} ---------- –0.3V to 6V
- Output Voltage, V_{OUT} ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  SOP-8 (Exposed Pad) ---------- 1.163W
- Package Thermal Resistance (Note 2)
  SOP-8 (Exposed Pad), θ_{JA} ---------- 86°C/W
  SOP-8 (Exposed Pad), θ_{JC} ---------- 15°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Input Voltage, V_{IN} ---------- 1V to 5.5V
- Control Voltage, V_{CNTL} ---------- 5V ± 5%
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 1.8V / 1.5V, V_{CNTL} = 5V, V_{REFEN} = 0.9V / 0.75V, C_{OUT} = 10µF (Ceramic), T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input							
VCNTL Operation Current		I_{CNTL}	I_{OUT} = 0A	--	0.7	2.5	mA
VCNTL Power on Reset		V_{POR}	V_{CNTL} Rising	--	3.6	--	V
Standby Current (Note 5)		I_{STBY}	V_{REFEN} < 0.2V (Shutdown), R_{LOAD} = 180Ω	--	20	90	µA
Output							
Output Offset Voltage (Note 6)		V_{OS}	I_{OUT} = 0A	–13	--	13	mV
Load Regulation (Note 7)		ΔV_{LOAD}	V_{IN} = 1.8V, V_{REFEN} = 0.9V, I_{OUT} = ±1.8A	–13	--	13	mV
			V_{IN} = 1.5V, V_{REFEN} = 0.75V, I_{OUT} = ±1.5A				
			V_{IN} = 1.35V, V_{REFEN} = 0.675V, I_{OUT} = ±1.2A				
			V_{IN} = 1.2V, V_{REFEN} = 0.6V, I_{OUT} = ±1.2A				
Protection							
Current Limit	Source	$I_{LIMITsr}$	V_{IN} = 1.8V, V_{REFEN} = 0.9V	1.8	--	3.5	A
			V_{IN} = 1.5V, V_{REFEN} = 0.75V				
	Sink	$I_{LIMITsk}$	V_{IN} = 1.8V, V_{REFEN} = 0.9V	1.8	--	3.5	A
			V_{IN} = 1.5V, V_{REFEN} = 0.75V				

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Short Circuit Current		V_{IN} = 1.8V / 1.5V / 1.35V / 1.2V, V_{OUT} < 0.2V	--	1.5	--	A
Thermal Shutdown Temperature	T_{SD}	V_{CNTL} = 5V	125	170	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}	V_{CNTL} = 5V	--	35	--	°C
Short Circuit Current		V_{IN} = 1.8V / 1.5V / 1.35V / 1.2V, V_{OUT} < 0.2V	--	1.5	--	A
Thermal Shutdown Temperature	T_{SD}	V_{CNTL} = 5V	125	170	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}	V_{CNTL} = 5V	--	35	--	°C
REFEN Shutdown						
Shutdown Threshold	V_{IH}	Enable	0.4	--	--	V
	V_{IL}	Shutdown	--	--	0.15	

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective thermal conductivity test board (4 Layers, 2S2P) of JEDEC 51-7 thermal measurement standard. The case point of θ_{JC} is on the exposed pad for package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

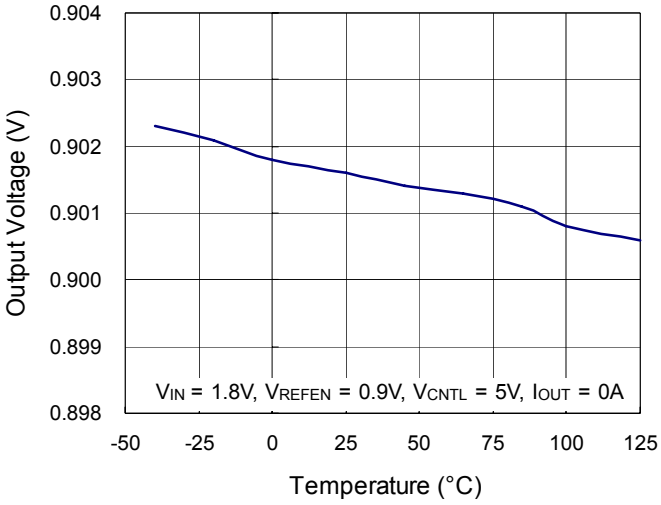
Note 5. Standby current is the input current drawn by a regulator when the output voltage is disabled by a shutdown signal on REFEN pin (V_{IL} < 0.15V). It is measured with V_{IN} = 1.8V, V_{CNTL} = 5V.

Note 6. V_{OS} offset is the voltage measurement defined as V_{OUT} subtracted from V_{REFEN}.

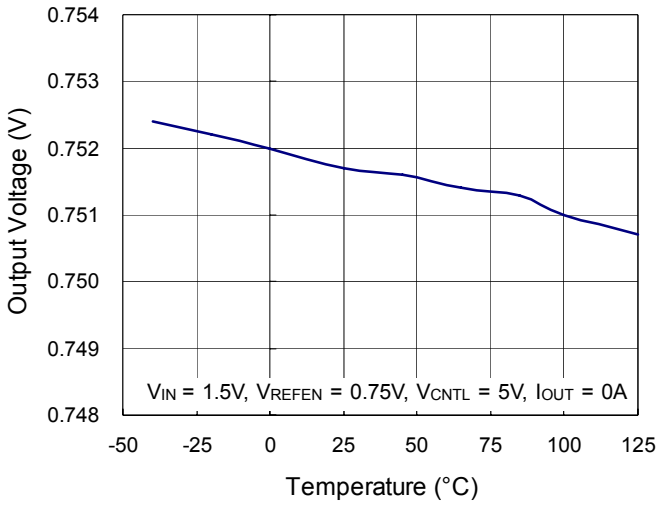
Note 7. Regulation is measured at constant junction temperature by using a 5ms current pulse. Devices are tested for load regulation in the load range from 0A to 1.8A peak.

Typical Operating Characteristics

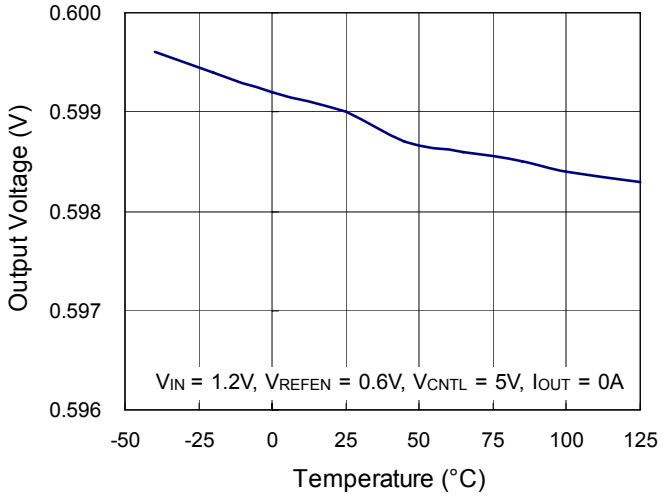
DDR II Output Voltage vs. Temperature



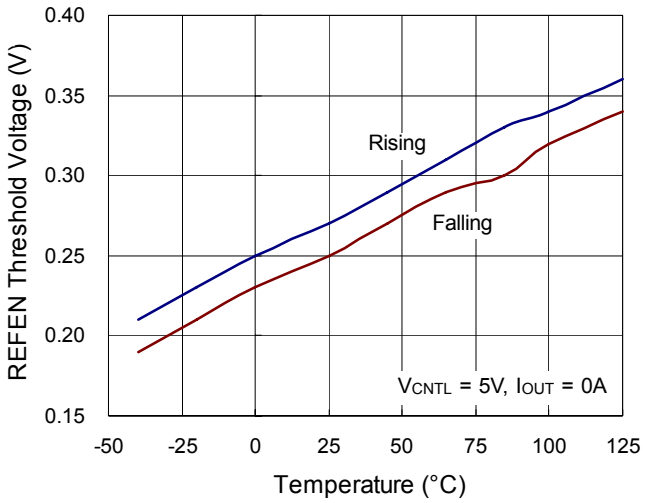
DDR III Output Voltage vs. Temperature



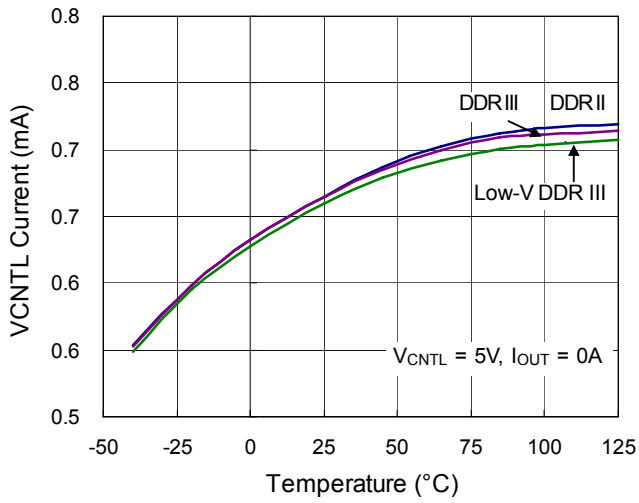
Low-V DDR III Output Voltage vs. Temperature



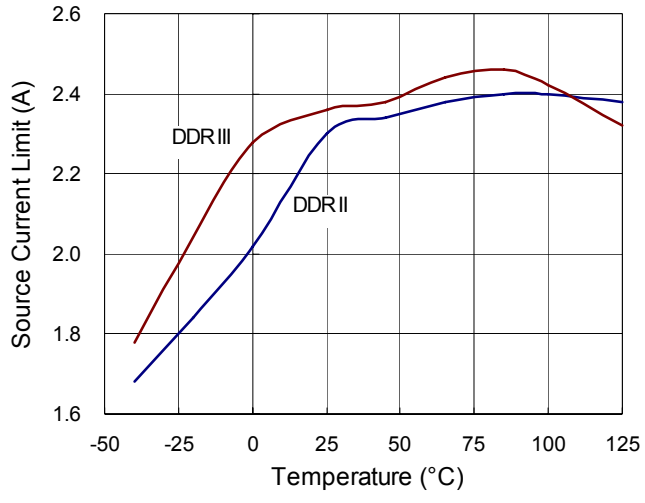
REFEN Threshold Voltage vs. Temperature



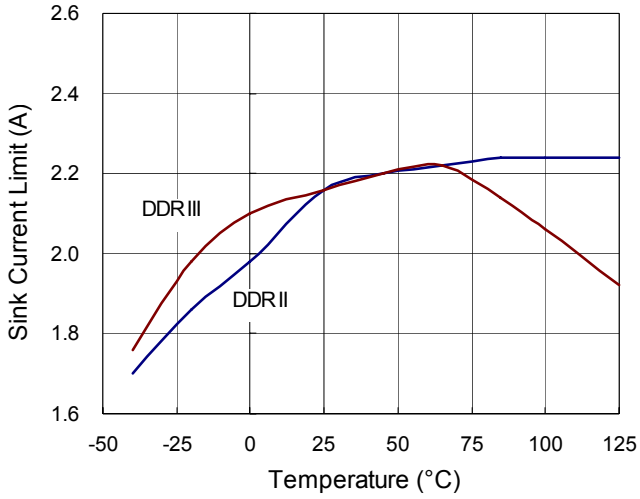
VCNTL Current vs. Temperature



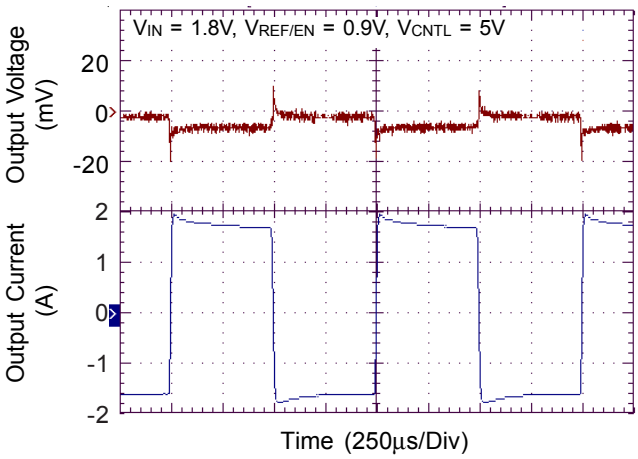
Source Current Limit vs. Temperature



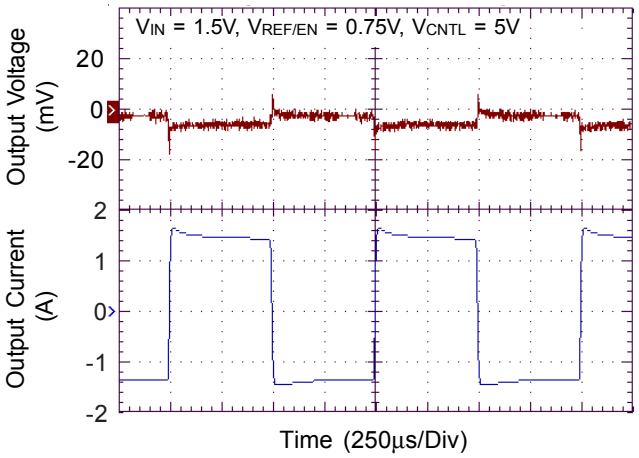
Sink Current Limit vs. Temperature



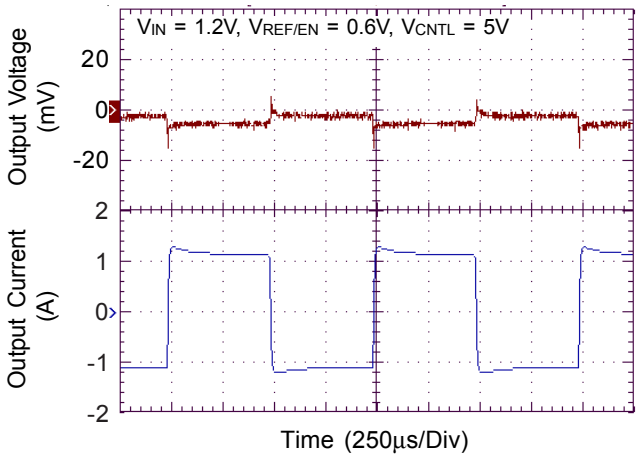
0.9V_{TT} @ 1.8A Transient Response



0.75V_{TT} @ 1.5A Transient Response



0.6V_{TT} @ 1.2A Transient Response



Application Information

Output Voltage Setting

The RT9045 is a high-speed linear regulator designed to generate termination voltage in Double Data Rate (DDR) memory system. Besides, the RT9045 could also serves as a general linear regulator. The RT9045 accepts an external reference voltage at the REFEN pin and provides an output voltage regulated to this reference voltage level as shown in Figure 6, where

$V_{OUT} = V_{IN} \times R2 / (R1 + R2)$

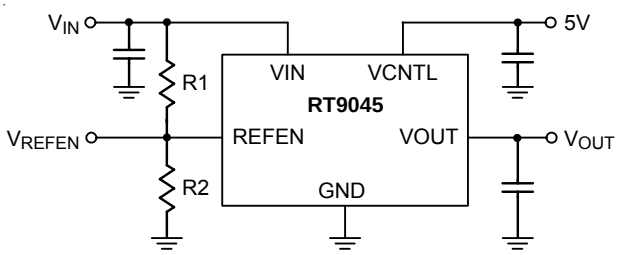


Figure 6. RT9045 Operating as a Linear Regulator

General Regulator

Like other linear regulator, dropout voltage and thermal issue should be specially considered. Figure 7 shows the $R_{DS(ON)}$ vs. Temperature curve of RT9045. The minimum dropout voltage could be obtained by the product of $R_{DS(ON)}$ and output current. For thermal consideration, please refer to the relative section.

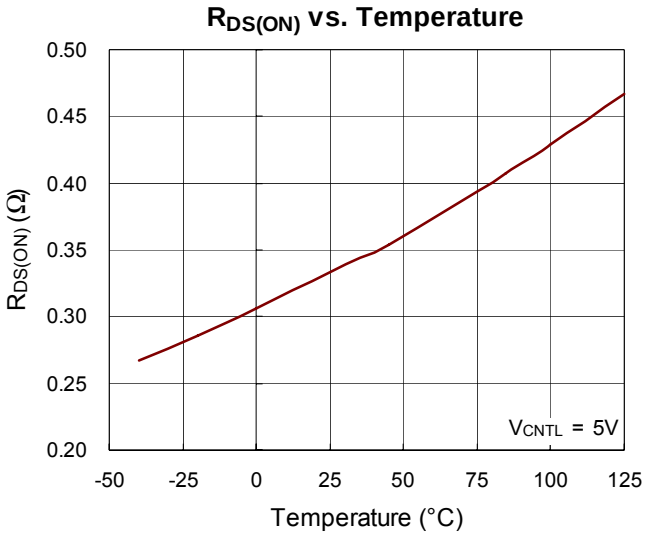


Figure 7. $R_{DS(ON)}$ vs. Temperature

Shutdown Control

Refer to the "Typical Application Circuit". Make sure the current sinking capability of pull-down N-MOSFET is enough for the chosen voltage divider to pull-down the voltage at REFEN pin below 0.15V to shutdown the device.

In addition, the capacitor C_{SS} and voltage divider form the low-pass filter.

Soft-Start

The RT9045 builds in an internal soft-start circuit to prevent inrush current during start-up. The internal soft-start time depends on REFEN voltage. For DDRIII application (REFEN = 0.75V), soft-start time is around 100μs.

Current Limit & Short Circuit Protection

The RT9045 implements the current limit and output short protection circuit against the unexpected applications. The current limit circuit monitors and controls the pass transistor's gate voltage, providing the load current up to at least 1.8A. If the load current exceeds the current limit trip point, RT9045 will soon reduce the load current to around 1.5A constantly, refer to Figure 8.

If the output voltage is abruptly pulled down to less than 0.2V, the short circuit protection is triggered and then maintains the load current at 1.5A. It prevents RT9045 from being damaged in case an output short to ground event occurs.

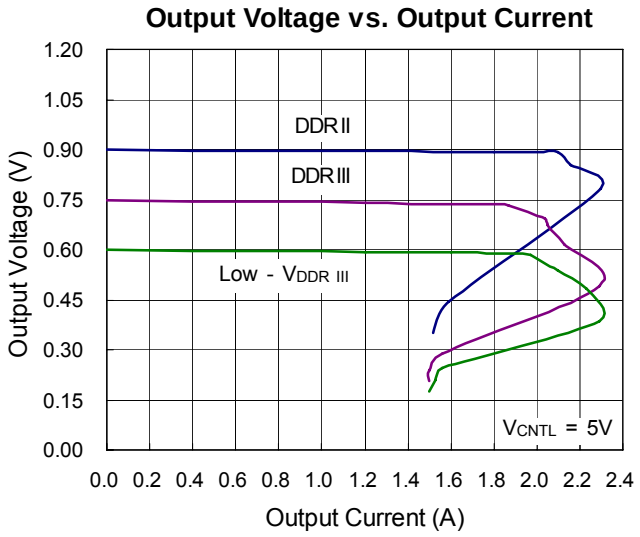


Figure 8. Output Voltage vs. Output Current

Input Capacitor and Layout Consideration

Place the input bypass capacitor as close as possible to the RT9045. A low ESR capacitor larger than 20μF is recommended for the input capacitor. Use short and wide traces to minimize parasitic resistance and inductance. Inappropriate layout may result in large parasitic inductance and cause undesired oscillation between the RT9045 and the proceeding power converter.

Thermal Consideration

RT9045 regulators have internal thermal limiting circuitry designed to protect the device during overload conditions. For continued operation, do not exceed absolute maximum operation junction temperature of 125°C. The power dissipation definition in device is :

$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

$T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance. The junction to ambient thermal resistance for SOP-8 (Exposed Pad) package is 86°C/W on the standard JEDEC 51-7 (4 layers, 2S2P) thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)} = (125°C - 25°C) / (86°C/W) = 1.163W$

Figure 9 shows the package sectional drawing of SOP-8 (Exposed Pad). Every package has several thermal dissipation paths. As shown in Figure 10, the thermal resistance equivalent circuit of SOP-8 (Exposed Pad). The path 2 is the main path due to these materials thermal conductivity. We define the exposed pad is the case point of the path 2.

The thermal resistance θ_{JA} of SOP-8 (Exposed Pad) is determined by the package design and the PCB design. However, the package design has been decided. If possible, it's useful to increase thermal performance by the PCB design. The thermal resistance can be decreased by adding copper under the SOP-8 (Exposed Pad) package.

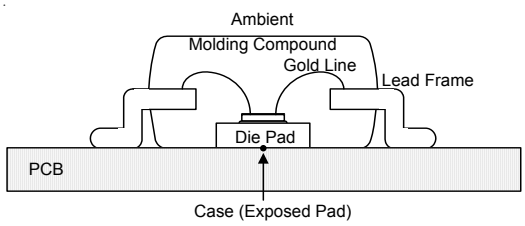


Figure 9. SOP-8 (Exposed Pad) Package Sectional Drawing

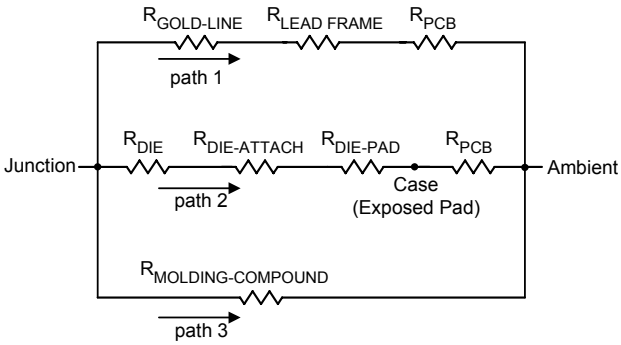


Figure 10. Thermal Resistance Equivalent Circuit

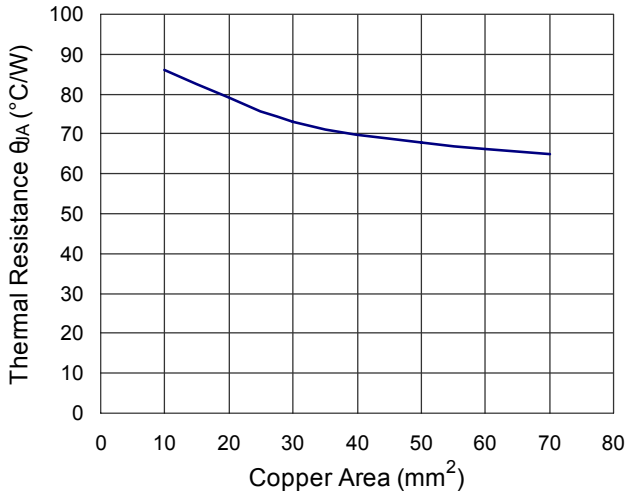


Figure 11. Relation Between Thermal Resistance θ_{JA} and Copper Area

Figure 11 shows the relation between thermal resistance θ_{JA} and copper area on a standard JEDEC 51-7 (4 layers, 2S2P) thermal test board at T_A = 25°C. We have to consider the copper couldn't stretch infinitely and avoid the tin overflow. We use the "Dog-Bone" copper patterns on the top layer as shown in Figure 12.

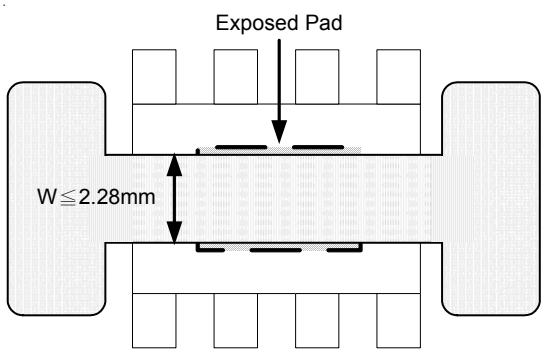
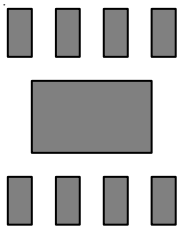
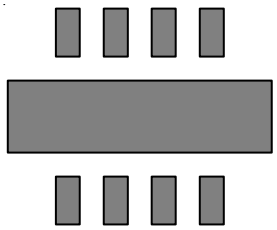


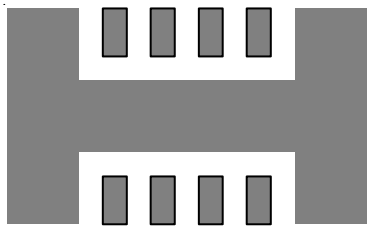
Figure 12. Dog-Bone Layout



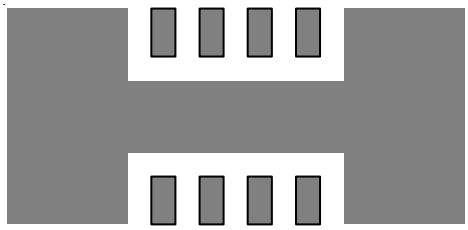
(a) Copper Area = 10mm^2, θ_{JA} = 86°C/W



(b) Copper Area = 30mm^2, θ_{JA} = 73°C/W



(c) Copper Area = 50mm^2, θ_{JA} = 68°C/W



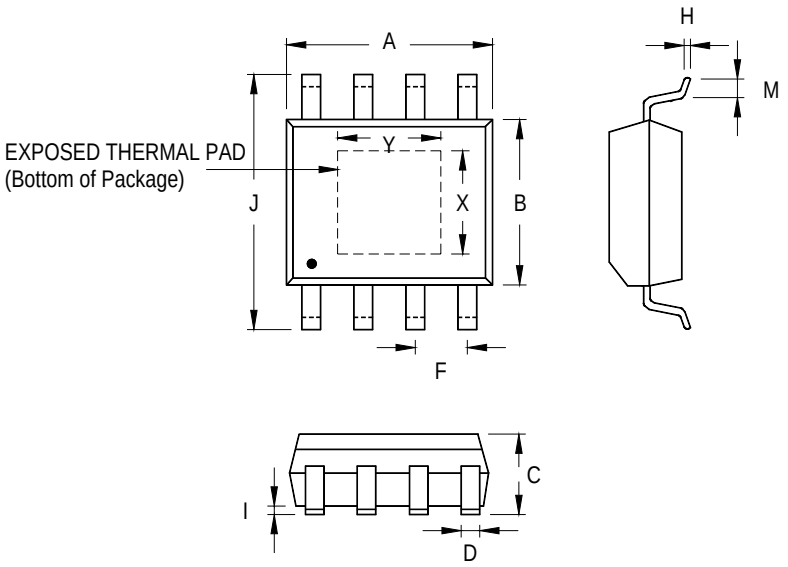
(d) Copper Area = 70mm^2, θ_{JA} = 65°C/W

Figure 13. Thermal Resistance vs. Copper Area Layout

Thermal Design

As shown in Figure 13, the amount of copper area to which the SOP-8 (Exposed Pad) is mounted affects thermal performance. When mounted to the standard SOP-8 (Exposed Pad) pad of 2 oz. copper (Figure 13.a), θ_{JA} is 86°C/W. Adding copper area of pad under the SOP-8 (Exposed Pad) (Figure 13.b) reduces the θ_{JA} to 73°C/W. Even further, increasing the copper area of pad to 70mm^2 (Figure 13.d) reduces the θ_{JA} to 65°C/W.

Outline Dimension



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.700	5.100	0.185	0.200
B		3.800	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.790	6.200	0.228	0.244
M		0.400	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.513	0.083	0.099
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

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