TPS22968x Dual Channel, Ultra-Low Resistance Load Switch

1 Features

- Integrated Dual Channel Load Switch
- Input Voltage Range: 0.8 V to 5.5 V
- VBIAS Voltage Range: 2.5 V to 5.5 V
  - Ideal for 1S Battery Configuration
- Ultra-Low R_{ON} Resistance
  - R_{ON} = 27 mΩ at V_{IN} = 5 V (V_{BIAS} = 5 V)
  - R_{ON} = 25 mΩ at V_{IN} = 3.3 V (V_{BIAS} = 5 V)
  - R_{ON} = 25 mΩ at V_{IN} = 1.8 V (V_{BIAS} = 5 V)
- 4-A Maximum Continuous Switch Current per Channel
- Low Quiescent Current
  - 55 µA at V_{BIAS} = 5 V (Both Channels)
  - 55 µA at V_{BIAS} = 5 V (Single Channel)
- Low Control Input Threshold Enables Use of 1.2-V/1.8-V/2.5-V/3.3-V Logic
- Configurable Rise Time(1)
- Quick Output Discharge (QOD)(2) (TPS22968 Only)
- SON 14-Pin Package With Thermal Pad
- ESD Performance Tested per JEDEC Standard
  - 2-kV HBM and 1-kV CDM
- Latch-Up Performance Exceeds 100 mA per JESD 78, Class II
- GPIO Enable – Active High
- TPS22968N: Product Preview Only

(1) See Application Information section for CT value vs. rise time

(2) This feature discharges output of the switch to GND through a 270-Ω resistor, preventing the output from floating.

2 Applications

- Ultrabook™
- Notebooks/Netbooks
- Tablets
- Consumer Electronics
- Set-Top Boxes
- Telecom Systems

3 Description

The TPS22968x is a small, ultra-low R_{ON}, dual-channel load switch with controlled turn on. The device contains two N-channel MOSFETs that can operate over an input voltage range of 0.8 to 5.5 V and can support a maximum continuous current of 4 A per channel. Each switch is independently controlled by an on/off input (ON1 and ON2), which is capable of interfacing directly with low-voltage control signals. In TPS22968, a 270-Ω on-chip load resistor is added for output quick discharge when switch is turned off.

The TPS22968x is available in a small, space-saving package (DPU) with integrated thermal pad allowing for high power dissipation. The device is characterized for operation over the free-air temperature range of –40 to +105°C.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22968x	WSON (14)	3.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic

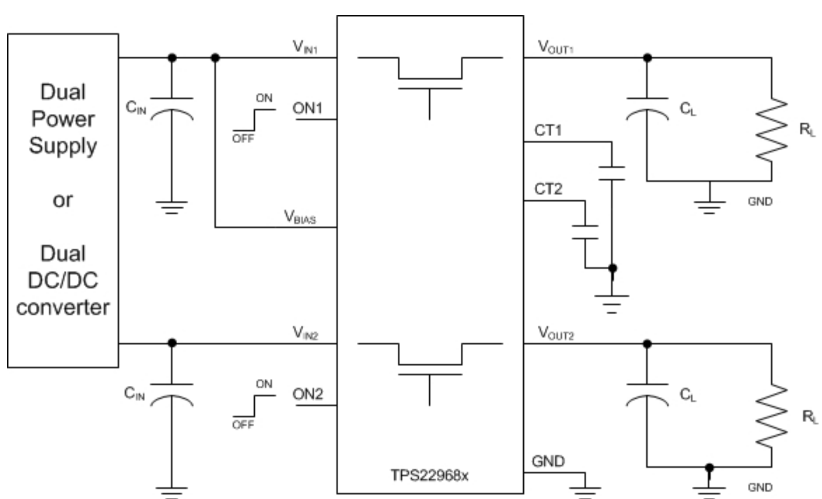


Table of Contents

4 Revision History

Changes from Revision C (October 2015) to Revision D — **Page**

- Made Changes to Thermal Considerations 22

Changes from Revision B (June 2015) to Revision C — **Page**

- Updated information for TPS22968N release. 1
- Updated “TEST CONDITIONS” for RON. 5
- Updated “TEST CONDITIONS” for RON. 6

Changes from Revision A (July 2014) to Revision B — **Page**

- Added temperature operating ranges to Electrical Characteristics (V_{BIAS} = 5 V) table. 5
- Added temperature operating ranges to Electrical Characteristics (V_{BIAS} = 2.5 V) table. 6
- Updated Typical Characteristics graphs. 8

Changes from Original (January 2014) to Revision A — **Page**

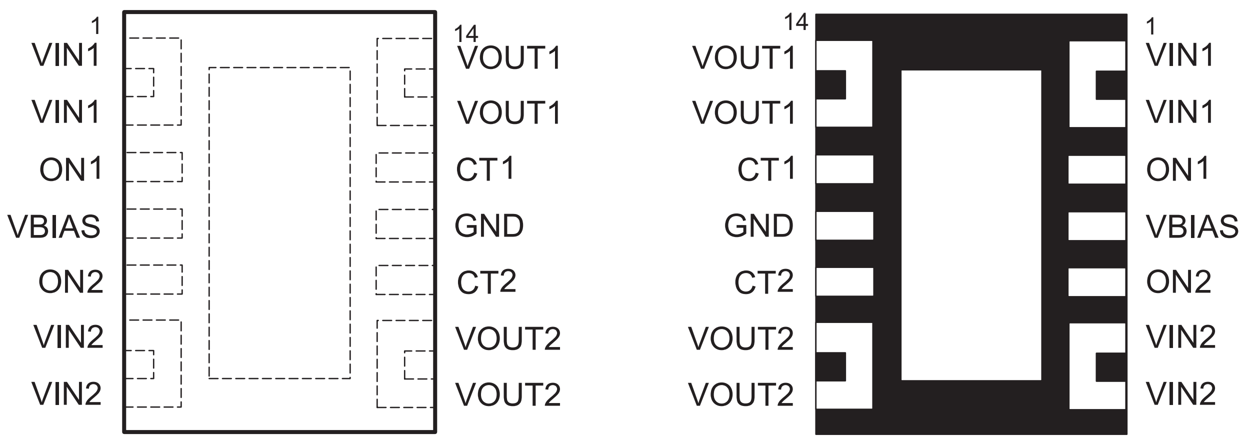
- Added *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

5 Device Comparison Table

DEVICE	Ron (typ) at VIN = 3.3 V, VBIAS = 5.0 V	QUICK OUTPUT DISCHARGE	MAXIMUM OUTPUT CURRENT	ENABLE
TPS22968	25 mΩ	Yes	4 A	Active High
TPS22968N	25 mΩ	No	4 A	Active High

6 Pin Configuration and Functions

DPU PACKAGE
14-Pin WSON
Top and Bottom View



Top View **Bottom View**

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VIN1	1	I	Switch 1 input. Bypass this input with a ceramic capacitor to GND.
	2		
ON1	3	I	Active-high switch 1 control input. Do not leave floating.
VBIAS	4	I	Bias voltage. Power supply to the device. Recommended voltage range for this pin is 2.5 V to 5.5 V. See *VIN and VBIAS Voltage Range* .
ON2	5	I	Active-high switch 2 control input. Do not leave floating.
VIN2	6	I	Switch 2 input. Bypass this input with a ceramic capacitor to GND.
	7		
VOUT2	8	O	Switch 2 output
	9		
CT2	10	O	Switch 2 slew rate control. Can be left floating.
GND	11	—	Ground
CT1	12	O	Switch 1 slew rate control. Can be left floating.
VOUT1	13	O	Switch 2 output
	14		
Thermal Pad	15	—	Thermal pad (exposed center pad) to alleviate thermal stress. Tie to GND. See *Application Information* for layout guidelines.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature (unless otherwise noted)[1]

		MIN	MAX	UNIT [2]
$V_{IN1,2}$	Input voltage	–0.3	6	V
V_{BIAS}	Bias voltage	–0.3	6	V
$V_{OUT1,2}$	Output voltage	–0.3	6	V
$V_{ON1,2}$	ON voltage	–0.3	6	V
I_{MAX}	Maximum continuous switch current per channel, T_A = 30 °C		4	A
I_{PLS}	Maximum pulsed switch current, pulse < 300 µs, 2% duty cycle		6	A
T_J	Maximum junction temperature		125	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 [2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
$V_{IN1,2}$	Input voltage range		0.8	V_{BIAS}	V
V_{BIAS}	Bias voltage range		2.5	5.5	V
$V_{ON1,2}$	ON voltage range		0	5.5	V
$V_{OUT1,2}$	Output voltage range			V_{IN}	V
$V_{IH,\ ON1,2}$	High-level input voltage, ON1,2	V_{BIAS} = 2.5 V to 5.5 V	1.2	5.5	V
$V_{IL,\ ON1,2}$	Low-level input voltage, ON1,2	V_{BIAS} = 2.5 V to 5.5 V	0	0.5	V
$C_{IN1,2}$	Input capacitor		1 [1]		µF
T_A	Operating free-air temperature [2]		–40	105	°C

(1) Refer to the *Application Information* section.
(2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(max)}$], the maximum power dissipation of the device in the application [$P_{D(max)}$], and the junction-to-ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A(max)} = T_{J(max)} – (R_{\theta JA} \times P_{D(max)})$.

7.4 Thermal Information

THERMAL METRIC [1] [2]		TPS22968	UNIT
		DPU (WSON)	
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	62.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the *TI PCB Thermal Calculator*.

Thermal Information (continued)

THERMAL METRIC [(1)] [(2)]		TPS22968 DPU (WSON) 14 PINS	UNIT
ψ_{JB}	Junction-to-board characterization parameter	23.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.0	°C/W

7.5 Electrical Characteristics (V_{BIAS} = 5 V)

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature –40°C ≤ T_A ≤ +105°C (full) and V_{BIAS} = 5 V. Typical values are for T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{Q,\ VBIAS}$	V_{BIAS} quiescent current (both channels)	$I_{OUT1} = I_{OUT2} = 0$, $V_{IN1,2} = V_{ON1,2} = V_{BIAS}$ = 5 V		–40°C to +105°C		55	70	µA
	V_{BIAS} quiescent current (single channel)	$I_{OUT1} = I_{OUT2} = 0$, V_{ON2} = 0 V, $V_{IN1,2} = V_{ON1} = V_{BIAS}$ = 5.0 V		–40°C to +105°C		55	68	µA
$I_{SD,\ VBIAS}$	V_{BIAS} shutdown current	$V_{ON1,2}$ = 0 V, $V_{OUT1,2}$ = 0 V		–40°C to +105°C		1	2	µA
$I_{SD,\ VIN1,2}$	$V_{IN1,2}$ shutdown current (per channel)	$V_{ON1,2}$ = 0 V, $V_{OUT1,2}$ = 0 V	$V_{IN1,2}$ = 5 V	–40°C to +85°C		0.5	8	µA
				–40°C to +105°C			10	
			$V_{IN1,2}$ = 3.3 V	–40°C to +85°C		0.1	3	
				–40°C to +105°C			4	
			$V_{IN1,2}$ = 1.8 V	–40°C to +85°C		0.07	2	
				–40°C to +105°C			3	
			$V_{IN1,2}$ = 1.2 V	–40°C to +85°C		0.05	1	
				–40°C to +105°C			2	
			$V_{IN1,2}$ = 0.8 V	–40°C to +85°C		0.04	1	
				–40°C to +105°C			2	
$I_{ON1,2}$	ON pin input leakage current	V_{ON} = 5.5 V		–40°C to +105°C			0.1	µA
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance	I_{OUT} = –200 mA, V_{BIAS} = 5 V, $V_{ON1,2}$ = 5 V	V_{IN} = 5 V	25°C		27	36	mΩ
				–40°C to +85°C			40	
				–40°C to +105°C			42	
			V_{IN} = 3.3 V	25°C		25	34	mΩ
				–40°C to +85°C			38	
				–40°C to +105°C			40	
			V_{IN} = 1.8 V	25°C		25	34	mΩ
				–40°C to +85°C			38	
				–40°C to +105°C			40	
			V_{IN} = 1.5 V	25°C		25	34	mΩ
				–40°C to +85°C			38	
				–40°C to +105°C			40	
			V_{IN} = 1.2 V	25°C		25	34	mΩ
				–40°C to +85°C			38	
				–40°C to +105°C			40	
			V_{IN} = 0.8 V	25°C		25	34	mΩ
				–40°C to +85°C			38	
				–40°C to +105°C			40	
R_{PD} [(1)]	Output pulldown resistance	V_{IN} = 5 V, V_{ON} = 0 V, I_{OUT} = 10 mA		–40°C to +105°C		270	320	Ω

(1) TPS22968 only.

7.6 Electrical Characteristics (V_{BIAS} = 2.5 V)

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature –40 °C ≤ T_A ≤ +105 °C (full) and V_{BIAS} = 2.5 V. Typical values are for T_A = 25°C (unless otherwise noted).

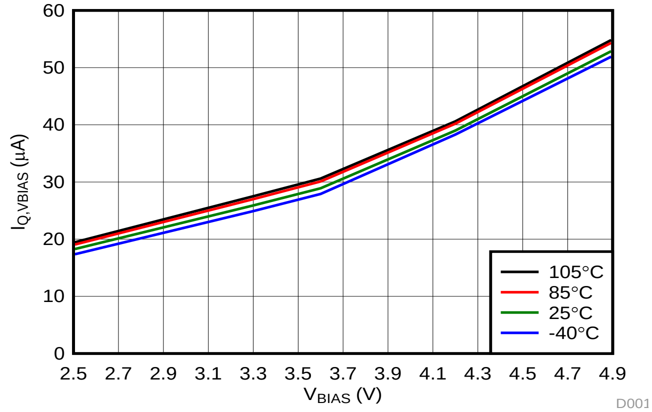
PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{Q, VBIAS}$	V_{BIAS} quiescent current (both channels)	I_{OUT1} = I_{OUT2} = 0, $V_{IN1,2}$ = $V_{ON1,2}$ = V_{BIAS} = 2.5 V		–40°C to +105°C		18	27	µA
	V_{BIAS} quiescent current (single channel)	I_{OUT1} = I_{OUT2} = 0, V_{ON2} = 0 V, $V_{IN1,2}$ = V_{ON1} = V_{BIAS} = 2.5 V		–40°C to +105°C		18	27	µA
$I_{SD, VBIAS}$	V_{BIAS} shutdown current	$V_{ON1,2}$ = 0 V, $V_{OUT1,2}$ = 0 V		–40°C to +105°C		0.5	2	µA
$I_{SD, VIN1,2}$	$V_{IN1,2}$ shutdown current (per channel)	$V_{ON1,2}$ = 0 V, $V_{OUT1,2}$ = 0 V	$V_{IN1,2}$ = 2.5 V	–40°C to +85°C		0.1	2	µA
				–40°C to +105°C			4	
			$V_{IN1,2}$ = 1.8 V	–40°C to +85°C		0.07	2	
				–40°C to +105°C			3	
			$V_{IN1,2}$ = 1.2 V	–40°C to +85°C		0.05	1	
				–40°C to +105°C			2	
			$V_{IN1,2}$ = 0.8 V	–40°C to +85°C		0.04	1	
				–40°C to +105°C			2	
$I_{ON1,2}$	ON pin input leakage current	V_{ON} = 5.5 V		–40°C to +85°C			0.1	µA
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance	I_{OUT} = –200 mA, V_{BIAS} = 2.5 V $V_{ON1,2}$ = 5 V	V_{IN} = 2.5 V	25°C		30	39	mΩ
				–40°C to +85°C			44	
				–40°C to +105°C			46	
			V_{IN} = 1.8 V	25°C		28	36	mΩ
				–40°C to +85°C			41	
				–40°C to +105°C			43	
			V_{IN} = 1.5 V	25°C		28	36	mΩ
				–40°C to +85°C			41	
				–40°C to +105°C			43	
			V_{IN} = 1.2 V	25°C		27	36	mΩ
				–40°C to +85°C			41	
				–40°C to +105°C			43	
			V_{IN} = 0.8 V	25°C		26	35	mΩ
				–40°C to +85°C			39	
				–40°C to +105°C			41	
R_{PD} [1]	Output pulldown resistance	V_{IN} = 2.5 V, V_{ON} = 0 V, I_{OUT} = 10 mA		–40°C to +105°C		270	320	Ω

(1) TPS22968 only.

7.7 Switching Characteristics

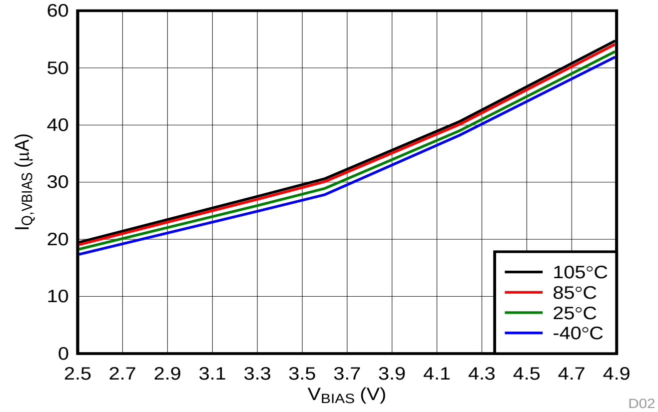
PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN} = V_{ON} = V_{BIAS} = 5 V, T_A = 25 °C (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		1128		µs
t_{OFF}	Turn-off time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		5		µs
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		1387		µs
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		2		µs
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		455		µs
V_{IN} = 0.8 V, V_{ON} = V_{BIAS} = 5 V, T_A = 25 ºC (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		508		µs
t_{OFF}	Turn-off time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		33		µs
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		273		µs
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		2		µs
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		377		µs
V_{IN} = 2.5 V, V_{ON} = 5 V, V_{BIAS} = 2.5V, T_A = 25 ºC (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		1718		µs
t_{OFF}	Turn-off time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		7		µs
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		1701		µs
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		2		µs
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		859		µs
V_{IN} = 0.8 V, V_{ON} = 5 V, V_{BIAS} = 2.5 V, T_A = 25 ºC (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		1117		µs
t_{OFF}	Turn-off time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		30		µs
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		651		µs
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		2		µs
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		775		µs

7.8 Typical Characteristics



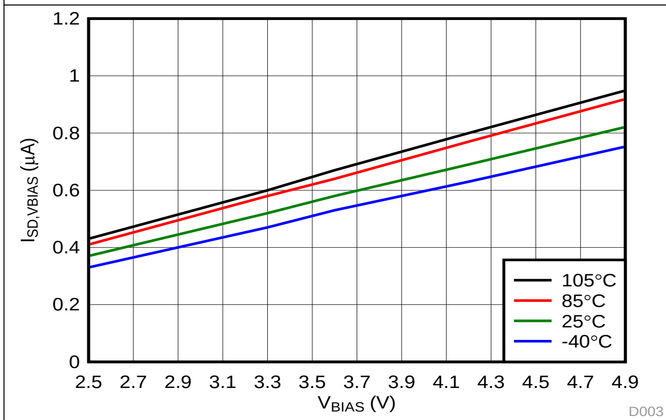
$V_{IN1} = V_{IN2} = V_{BIAS}$ V_{OUT} = Open
$V_{ON1} = V_{ON2}$ = 5 V

Figure 1. V_{BIAS} vs Quiescent Current (Both Channels)



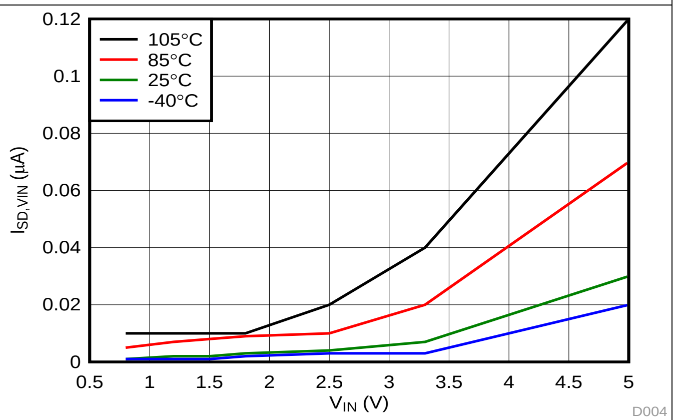
$V_{IN1} = V_{IN2} = V_{BIAS}$ V_{ON2} = 0 V
V_{ON1} = 5 V V_{OUT} = Open

Figure 2. V_{BIAS} vs Quiescent Current (Single Channel)



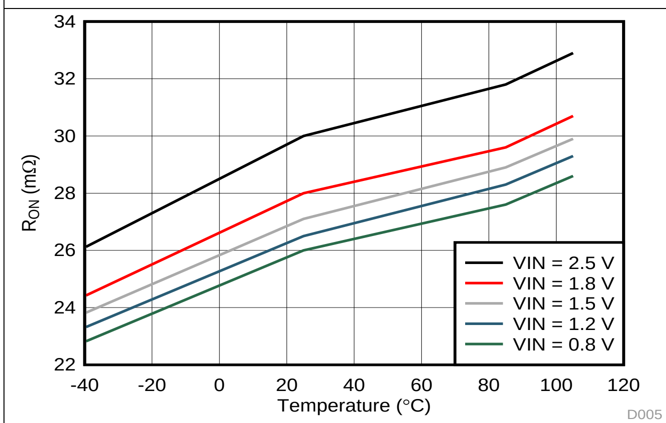
$V_{IN1} = V_{IN2} = V_{BIAS}$ V_{OUT} = 0 V
$V_{ON1} = V_{ON2}$ = 0 V

Figure 3. V_{BIAS} vs Shutdown Current (Both Channels)



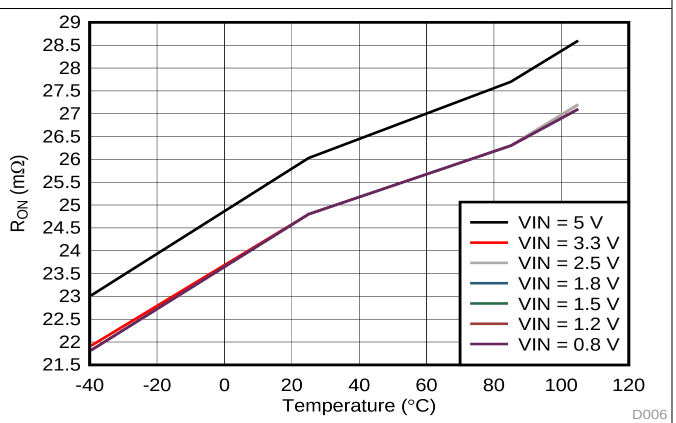
V_{BIAS} = 5 V V_{OUT} = 0 V
$V_{ON1} = V_{ON2}$ = 0 V

Figure 4. V_{IN} vs V_{IN} Shutdown Current



V_{BIAS} = 2.5 V
I_{OUT} = –200 mA

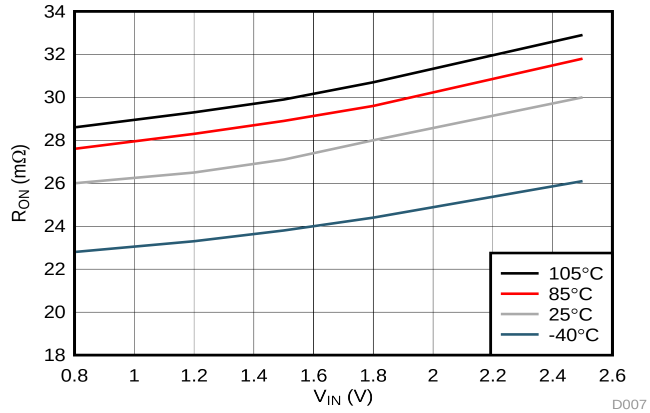
Figure 5. Temperature vs R_{ON}



V_{BIAS} = 5 V
I_{OUT} = –200 mA

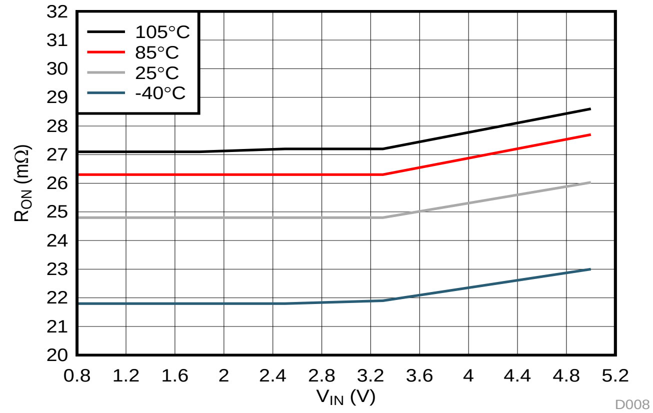
Figure 6. Temperature vs R_{ON}

Typical Characteristics (continued)



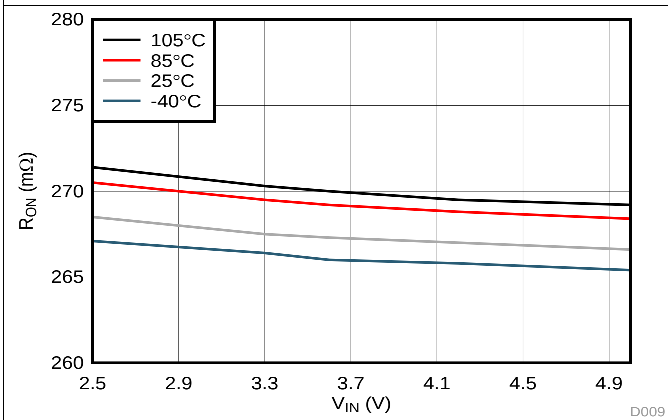
V_{BIAS} = 2.5 V
I_{OUT} = –200 mA

Figure 7. V_{IN} vs R_{ON}



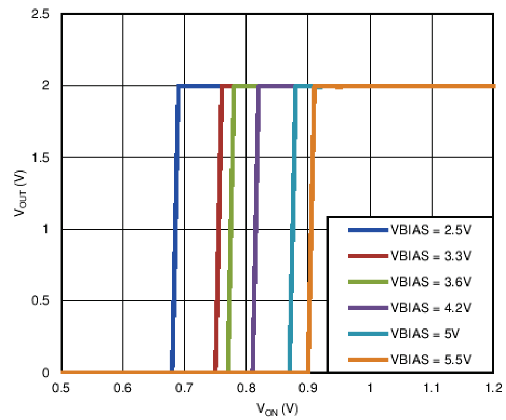
V_{BIAS} = 5 V
I_{OUT} = –200 mA

Figure 8. V_{IN} vs R_{ON}



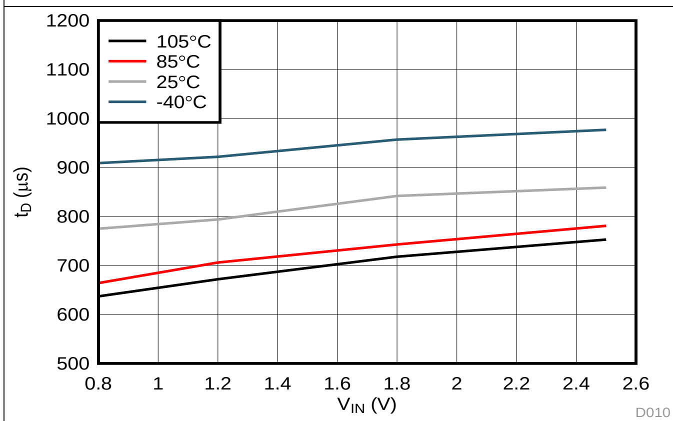
V_{BIAS} = 5 V I_{OUT} = 1 mA
V_{ON} = 0 V

Figure 9. V_{IN} vs R_{PD} (TPS22968 Only) (Single Channel)



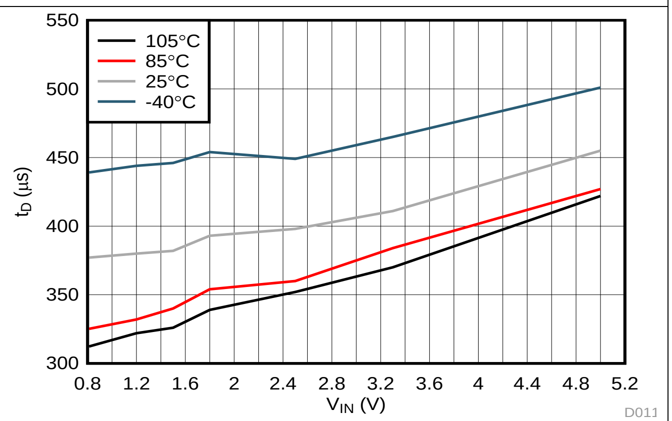
T_A = 25°C
V_{IN} = 2 V

Figure 10. V_{ON} vs V_{OUT}



V_{BIAS} = 2.5 V
CT= 1 nF

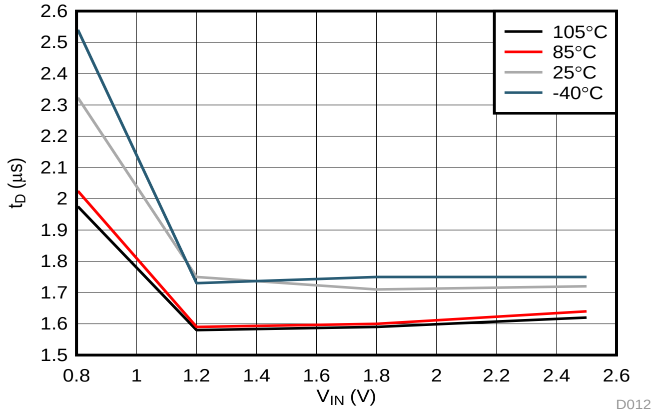
Figure 11. V_{IN} vs t_D



V_{BIAS} = 5 V
CT = 1 nF

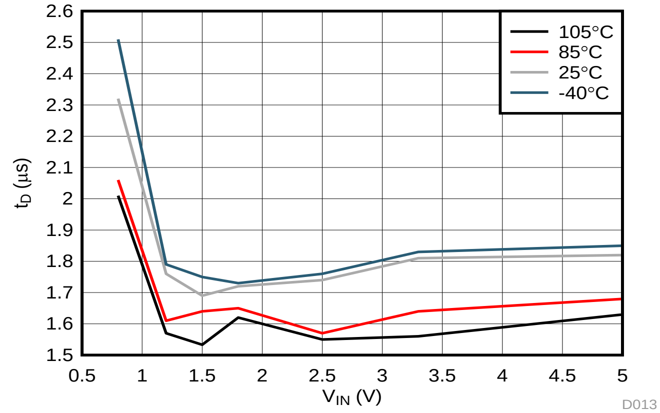
Figure 12. V_{IN} vs t_D

Typical Characteristics (continued)



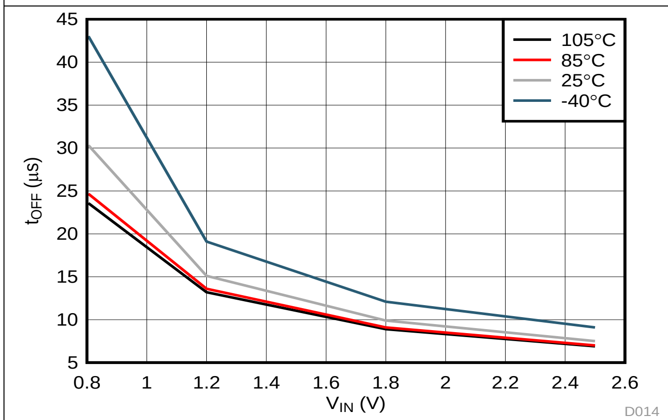
V_{BIAS} = 2.5 V
CT = 1 nF

Figure 13. V_{IN} vs t_F



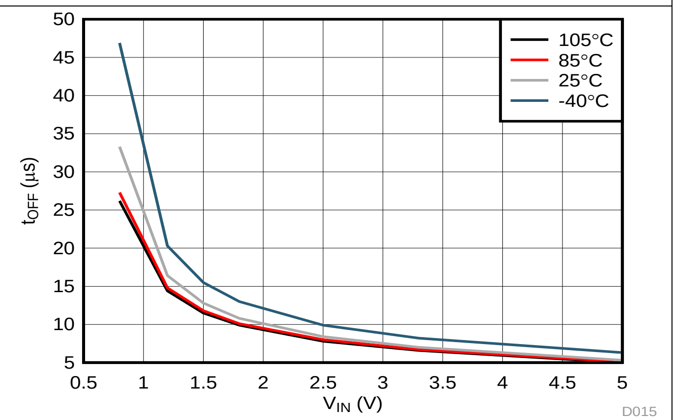
V_{BIAS} = 5 V
CT = 1 nF

Figure 14. V_{IN} vs t_F



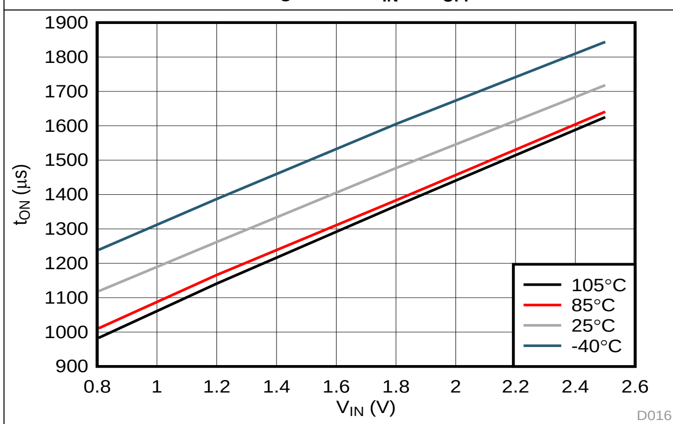
V_{BIAS} = 2.5 V
CT = 1 nF

Figure 15. V_{IN} vs t_{OFF}



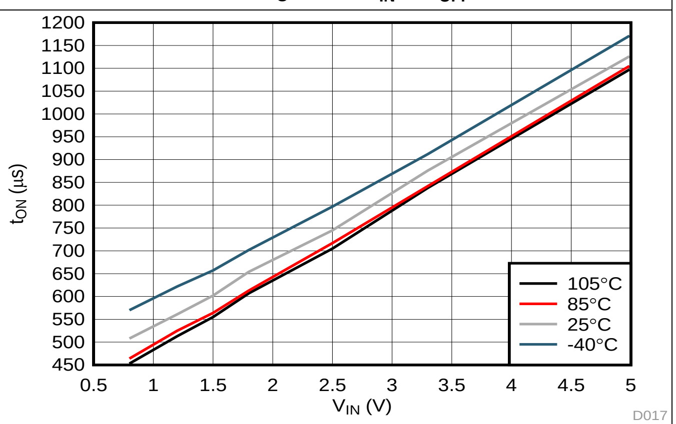
V_{BIAS} = 5 V
CT = 1 nF

Figure 16. V_{IN} vs t_{OFF}



V_{BIAS} = 2.5 V
CT = 1 nF

Figure 17. V_{IN} vs t_{ON}



V_{BIAS} = 5 V
CT = 1 nF

Figure 18. V_{IN} vs t_{ON}

Typical Characteristics (continued)

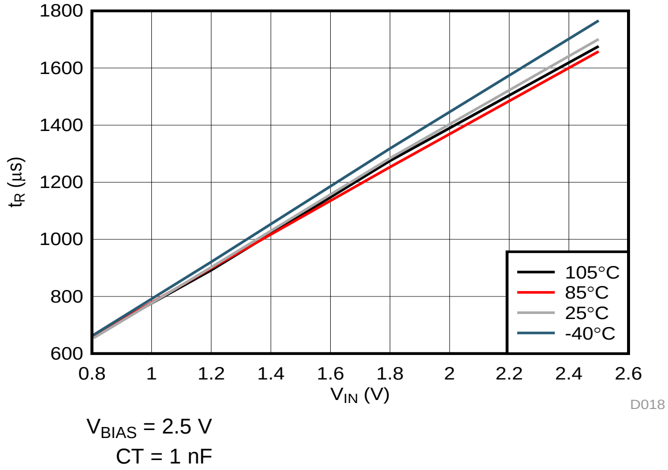


Figure 19. V_{IN} vs t_{ON}

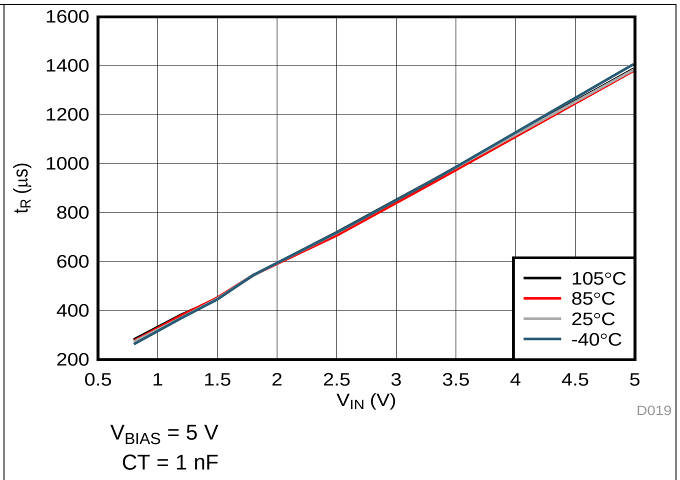


Figure 20. V_{IN} vs t_R

7.9 Typical AC Characteristics

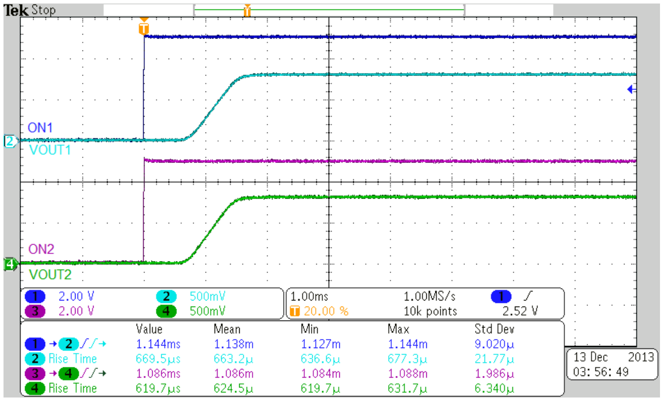


Figure 21. Turn-on Response Time
(V_{IN} = 0.8 V, V_{BIAS} = 2.5 V, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω)

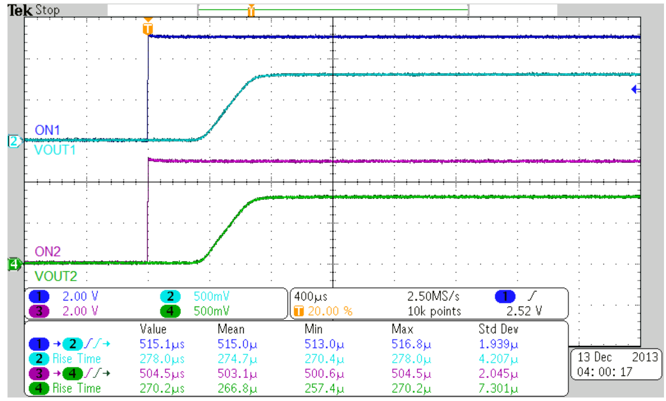


Figure 22. Turn-on Response Time
(V_{IN} = 0.8 V, V_{BIAS} = 5 V, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω)

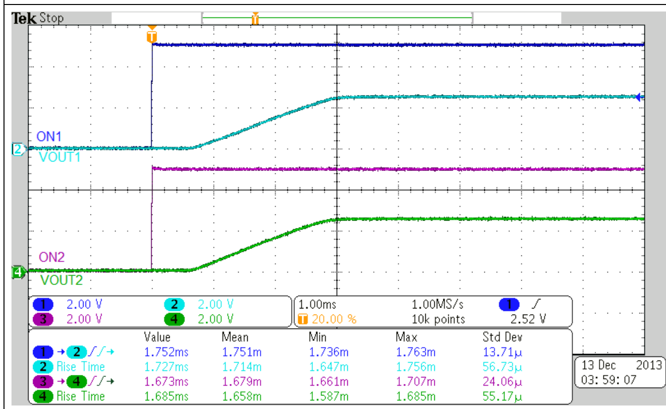


Figure 23. Turn-on Response Time
(V_{IN} = 2.5 V, V_{BIAS} = 2.5 V, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω)

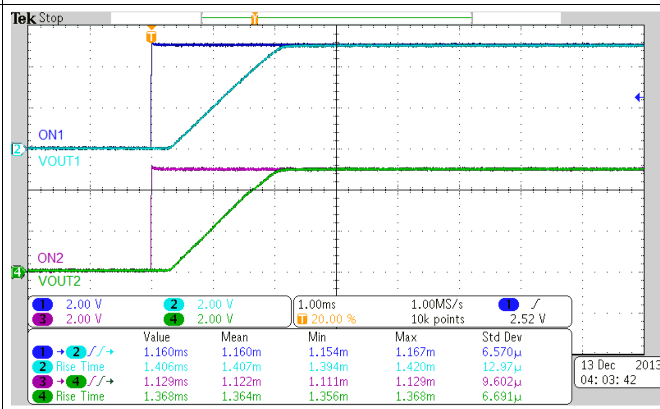


Figure 24. Turn-on Response Time
(V_{IN} = 5 V, V_{BIAS} = 5 V, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω)

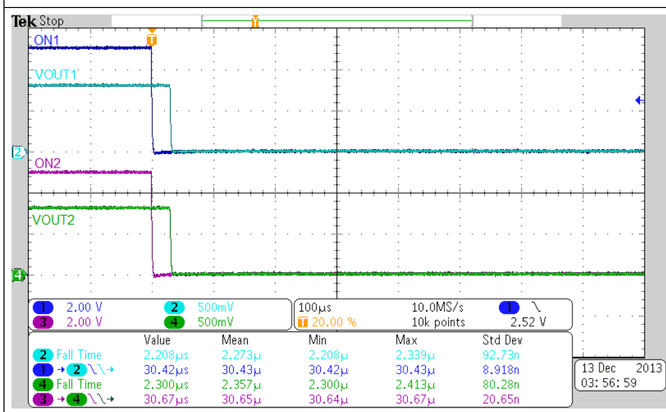


Figure 25. Turn-Off Response Time
(V_{IN} = 0.8 V, V_{BIAS} = 2.5 V, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω)

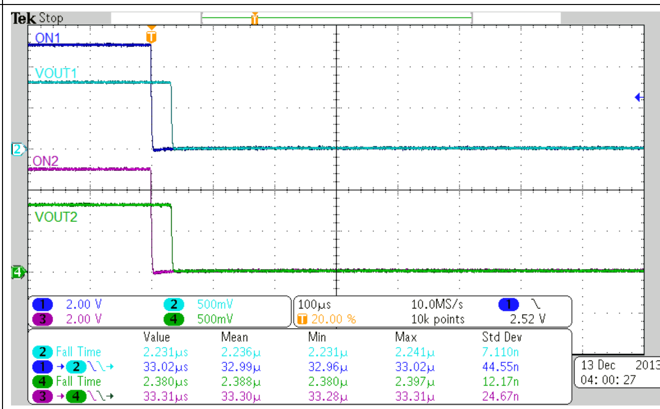


Figure 26. Turn-off Response Time
(V_{IN} = 0.8 V, V_{BIAS} = 5 V, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω)

Typical AC Characteristics (continued)

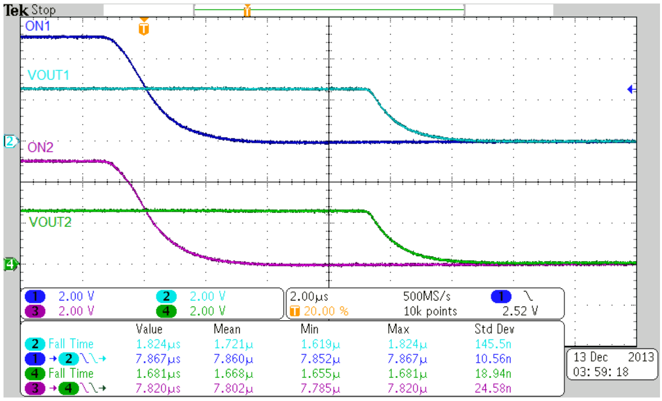


Figure 27. Turn-off Response Time
(V_{IN} = 2.5 V, V_{BIAS} = 2.5 V, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω)

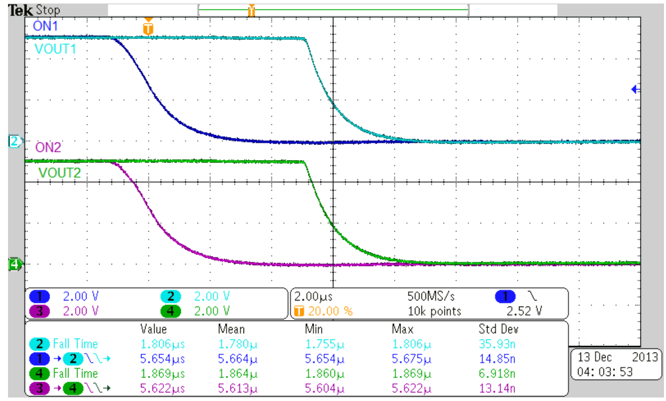
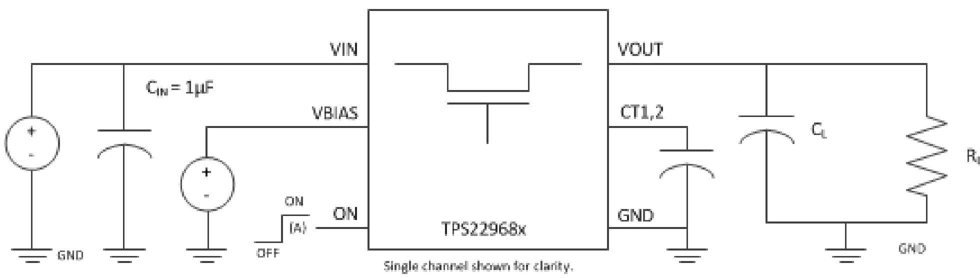
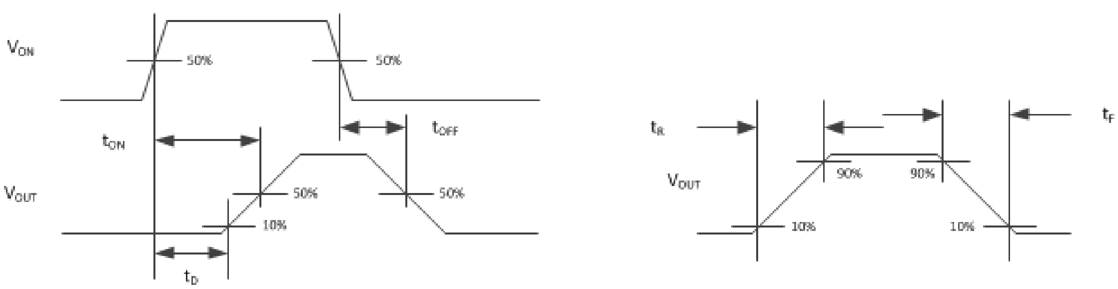


Figure 28. Turn-on Response Time
(V_{IN} = 5 V, V_{BIAS} = 5 V, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω)

8 Parameter Measurement Information



TEST CIRCUIT



TIMING WAVEFORMS

A. Rise and fall times of the control signal is 100 ns.

Figure 29. Test Circuit and Timing Waveforms

9 Detailed Description

9.1 Overview

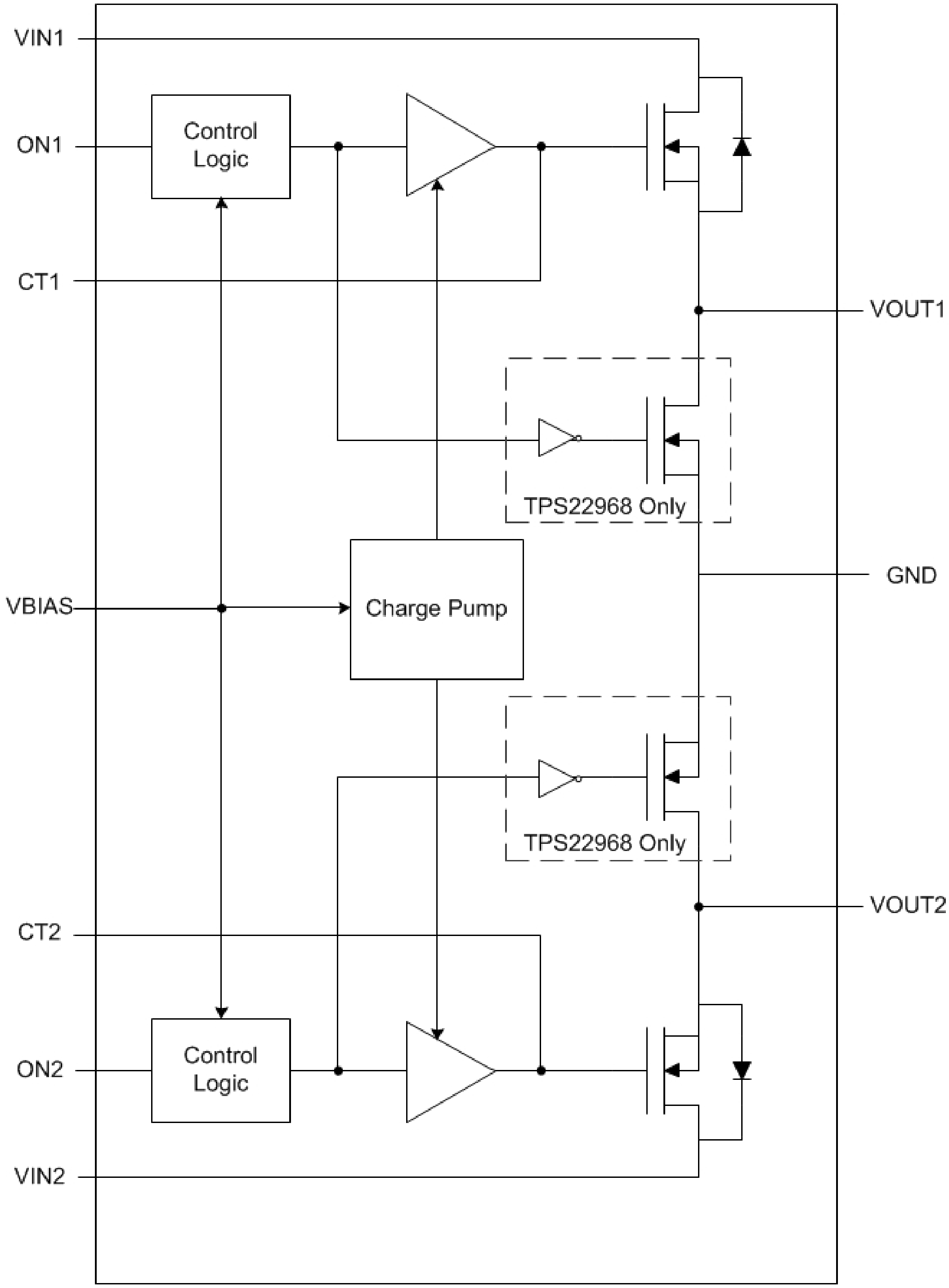
TheTPS22968 is a 5.5 V, 4-A, dual-channel ultra-low R_{ON} load switch with controlled turn on. The device contains two N-channel MOSFETs. Each channel can support a maximum continuous current of 4 A and is controlled by an on/off GPIO-compatible input. The ON pin must be connected and cannot be left floating. The device is designed to control the turn-on rate and therefore the inrush current. By controlling the inrush current, power supply sag can be reduced during turn-on. The slew rate for each channel is set by connecting a capacitor to GND on the CT pins.

The slew rate is proportional to the capacitor on the CT pin. Refer to the *Adjustable Rise Time* section to determine the correct CT value for a desired rise time.

The internal circuitry is powered by the VBIAS pin, which supports voltages from 2.5 V to 5.5 V. This circuitry includes the charge pump, QOD (TPS22968 only), and control logic. For these internal blocks to function correctly, a voltage between 2.5 V and 5.5 V must be supplied to VBIAS.

When a voltage is supplied to VBIAS, the ON1 pin goes low, and the ON2 pins go low, the QOD turns on. This connects VOUT1 and VOUT2 to GND through an on-chip resistor. The typical pulldown resistance (R_{PD}) is 270 Ω.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 ON/OFF Control

The ON pins control the state of the switch. Asserting ON high enables the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2-V or higher GPIO voltage. This pin cannot be left floating and must be tied either high or low for proper functionality.

Feature Description (continued)

9.3.2 Input Capacitor (Optional)

When the switch turns on into a discharged load capacitor or short-circuit, a capacitor must be placed between VIN and GND to limit the voltage drop on the input supply caused by transient inrush currents. A 1-µF ceramic capacitor (C_{IN}), placed close to the pins, is sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high-current application. When switching heavy loads, TI recommends having an input capacitor 10× higher than the output capacitor to avoid excessive voltage drop.

9.3.3 Output Capacitor (Optional)

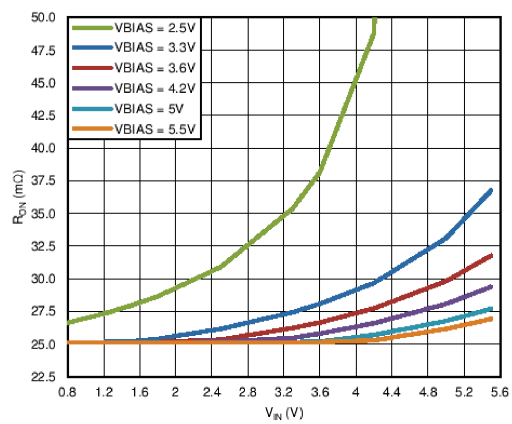
TI highly recommends a C_{IN} greater than C_L, due to the integrated body diode in the NMOS switch. A C_L greater than C_{IN} can cause the voltage on VOUT to exceed VIN when the system supply is removed. This could result in current flow through the body diode from VOUT to VIN. TI recommends a C_{IN} to C_L ratio of 10 to 1 for minimizing V_{IN} dip caused by inrush currents during startup.

9.3.4 QOD (TPS22968 Only)

The TPS22968 includes a QOD feature. When the switch is disabled, a discharge resistor is connected between VOUT and GND. This resistor has a typical value of 270 Ω and prevents the output from floating while the switch is disabled.

9.3.5 VIN and VBIAS Voltage Range

For optimal R_{ON} performance, make sure $V_{IN} \leq V_{BIAS}$. The device is still functional if $V_{IN} > V_{BIAS}$, but it will exhibit R_{ON} greater than what is listed in the *Electrical Characteristics (V_{BIAS} = 5 V)* and *Electrical Characteristics (V_{BIAS} = 2.5 V)* table. See Figure 30 for an example of a typical device. Notice the increasing R_{ON} as V_{IN} exceeds V_{BIAS} voltage. Be sure to never exceed the maximum voltage rating for V_{IN} and V_{BIAS}.



Temperature = 25°C I_{OUT} = 200 mA

Figure 30. R_{ON} vs V_{IN}

Feature Description (continued)

9.3.6 Adjustable Rise Time

A capacitor to GND on the CT pins sets the slew rate for each channel. The capacitor to GND on the CT pins should be rated for 25 V and above. An approximate formula for the relationship between CT and slew rate with V_{BIAS} = 5 V is:

$$SR = 0.32 \times CT + 13.7 \quad (1)$$

where

- SR = slew rate (in µs/V)
- CT = the capacitance value on the CT pin (in pF)
- The units for the constant 13.7 is in µs/V.

Rise time can be calculated by multiplying the input voltage by the slew rate. Table 1 contains rise time values measured on a typical device.

Table 1. Rise Time Table

CTx (pF)	RISE TIME (µs) 10% - 90%, C_L = 0.1 µF, C_{IN} = 1 µF, R_L = 10 Ω, V_{BIAS} = 5 V Typical values at 25°C with a 25-V X7R 10% ceramic capacitor on CT						
	VIN = 5 V	VIN = 3.3 V	VIN = 2.5 V	VIN = 1.8 V	VIN = 1.5 V	VIN = 1.2V	VIN = 0.8 V
0	65	48	41	35	31	29	24
220	378	253	197	152	131	111	83
470	704	474	363	272	234	192	140
1000	1387	931	717	544	449	372	273
2200	3062	2021	1536	1173	991	825	595
4700	7091	4643	3547	2643	2213	1828	1349
10000	14781	9856	7330	5507	4600	3841	2805

9.4 Device Functional Modes

Table 2 lists the device function table.

Table 2. Functional Table

ONx	VINx to VOUTx	VOUTx to GND
L	Off	On
H	On	Off

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

This section highlights some of the design considerations for implementing this device in various applications. A PSPICE model for this device is also available on the product page for additional information.

10.1.1 Parallel Configuration

To increase the current capabilities and lower the R_{ON} by approximately 50%, both channels can be placed in parallel as shown in Figure 31 (parallel configuration). With this configuration, the CT1 and CT2 pins can be tied together to use one capacitor, CT, as shown in Figure 31. With a single CT capacitor, the rise time will be half of the typical rise-time value. Refer to the Table 1 for typical timing values.

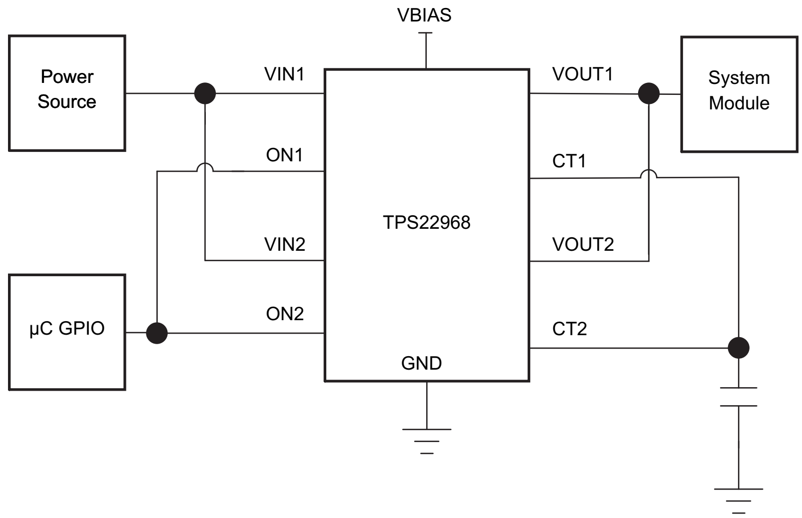


Figure 31. Parallel Configuration

Application Information (continued)

10.1.2 Standby Power Reduction

Any end equipment that is powered from the battery has a need to reduce current consumption to keep the battery charged for a longer time. TPS22968 helps to accomplish this by turning off the supply to the modules that are in standby state, and therefore, significantly reduces the leakage current overhead of the standby modules.

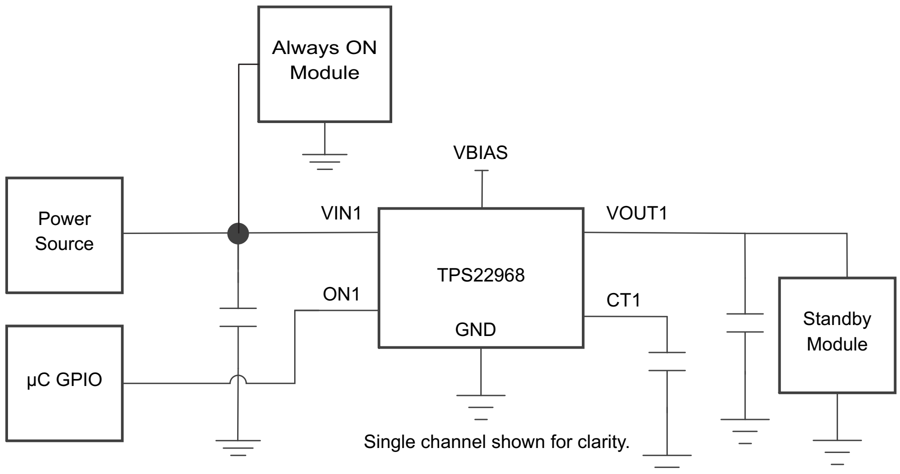
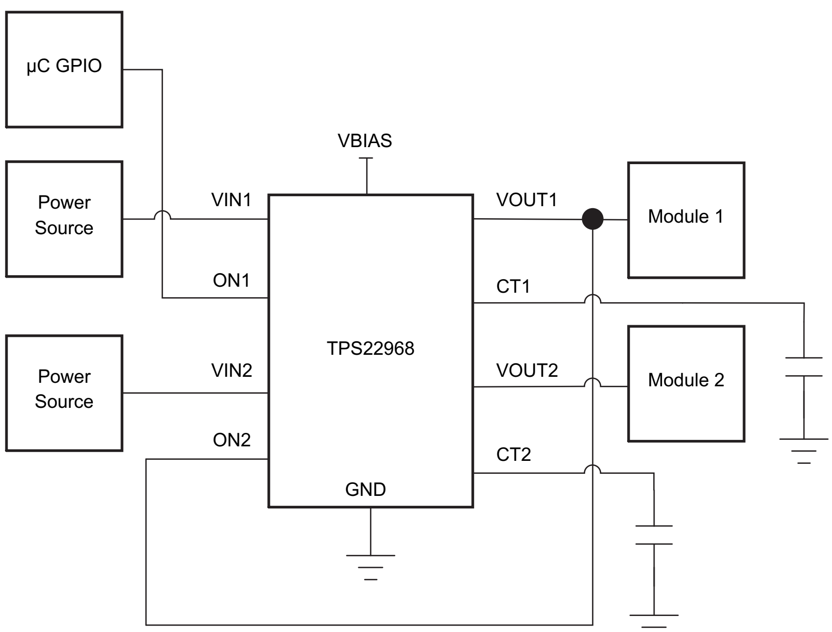


Figure 32. Standby Power Reduction

10.1.3 Power Supply Sequencing Without a GPIO Input

In many end equipments, there is a need to power up various modules in a predetermined manner. The TPS22968 can solve the problem of power sequencing without adding any complexity to the overall system.



VIN1 must be greater V_{IH}.

Figure 33. Power Sequencing Without a GPIO Input

Application Information (continued)

10.1.4 Reverse Current Blocking

In certain applications, it may be desirable to have reverse current blocking. Reverse current blocking prevents current from flowing from the output to the input of the load switch when the device is disabled. With the following configuration, the TPS22968 can be converted into a single-channel switch with reverse current blocking. In this configuration, VIN1 or VIN2 can be used as the input and VIN2 or VIN1 is the output.

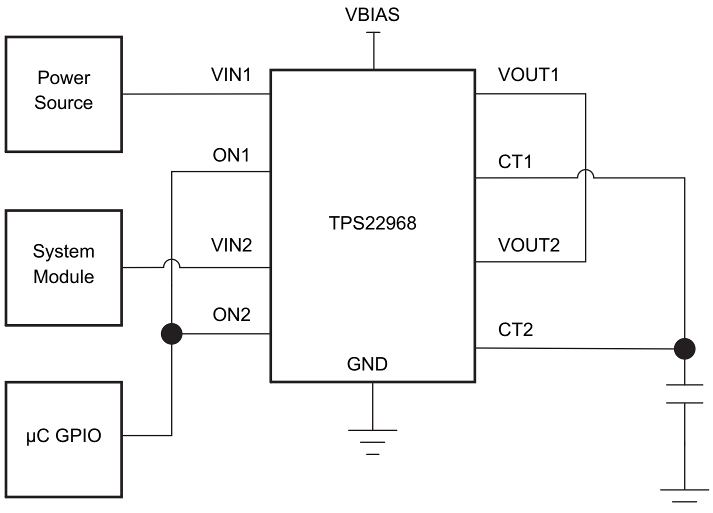


Figure 34. Reverse Current Blocking

10.2 Typical Application

This application demonstrates how the TPS22968 can be used to power downstream modules with large capacitances. The example in Figure 35 is powering a 100-µF capacitive output load.

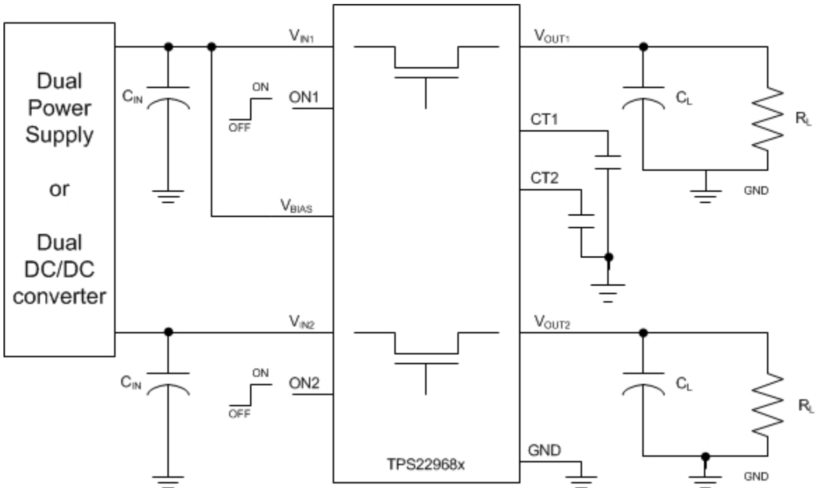


Figure 35. Typical Application Schematic for Powering a Downstream Module

10.2.1 Design Requirements

For this design example, use the following Table 3 as the input parameters.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	3.3 V
V_{BIAS}	5.0 V
Load current	4 A
Output capacitance (C_L)	22 µF
Allowable inrush current on VOUT	0.33 A

10.2.2 Detailed Design Procedure

To begin the design process, the designer needs to know the following:

- V_{IN} voltage
- V_{BIAS} voltage
- Load current
- Allowable inrush current on VOUT due to C_L capacitor

10.2.2.1 VIN to VOUT Voltage Drop

The VIN to VOUT voltage drop in the device is determined by the R_{ON} of the device and the load current. The R_{ON} of the device depends upon the V_{IN} and V_{BIAS} conditions of the device. Refer to the R_{ON} specification of the device in the *Electrical Characteristics (V_{BIAS} = 5 V)* and *Electrical Characteristics (V_{BIAS} = 2.5 V)* . After the R_{ON} of the device is determined based upon the V_{IN} and V_{BIAS} conditions, use Equation 2 to calculate the VIN to VOUT voltage drop:

$$\Delta V = I_{LOAD} \times R_{ON}$$

where

- ΔV = voltage drop from VIN to VOUT
- I_{LOAD} = load current
- R_{ON} = On-resistance of the device for a specific V_{IN} and V_{BIAS} combination (2)

An appropriate I_{LOAD} must be chosen such that the I_{MAX} specification of the device is not violated.

10.2.2.2 Inrush Current

To determine how much inrush current will be caused by the C_L capacitor, use Equation 3.

$$I_{INRUSH} = C_L \times \frac{dV_{OUT}}{dt}$$

where
- I_{INRUSH} = amount of inrush caused by C_L
- C_L = capacitance on VOUT
- dt = time it takes for change in V_{OUT} during the ramp up of VOUT when the device is enabled
- dV_{OUT} = change in V_{OUT} during the ramp up of VOUT when the device is enabled (3)

The device offers adjustable rise time for VOUT. This feature allows the user to control the inrush current during turn-on through the CTx pins. The appropriate rise time can be calculated using the design requirements and the inrush current equation (Equation 3).

$$330 \text{ mA} = 22 \text{ µF} \times 3.3 \text{ V} / dt \quad (4)$$

$$dt = 220 \text{ µs} \quad (5)$$

To ensure an inrush current of less than 330 mA, choose a CT based on Table 1 or Equation 1 value that will yield a rise time of more than 220 µs. See the oscilloscope captures in the *Application Curves* for an example of how the CT capacitor can be used to reduce inrush current. See Table 1 for correlation between rise times and CT values.

An appropriate C_L value should be placed on VOUT such that the I_{MAX} and I_{PLS} specifications of the device are not violated.

10.2.2.3 Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use Equation 6.

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}}$$

where
- $P_{D(max)}$ = maximum allowable power dissipation
- $T_{J(max)}$ = maximum allowable junction temperature (125°C for the TPS22968)
- T_A = ambient temperature of the device
- $R_{\theta JA}$ = junction to air thermal impedance. See *Thermal Information* . This parameter is highly dependent upon board layout. (6)

Below are two examples to determine how to use this information correctly:

For V_{BIAS} = 5 V, V_{IN} = 5 V, the maximum ambient temperature with a 4-A load through each channel can be determined by using the following calculation:

$$P_D = I^2 \times R \times 2 \text{ (multiplied by 2 because there are two channels)} \quad (7)$$

$$2 \times I^2 \times R = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} \quad (8)$$

$$T_A = T_{J(MAX)} - R_{\theta JA} \times 2 \times I^2 \times R \quad (9)$$

$$T_A = 125°C - 62.5°C/W \times 2 \times (4\text{ A})^2 \times 27\text{ m}\Omega = 71°C \quad (10)$$

For V_{BIAS} = 5 V, V_{IN} = 5 V, the maximum continuous current for an ambient temperature of 85°C with the same current flowing through each channel can be determined by using the following calculation:

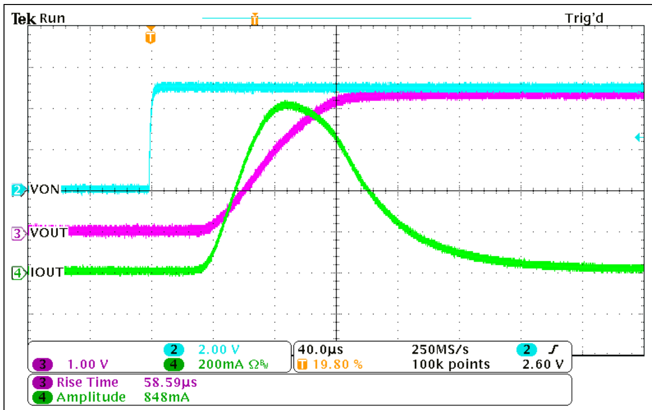
$$2 \times I^2 \times R = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} \quad (11)$$

$$I = \sqrt{\frac{T_{J(MAX)} - T_A}{2 \times R \times R_{\theta JA}}} \quad (12)$$

$$I = \sqrt{\frac{125°C - 105°C}{2 \times 27 m\Omega \times 62.5°C/W}} = 3.44 \text{ A per channel} \quad (13)$$

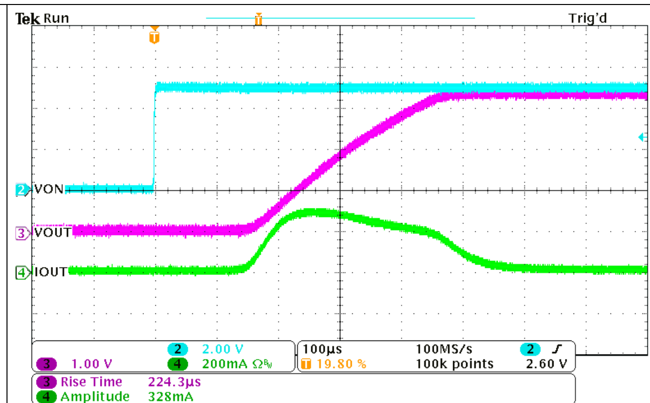
10.2.3 Application Curves

The twp scope captures show the usage of a CT capacitor in conjunction with the device. A higher CT value results in a slower rise and a lower inrush current.



VBIAS = 5 V   VIN = 3.3 V T_A = 25°C
CT = Open

Figure 36. Inrush Current Without CT Capacitor



VBIAS = 5 V   VIN = 3.3 V T_A = 25°C
CT = 220 pF

Figure 37. Inrush Current With CT = 220 pF

11 Power Supply Recommendations

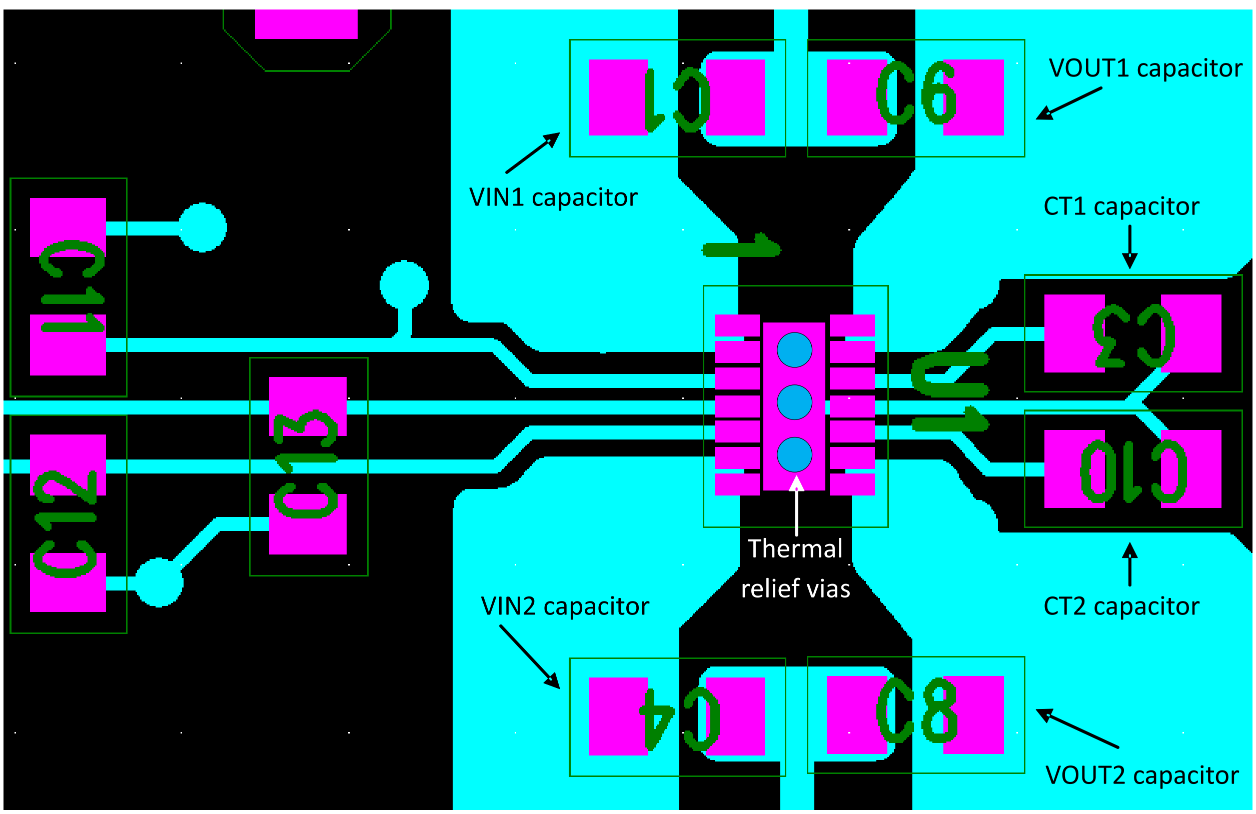
The device is designed to operate from a V_{BIAS} range of 2.5 V to 5.5 V and V_{IN} range of 0.8 V to 5.5 V. This supply must be well regulated and placed as close to the device pin as possible with the recommended 1-µF bypass capacitor. If the supply is located more than a few inches from the device pins, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 10 µF may be sufficient.

12 Layout

12.1 Layout Guidelines

- VIN and VOUT traces should be as short and wide as possible to accommodate for high current.
- Use vias under the exposed thermal pad for thermal relief for high current operation.
- VINx pins should be bypassed to ground with low-ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 1-µF ceramic with X5R or X7R dielectric. This capacitor should be placed as close to the device pins as possible.
- VOUTx pins should be bypassed to ground with low-ESR ceramic bypass capacitors. The typical recommended bypass capacitance is one-tenth of the VINx bypass capacitor of X5R or X7R dielectric rating. This capacitor should be placed as close to the device pins as possible.
- The VBIAS pin should be bypassed to ground with low-ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 0.1-µF ceramic with X5R or X7R dielectric.
- The CTx capacitors should be placed as close to the device pins as possible. The typical recommended CTx capacitance is a capacitor of X5R or X7R dielectric rating with a rating of 25 V or higher.

12.2 Layout Example



13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS22968	Click here	Click here	Click here	Click here	Click here
TPS22968N	Click here	Click here	Click here	Click here	Click here

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

E2E is a trademark of Texas Instruments.
Ultrabook is a trademark of Intel.

13.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22968DPUR	ACTIVE	WSON	DPU	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	RB968	Samples
TPS22968DPUT	ACTIVE	WSON	DPU	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	RB968	Samples
TPS22968NDPUR	ACTIVE	WSON	DPU	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	RB968N	Samples
TPS22968NDPUT	ACTIVE	WSON	DPU	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	RB968N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS22968 :

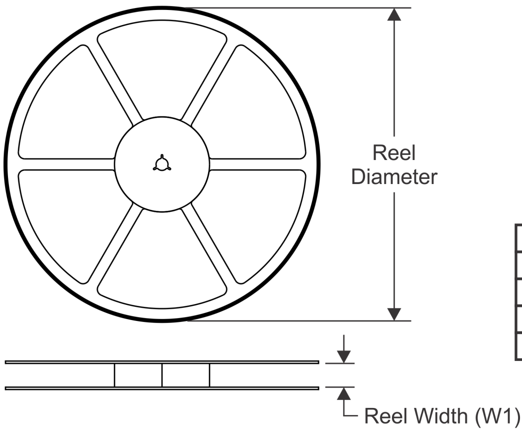
- Automotive: TPS22968-Q1

NOTE: Qualified Version Definitions:

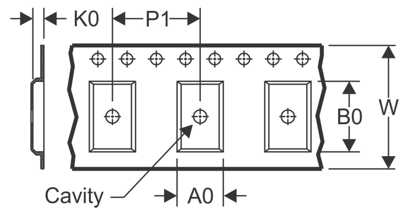
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

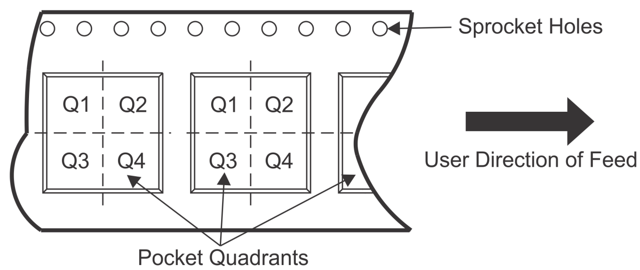


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

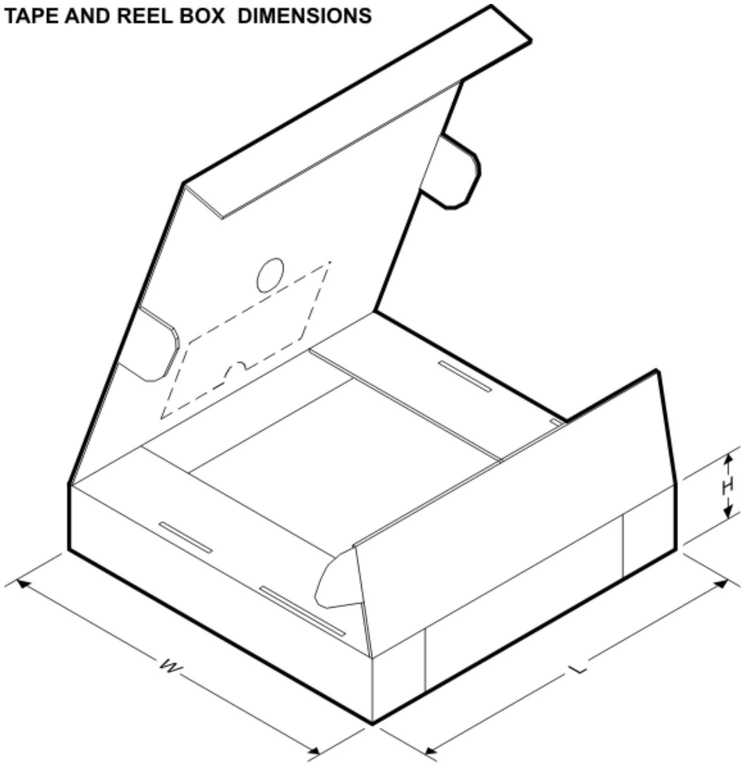
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22968DPUR	WSON	DPU	14	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS22968DPUT	WSON	DPU	14	250	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS22968NDPUR	WSON	DPU	14	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS22968NDPUT	WSON	DPU	14	250	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1

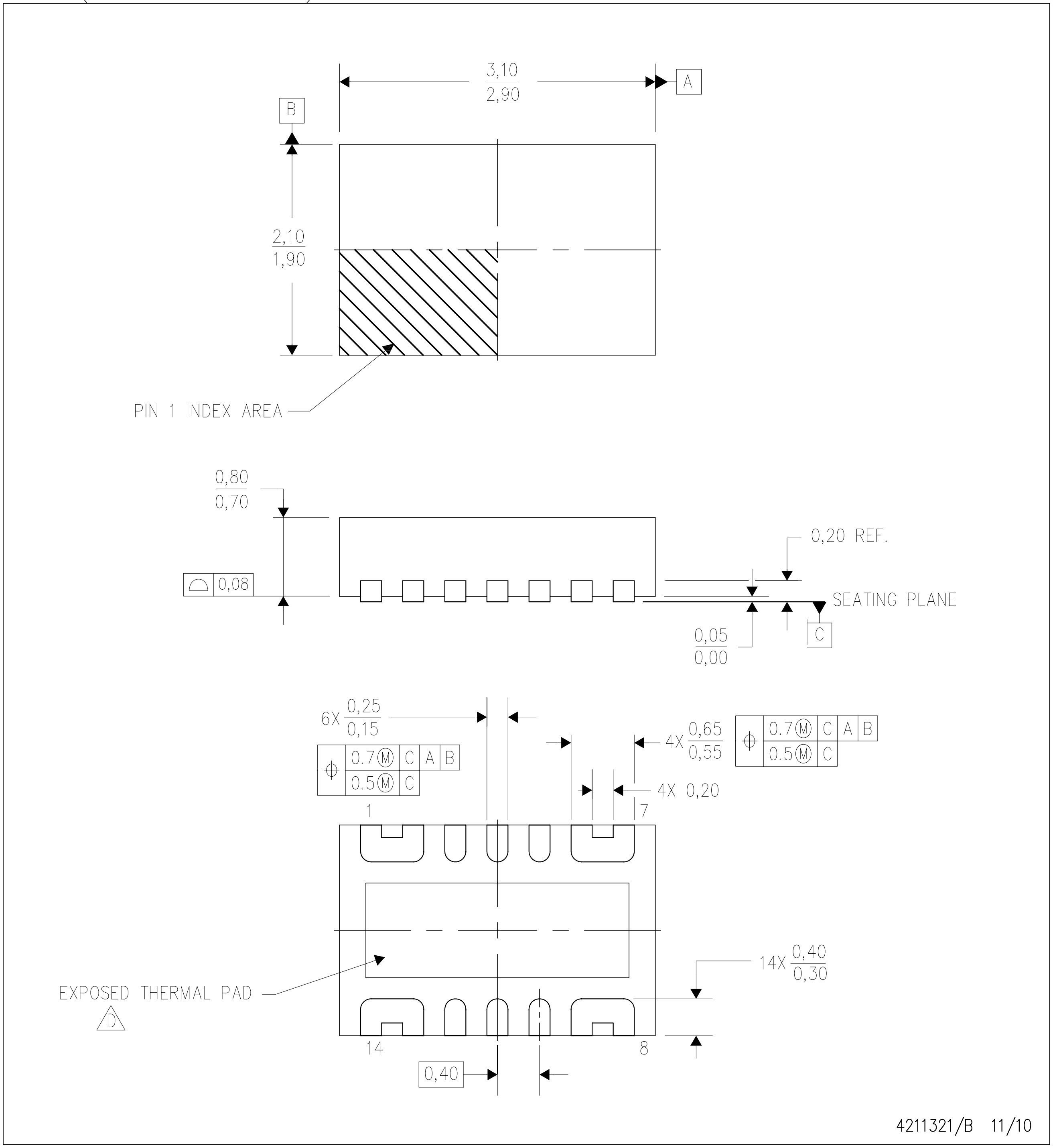
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22968DPUR	WSON	DPU	14	3000	210.0	185.0	35.0
TPS22968DPUT	WSON	DPU	14	250	210.0	185.0	35.0
TPS22968NDPUR	WSON	DPU	14	3000	210.0	185.0	35.0
TPS22968NDPUT	WSON	DPU	14	250	210.0	185.0	35.0

DPU (R–PWSON–N14) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Small Outline No–Lead (SON) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
- E. This package is Pb–free.

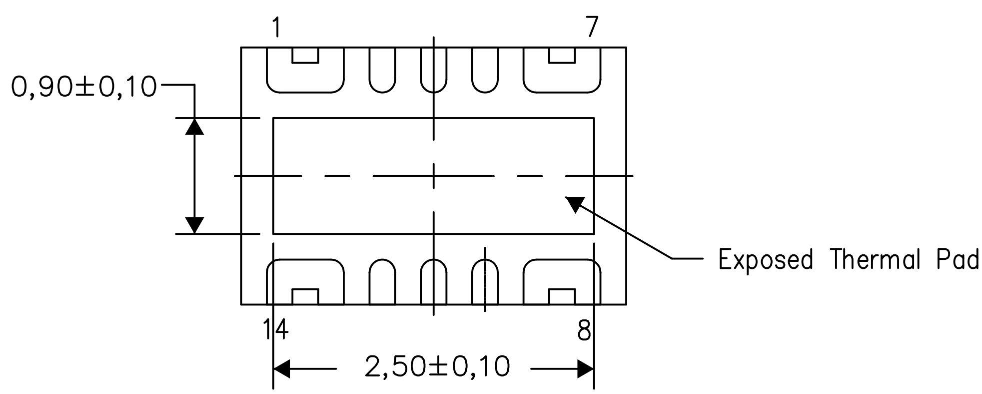
DPU (R-PWSON-N14) PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



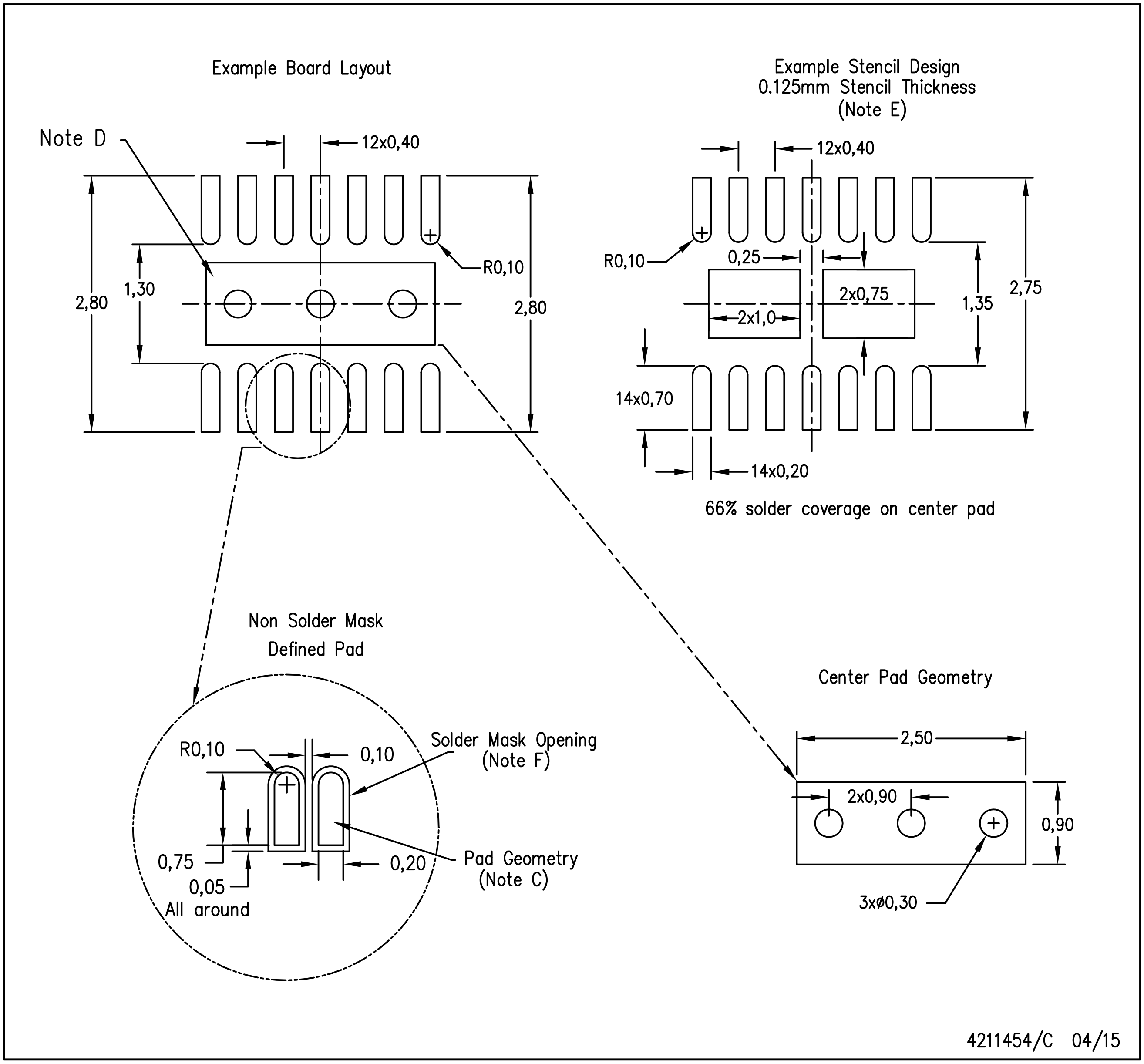
Bottom View

Exposed Thermal Pad Dimensions

4211395/C 04/15

NOTE: All linear dimensions are in millimeters

DPU (R–PWSON–N14) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.