TPS22971 3.6-V, 3-A, 7.5-mΩ On-Resistance Load Switch With Adjustable Fast Turnon and Power Good

1 Features

- Input Voltage Range (V_{IN}): 0.65 V to 3.6 V
- On-Resistance
  - R_{ON} = 7.5 mΩ (typical) at V_{IN} ≥ 1.8 V
  - R_{ON} = 8 mΩ (typical) at V_{IN} = 1.05 V
  - R_{ON} = 10 mΩ (typical) at V_{IN} = 0.65 V
- Maximum Continuous Switch Current (I_{MAX}): 3 A
- ON State (I_Q): 35 µA (typical)
- OFF State (I_{SD}): 1 µA (typical)
- Controlled and Adjustable Slew Rate through CT Pin
- Power Good (PG) Indicator After Switch Turn ON
- Low Threshold Enable (ON) supports use of logic as low as 0.9 V (V_{IH}) of Logic
- Thermal Shutdown (T_{SD}): T_J > 125°C
- Quick Output Discharge (QOD): 150-Ω (typical)

2 Applications

- Notebook, Tablet
- Industrial PC
- Smartphones
- Telecom
- Storage

3 Description

The TPS22971 is a space-saving single-channel load switch with controlled and adjustable turnon slew rate and an integrated PG indicator. The device contains an N-channel MOSFET that can operate over a low input voltage range of 0.65 V to 3.6 V and can support a maximum continuous current of 3 A. A Low on-resistance of 7.5-mΩ minimizes the power loss and voltage drop across the load switch. The switch is controlled by an on and off input (ON), which is capable of interfacing directly with low-voltage control signals.

The TPS22971 is capable of thermal shutdown to turn off when the junction temperature is above the recommended operating maximum. The switch turns on again when the junction temperature lowers to a safe range.

The TPS22971 has a 150-Ω on-chip resistor for quick discharge of the output when switch is disabled to avoid any unknown state caused by floating supply to the downstream load.

The TPS22971 has an internally adjustable rise time in order to reduce inrush current. The switch also has integrated Power Good (PG) indicator for seamless downstream power sequencing.

The TPS22971 is available in a 1.9-mm × 0.9-mm, 0.4-mm pin pitch, 0.5-mm height 8-pin DSBGA package and is characterized for operation over the temperature range of –40°C to 125°C.

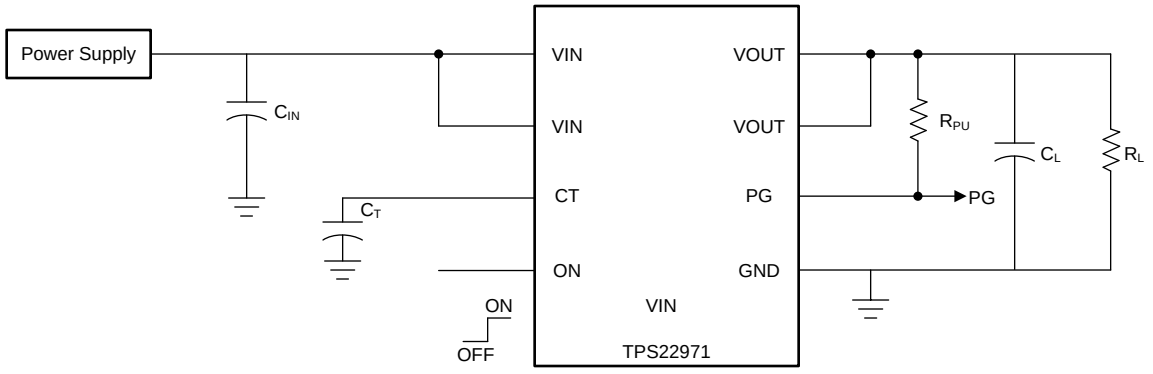
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22971YZPT	DSBGA (8)	1.90 mm × 0.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

ADVANCE INFORMATION

Typical Application



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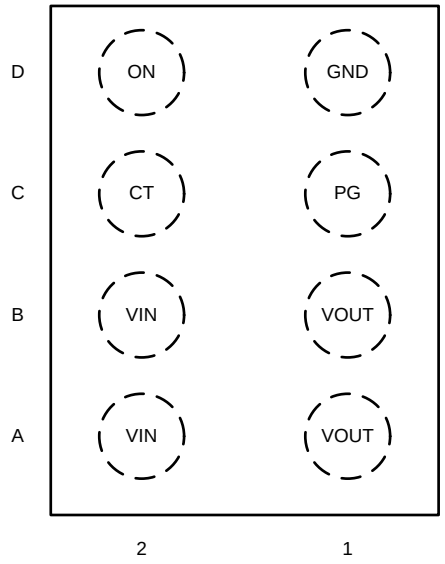
4 Revision History

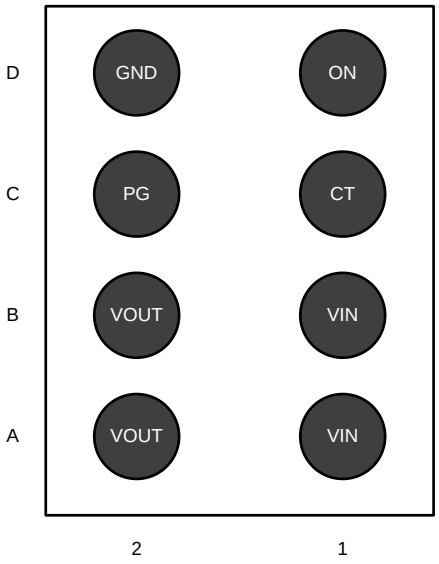
DATE	REVISION	NOTES
April 2017	*	Initial release.

5 Pin Configuration and Functions

YZP Package
8-Pin DSBGA
Laser Marking View



YZP Package
8-Pin DSBGA
Bump View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CT	C2	O	VOUT slew rate control
GND	D1	GND	Ground
ON	D2	I	Switch control input. Do not leave floating
PG	C1	O	Power good. Active high, open drain output
V_{OUT}	A1, B1	O	Switch output
V_{IN}	A2, B2	I	Switch input, bypass this input with a ceramic capacitor to ground

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	4	V
V_{OUT}	Output voltage	–0.3	4	V
V_{ON}	ON voltage	–0.3	4	V
V_{PG}	PG voltage	–0.3	4	V
I_{MAX}	Maximum continuous switch current		3	A
I_{PLS}	Maximum pulsed switch current, pulse < 300-µs, 2% duty cycle		4	A
T_J	Maximum junction temperature	Internally Limited		
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage	0.65	3.6	V
V_{OUT}	Output voltage		V_{IN}	V
V_{IH}	High-level input voltage, ON	0.9	3.6	V
V_{IL}	Low-level input voltage, ON	0	0.45	V
T_J	Operating temperature	–40	125	°C
C_T	C_T pin capacitor voltage rating	7		V

6.4 Thermal Information

THERMAL METRIC (1)		TPS22971 YZP (DSBGA) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	130	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Switching Characteristics

V_{IN} = 1 V, V_{ON} = 1 V, T_A = 0ºC to 85ºC (unless otherwise noted)

PARAMETER		TEST CONDITION	TYP	MAX	UNIT
t_{ON}	Turnon time	C_T = OPEN	30	65	µs

ADVANCE INFORMATION

6.6 Typical Characteristics

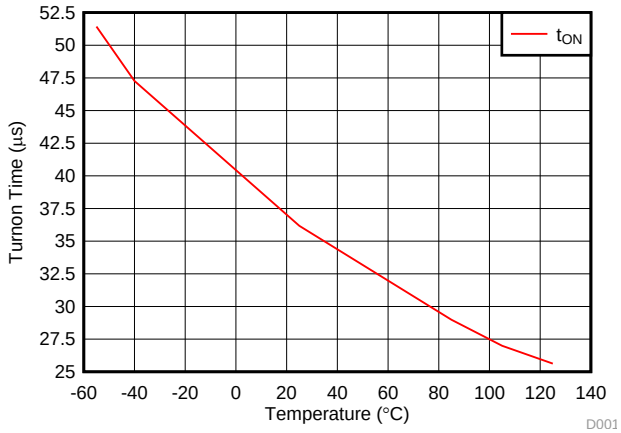


Figure 1. Turnon time vs Temperature

ADVANCE INFORMATION

7 Parameter Measurement Information

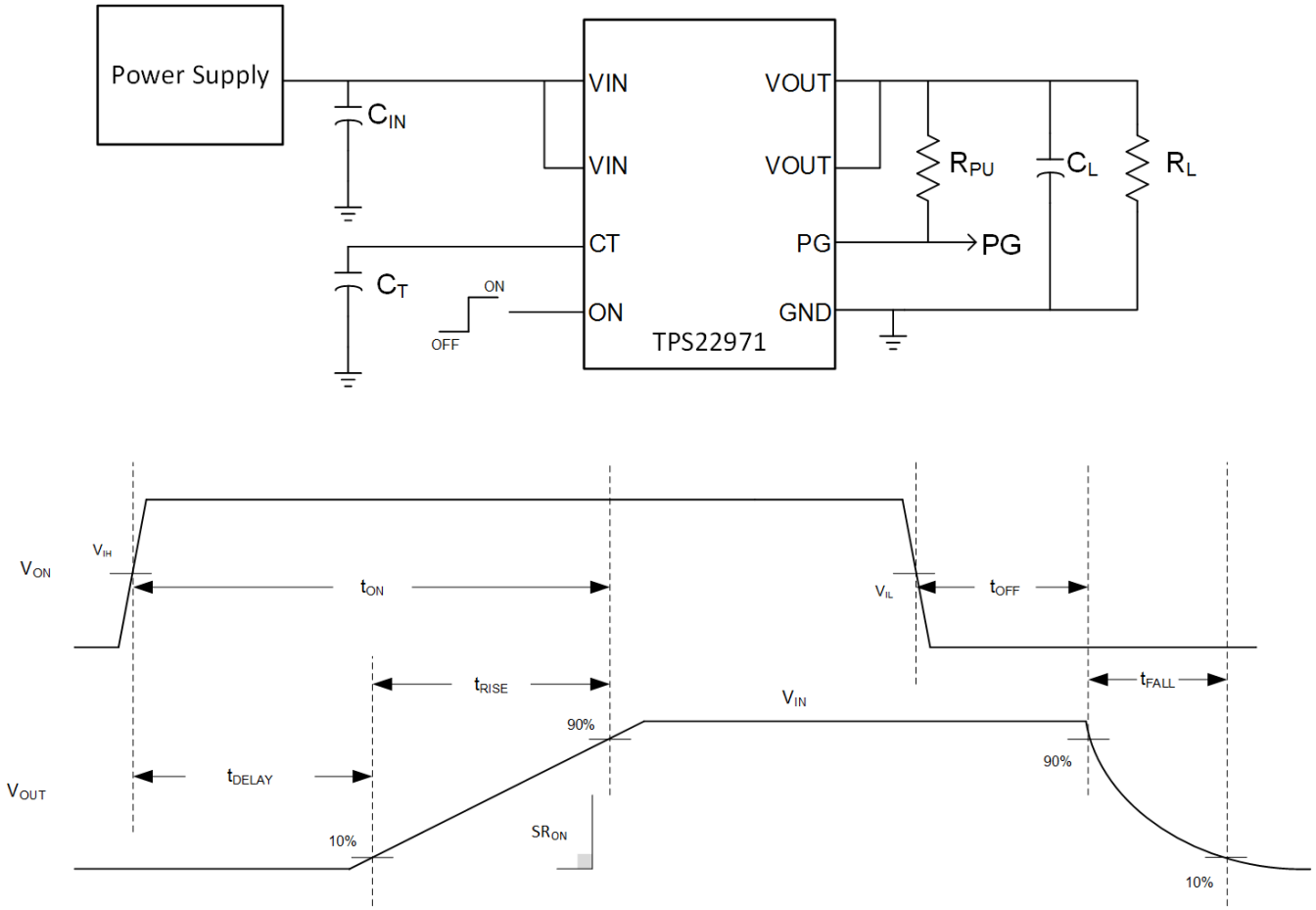


Figure 2. TPS22971 Test Circuit and T_{ON}/T_{OFF} Waveforms

ADVANCE INFORMATION

8 Detailed Description

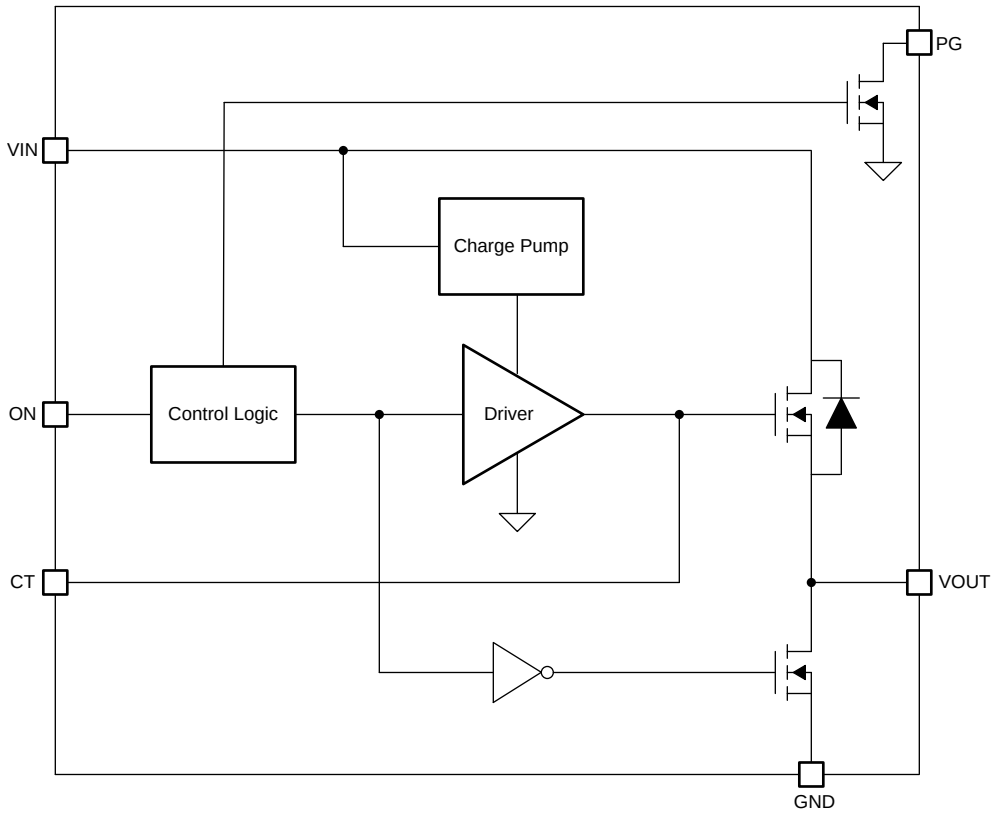
8.1 Overview

The TPS22971 is a single channel, 3-A load switch in a small, space-saving DSBGA-8 package. This device implements a low resistance N-channel MOSFET with a controlled rise time for applications that need to limit the inrush current.

The controlled rise time for the device greatly reduces inrush current caused by large bulk load capacitances, thereby reducing or eliminating power supply droop. The adjustable slew rate through CT provides the design flexibility to trade off the inrush current and power up timing requirements. Integrated PG indicator notifies the system about the status of the load switch to facilitate power sequencing.

This device is also designed to have low leakage current during off state, which prevents downstream circuits from pulling high standby current from the supply. Integrated control logic, driver, power supply, and output discharge FET eliminates the need for additional external components, which reduces solution size and bill of materials (BOM) count.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 On and Off Control

The ON pin controls the state of the switch. Asserting ON high enables the switch. ON has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic. It can be used with any microcontroller with 1.2-V, 1.8-V, 2.5-V or 3.3-V GPIOs. This pin does not have an internal bias and must not be left floating for proper functionality.

Feature Description (continued)

8.3.2 Quick Output Discharge (QOD)

The TPS22971 includes a QOD feature. When the switch is disabled, a discharge resistor is connected between VOUT and GND. This resistor has a typical value of 150 Ω and prevents the output from floating while the switch is disabled.

8.4 Device Functional Modes

Table 1 lists the functional modes for the TPS22971.

Table 1. Function Table

TPS22971			
ON-Pin	**V_{IN} to V_{OUT}**	**V_{OUT} to GND**	**PG to GND**
Below V_{IL}	OFF	ON	ON
Above V_{IH}	ON	OFF	OFF

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Thermal Consideration

It is recommended to limit the junction temperature (T_J) to below 125°C. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use Equation 1 as a guideline:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\theta_{JA}} \quad (1)$$

where

- $P_{D(max)}$ is maximum allowable power dissipation
- $T_{J(max)}$ is maximum allowable junction temperature
- T_A is ambient temperature of the device
- Θ_{JA} is junction to air thermal impedance. See the *Thermal Information* section. This parameter is highly dependent upon board layout

9.1.2 Power Sequencing

The TPS22971 has an integrated power good indicator which can be used for power sequencing. As shown in Figure 3, the switch to the second load is controlled by the PG signal from the first switch. This ensures that the power to load 2 is only enabled after the power to load 1 is enabled after the first switch has turned on.

ADVANCE INFORMATION

Application Information (continued)

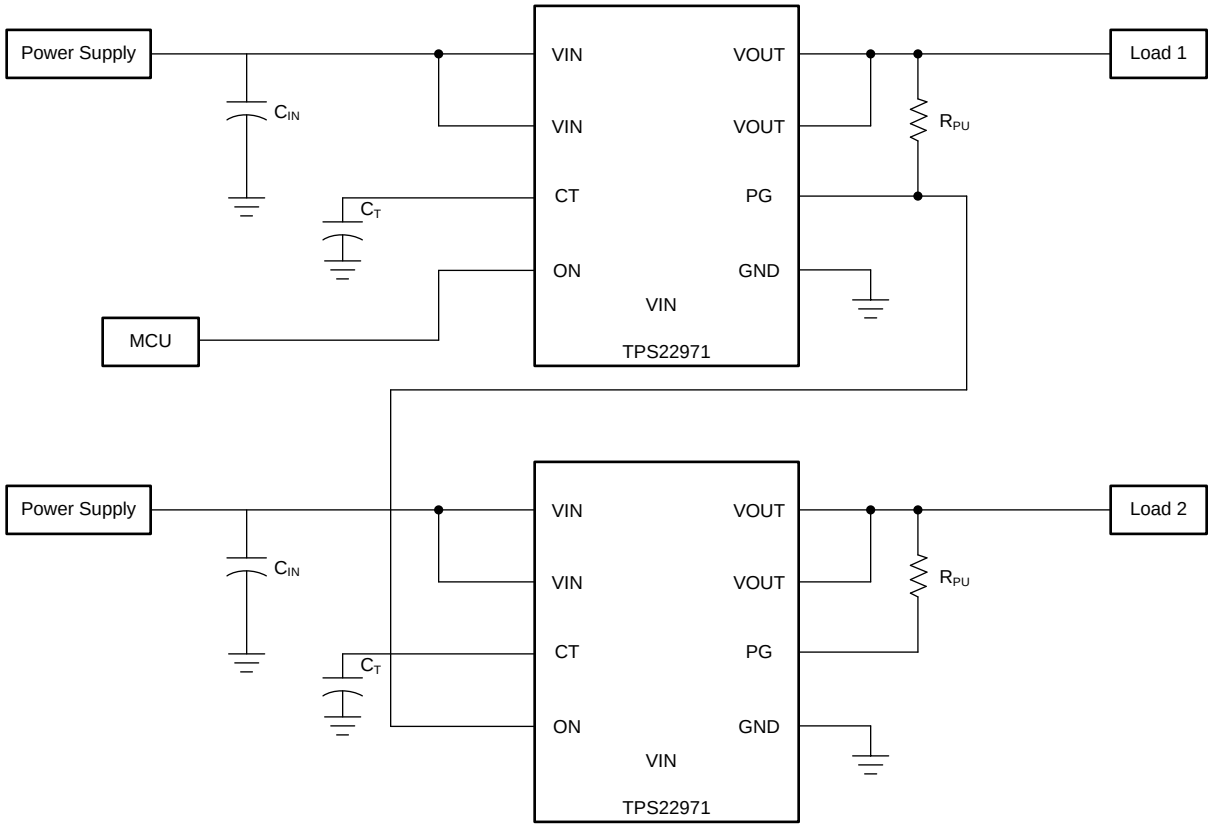


Figure 3. Power Sequencing

9.2 Typical Application

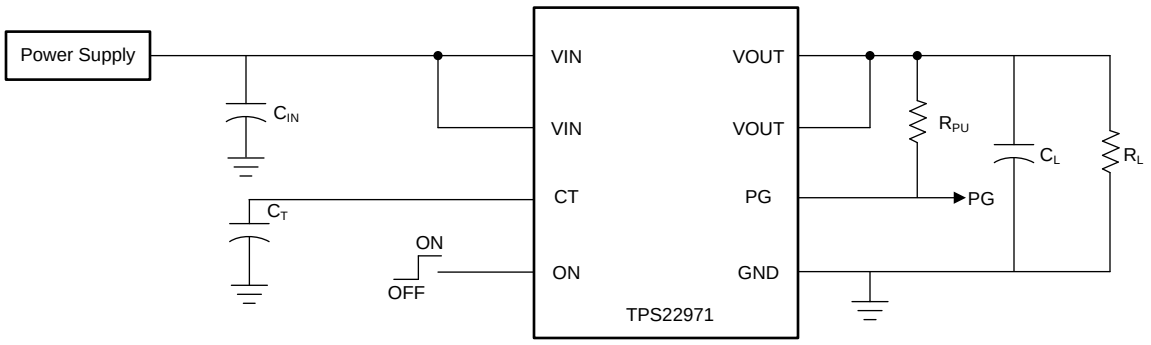


Figure 4. Typical Application Circuit

9.2.1 Design Requirements

For this design example, below, use the input parameters shown in Table 2.

ADVANCE INFORMATION

Typical Application (continued)

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	1.05 V
I_{LOAD}	2 A
Maximum voltage drop	5%

9.2.2 Detailed Design Procedure

At 1.05-V input voltage, with a maximum voltage drop tolerance of 5%, the TPS22971 has a typical R_{ON} of 8 mΩ. The rail is supplying 2 A of current; the voltage drop for a rail is calculated based on Equation 2.

$$V_{DROP} = R_{ON} \times I_{LOAD} \quad (2)$$

$$V_{DROP} = 16mV \quad (3)$$

The maximum voltage drop is 5% which is 52.5 mV. The voltage drop caused by the load current across the on resistance is 16 mV.

ADVANCE INFORMATION

10 Power Supply Recommendations

The device is designed to operate from a VIN range of 0.65 V to 3.6 V. The VIN power supply must be well regulated and placed as close to the device terminal as possible. The power supply must be able to withstand all transient load current steps. In most situations, using an input capacitance of 1 µF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input.

The requirements for larger input capacitance can be mitigated by adding additional capacitance to the CT pin. This causes the load switch to turn on more slowly. Not only does this reduce transient inrush current, but it also gives the power supply more time to respond to the load current step.

11 Layout

11.1 Layout Guidelines

All traces must be as short as possible for best performance. Using wide traces for V_{IN}, V_{OUT}, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

11.2 Layout Example

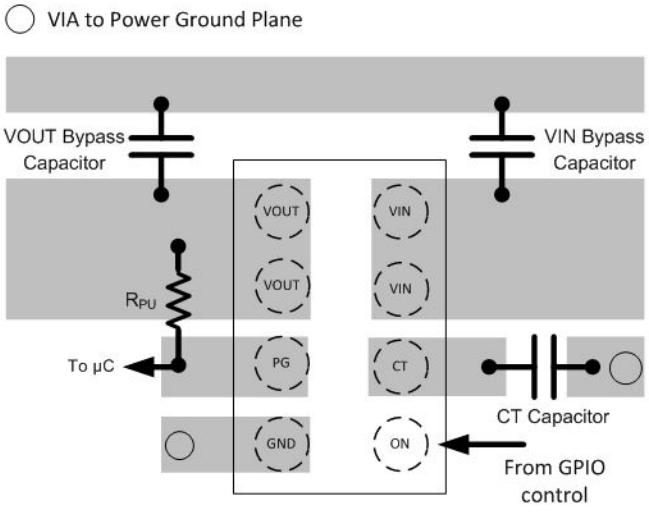


Figure 5. Package Layout Examples

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

TPS22971 Load Switch Evaluation Module User's Guide

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

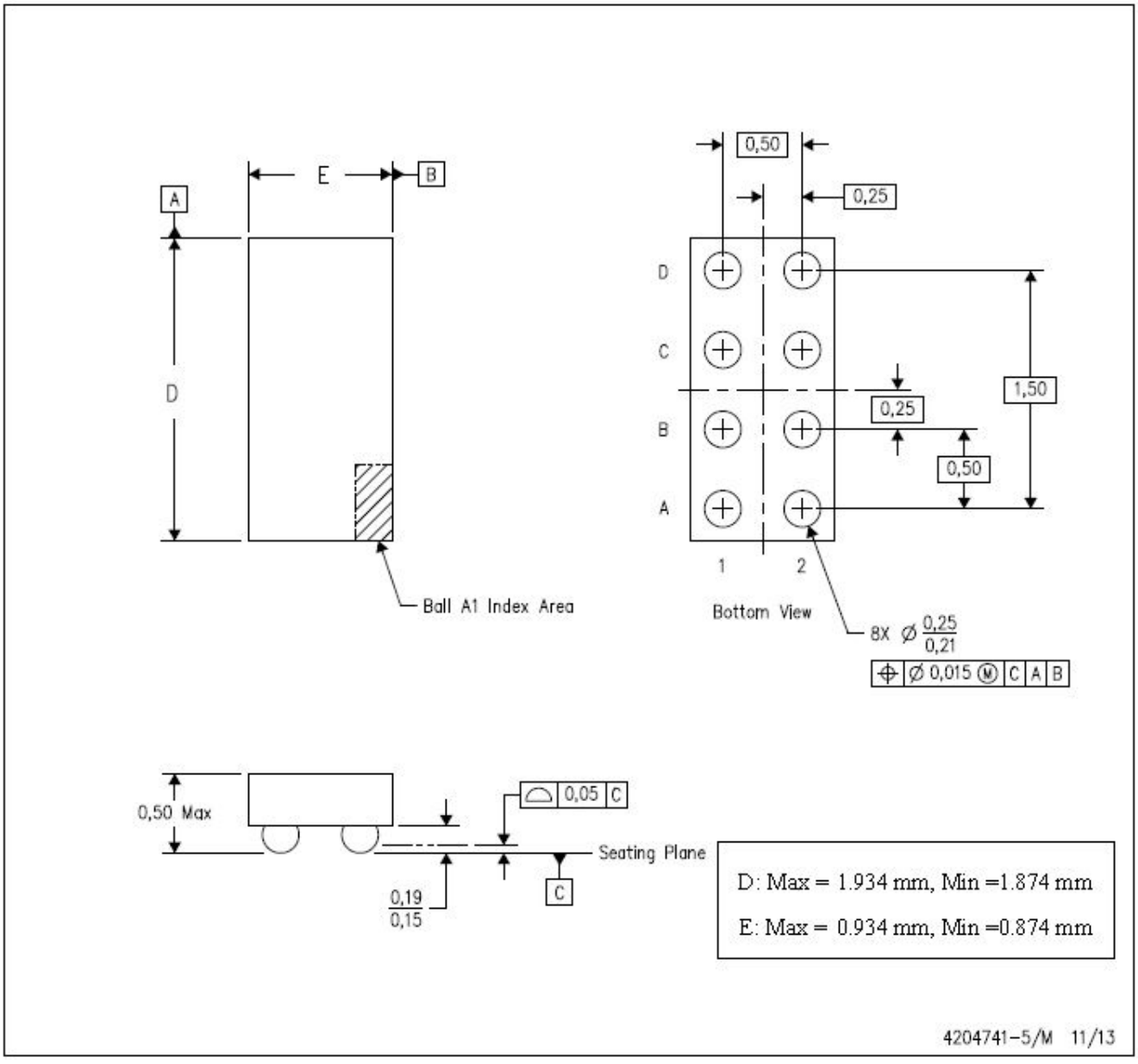
This glossary lists and explains terms, acronyms, and definitions.

ADVANCE INFORMATION

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

YZP (R–XBGA–N8) DIE–SIZE BALL GRID ARRAY



(1) All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

(2) This drawing is subject to change without notice.

(3) NanoFree™ package configuration.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS22971YZPT	ACTIVE	DSBGA	YZP	8	250	TBD	Call TI	Call TI	-40 to 85		Samples
TPS22971YZPR	PREVIEW	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 85	1CKI	
TPS22971YZPT	PREVIEW	DSBGA	YZP	8	250	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 85	1CLI	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
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Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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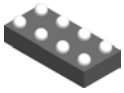
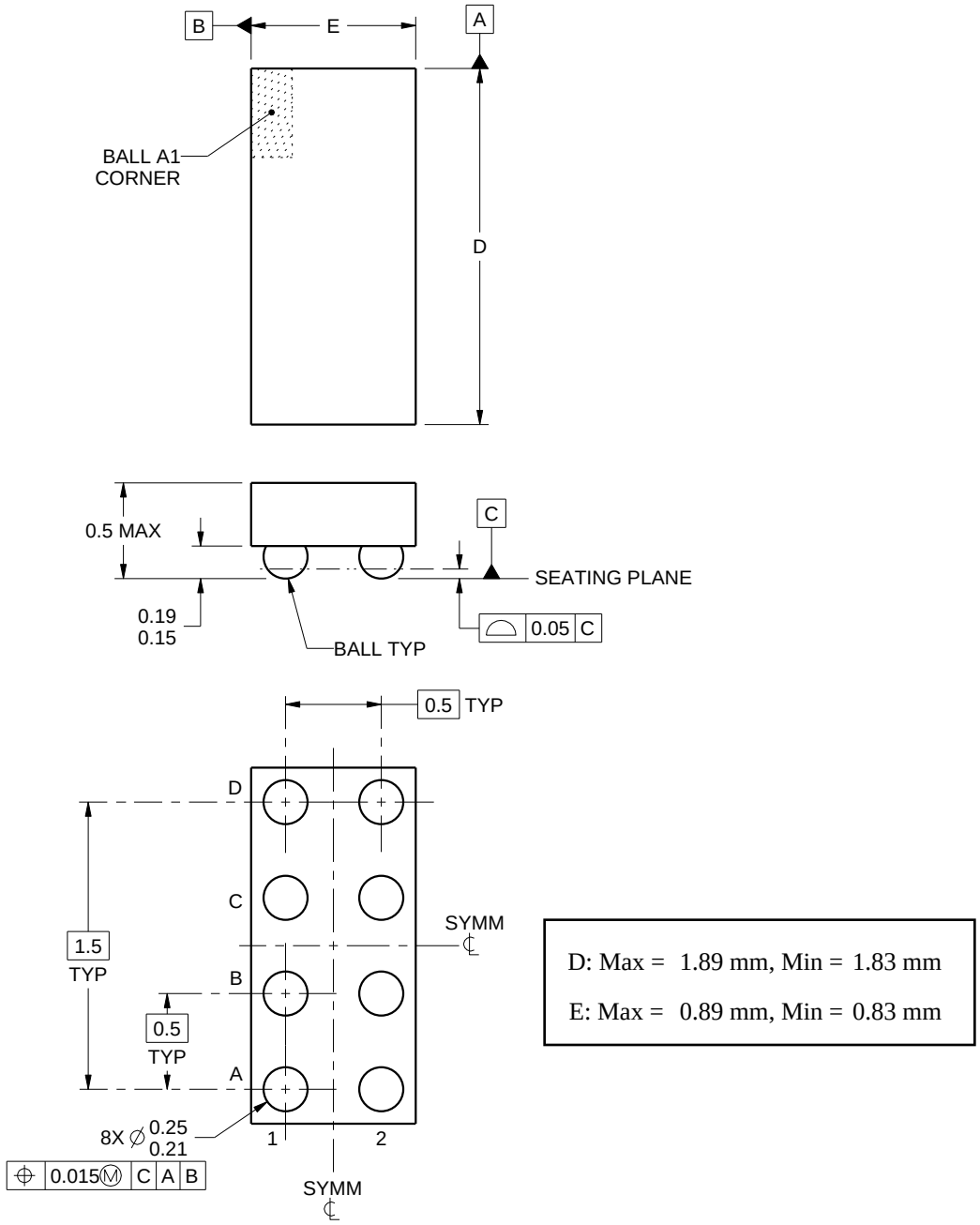


PACKAGE OUTLINE

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



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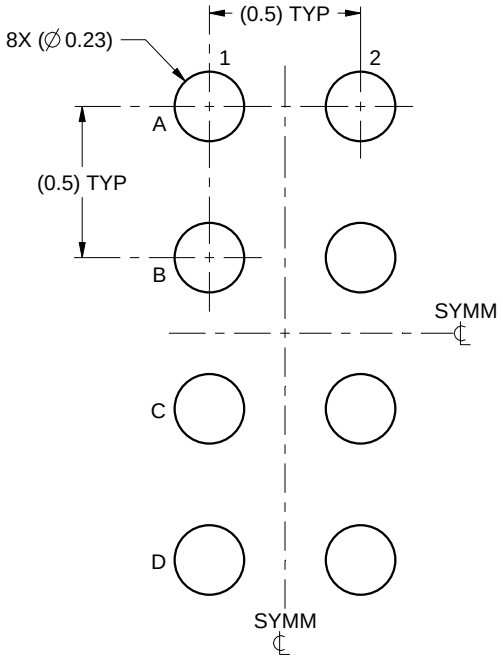
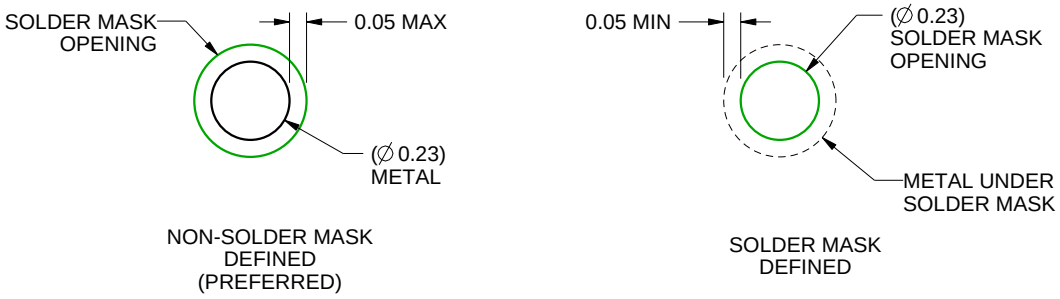
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

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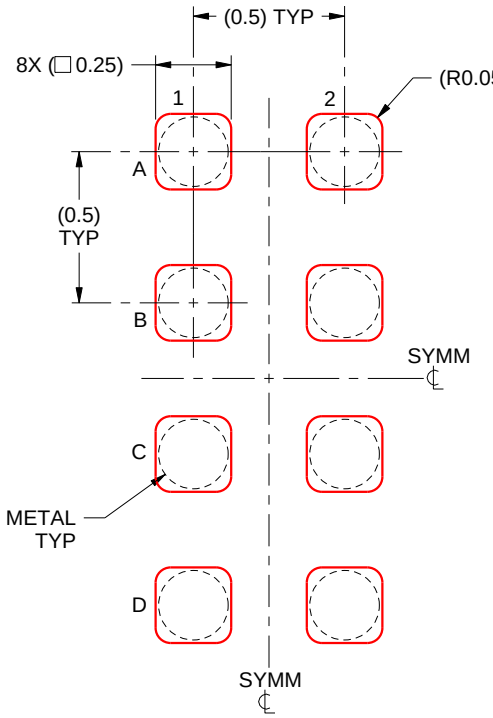
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

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