3V-17V, 300mA Step Down Converter With Adjustable Enable Threshold And Hysteresis

Check for Samples: TPS62125

FEATURES

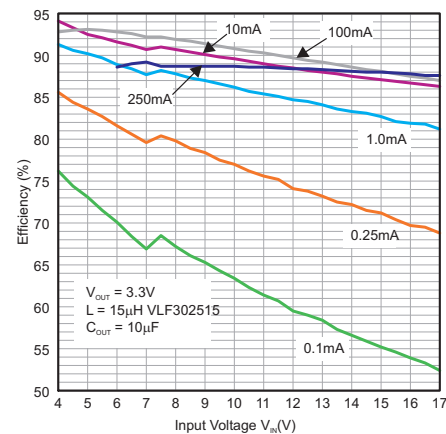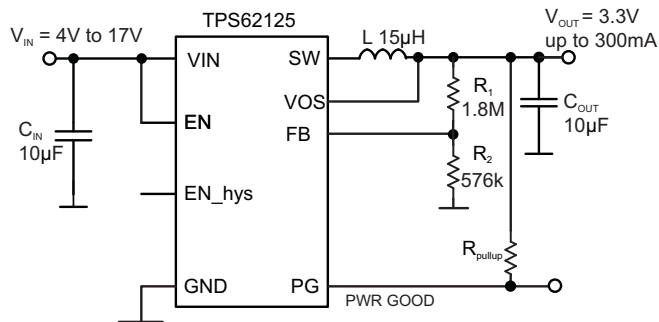- **Wide Input Voltage Range 3V to 17V**
- **Input SVS (Supply Voltage Supervisor) with Adjustable Threshold / Hysteresis Consuming typ. 6µA Quiescent Current**
- **Wide Output Voltage Range 1.2V to 10V**
- **Typ. 13 µA Quiescent Current**
- **350nA typ. Shutdown Current**
- **Seamless Power Save Mode Transition**
- **DCS-Control^{TM} Scheme**
- **Low Output Ripple Voltage**
- **Up to 1MHz Switching Frequency**
- **Highest Efficiency over Wide V$_{IN}$ and V$_{OUT}$ Range**
- **Pin to Pin Compatible with TPS62160/70**
- **100% Duty Cycle Mode**
- **Power Good Open Drain Output**
- **Output Discharge Function**
- **Small 2x2mm^2 SON 8 pin Package**

APPLICATIONS

- **Embedded processing**
- **4 cell alkaline, 1-4 cell Li-Ion battery powered applications**
- **9V - 15V standby power supply**
- **Energy harvesting**
- **Inverter (negative VOUT)**

DESCRIPTION

The TPS62125 is a high efficiency synchronous step down converter optimized for low and ultra low power applications providing up to 300mA output current. The wide input voltage range of 3V to 17V supports four cell alkaline and 1 to 4 cell Li-Ion batteries in series configuration as well as 9V to 15V powered applications. The device includes a precise low power enable comparator which can be used as an input supply voltage supervisor (SVS) to address system specific power up and down requirements. The enable comparator consumes only 6µA quiescent current and features an accurate threshold of 1.2V typical as well as an adjustable hysteresis. With this feature, the converter can generate a power supply rail by extracting energy from a storage capacitor fed from high impedance sources such as solar panels or current loops. With its DCS - Control ^{TM} scheme the converter provides power save mode operation to maintain highest efficiency over the entire load current range. At light loads the converter operates in PFM mode (pulse frequency modulation) and transitions seamlessly and automatically in PWM (pulse width modulation) mode at higher load currents. The DCS - Control^{TM} scheme is optimized for low output ripple voltage in PFM mode in order to reduce output noise to a minimum and features excellent AC load regulation. An open drain power good output indicates once the output voltage is in regulation.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

TA	PART NUMBER[1]	V$_{OUT}$	PACKAGE MARKING
−40°C to 85°C	TPS62125	adjustable	SAQ
	TPS62126[2]	1.8V	TBD

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com
(2) samples available, contact TI for further information

ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Pin voltage range [2]	VIN	- 0.3	20	V
	SW	- 0.3	V$_{IN}$ +0.3V	V
	EN	- 0.3	V$_{IN}$ +0.3V	V
	FB	− 0.3	3.6	V
	VOS, PG	- 0.3	12	V
	EN_hys	− 0.3	7	V
Power Good sink current	I$_{PG}$		10	mA
EN_hys sink current	I$_{EN\_hys}$		3	
ESD rating[3]	HBM Human body model		2	kV
	CDM Charge device model		1	
	Machine model		100	V
Maximum operating junction temperature, T$_J$		−40	125	°C
Storage temperature range, T$_{stg}$		−65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal GND.
(3) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. The machine model is a 200-pF capacitor discharged directly into each pin.

THERMAL INFORMATION

	THERMAL METRIC[1]	TPS62125	UNITS
		DSG	
		8 PINS	
θ$_{JA}$	Junction-to-ambient thermal resistance	65.2	°C/W
θ$_{JC(top)}$	Junction-to-case(top) thermal resistance	93.3	
θ$_{JB}$	Junction-to-board thermal resistance	30.1	
ψ$_{JT}$	Junction-to-top characterization parameter	0.5	
ψ$_{JB}$	Junction-to-board characterization parameter	47.4	
θ$_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	7.2	

(1) For more information about traditional and new thermal metrics, see the *IC PackageThermal Metrics* application report, SPRA953

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage V_{IN}		3		17	V
Output current capability	$3V \leq V_{IN} < 6V$			200	mA
	$6V \leq V_{IN} \leq 17V$			300	
Operating ambient temperature T_A [1], (Unless Otherwise Noted)		−40		85	°C
Operating junction temperature range, T_J		−40		125	°C

(1)   In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$) and the maximum power dissipation of the device in the application ($P_{D(max)}$). see the IC Package Thermal Metrics application report, SPRA953.

ELECTRICAL CHARACTERISTICS

T_A = −40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted), V_{IN} = 12V

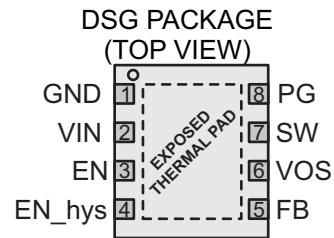| PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range[1]		3.0		17	V
V_{OUT}	Output voltage range		1.2		10	V
I_Q	Quiescent current	I_{OUT} = 0mA, Device not switching, EN = V_{IN}, regulator sleeps		13	23	µA
		I_{OUT} = 0mA, Device switching, V_{IN} = 7.2V, V_{OUT} = 1.2V, L = 22µH		14		µA
		V_{IN} = 5V, EN = 1.1V, enable comparator active, device DC/DC converter off		6	11	
I_{Active}	Active mode current consumption	V_{IN} = 5 V = V_{OUT}, T_A = 25°C, high-side MOSFET switch fully turned on (100% Mode)		230	275	µA
I_{SD}	Shutdown current[2]	Enable comparator off, EN < 0.4V, V_{OUT} = SW = 0 V, V_{IN} = 5V		0.35	2.4	µA
V_{UVLO}	Undervoltage lockout threshold	Falling V_{IN}		2.8	2.85	V
		Rising V_{IN}		2.9	2.95	V
ENABLE COMPARATOR THRESHOLD AND HYSTERESIS (EN, EN_hys)						
$V_{TH EN ON}$	EN pin threshold rising edge		1.16	1.20	1.24	V
$V_{TH EN OFF}$	EN pin threshold falling edge	3.0 V ≤ V_{IN} ≤ 17V	1.12	1.15	1.19	V
$V_{TH EN Hys}$	EN pin hysteresis			50		mV
$I_{IN EN}$	Input bias current into EN pin	EN = 1.3V		0	50	nA
V_{EN_hyst}	EN_hys pin output low	I_{EN_hyst} = 1mA, EN = 1.1V			0.4	V
$I_{IN EN\_hyst}$	Input bias current into EN_hyst pin	EN_hyst = 1.3V		0	50	nA
POWER SWITCH						
$R_{DS(ON)}$	high-side MOSFET on-resistance	V_{IN} = 3 V, I = 100mA		2.4	4	Ω
		V_{IN} = 12V, I = 100mA		1.5	2.6	
	low-side MOSFET on-resistance	V_{IN} = 3V, I = 100mA		0.75	1.3	
		V_{IN} = 12V, I = 100mA		0.6	1	
I_{LIMF}	Switch current limit high-side MOSFET	V_{IN} = 12V	600	750	900	mA
T_{SD}	Thermal shutdown	Increasing junction temperature		150		°C
	Thermal shutdown hysteresis	Decreasing junction temperature		20		°C
OUTPUT						
t_{ONmin}	Minimum ON time	V_{IN} = 5V, V_{OUT} = 2.5 V		500		ns
t_{OFFmin}	Minimum OFF time	V_{IN} = 5 V		60		ns

(1)   The part is functional down to the falling UVLO (Under Voltage Lockout) threshold
(2)   Current into VIN pin

ELECTRICAL CHARACTERISTICS (continued)

T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted), V_{IN} = 12V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF_FB}	Internal reference voltage of error amplifier			0.808		V
V_{FB}	Feedback voltage accuracy	Referred to internal reference (V_{REF_FB})	–2.5	0	2.5	%
	Feedback voltage line regulation	I_{OUT} = 100mA, 5V ≤ V_{IN} ≤ 17V, V_{OUT} = 3.3V [3]		-0.05		%/V
	Feedback voltage load regulation	V_{OUT} = 3.3V; I_{OUT} = 1mA to 300mA, V_{IN} = 12V [3]		-0.004		%/mA
I_{IN_FB}	Input bias current into FB pin	V_{FB} = 0.8 V		0	50	nA
t_{Start}	Regulator start-up time	Time from EN high to device starts switching, V_{IN} = 5V		50		µs
t_{Ramp}	Output voltage ramp time	Time to ramp up V_{OUT} = 1.8V, no load		200		
I_{LK_SW}	Leakage current into SW pin [4]	VOS = V_{IN} = V_{SW} = 1.8 V, EN = GND, device in shutdown mode.		1.8	2.85	µA
I_{IN_VOS}	Bias current into VOS pin			0	50	nA
POWER GOOD OUTPUT (PG)						
V_{TH_PG}	Power Good threshold voltage	Rising V_{FB} feedback voltage	93	95	97	%
		Falling V_{FB} feedback voltage	87	90	93	
V_{OL}	PG pin Output low voltage	Current into PG pin I_{PG}= 0.4mA			0.3	V
V_{OH}	PG pin Output high voltage	Open drain output, external pull up resistor			10	V
I_{IN_PG}	Bias current into PG pin	$V_{(PG)}$ = 3V, EN = 1.3V, FB = 0.85 V		0	50	nA

(3) VOUT = 3.3V, L = 15µH, C_{OUT} = 10µF
(4) An internal resistor divider network with typ. 1MΩ total resistance is connected between SW pin and GND.

DEVICE INFORMATION

PIN ASSIGNMENTS

DSG PACKAGE
(TOP VIEW)

```
GND   1 |  EXPOSED  | 8   PG
VIN   2 |  THERMAL  | 7   SW
EN    3 |    PAD    | 6   VOS
EN_hys 4 |_____| 5   FB
```

PIN FUNCTIONS

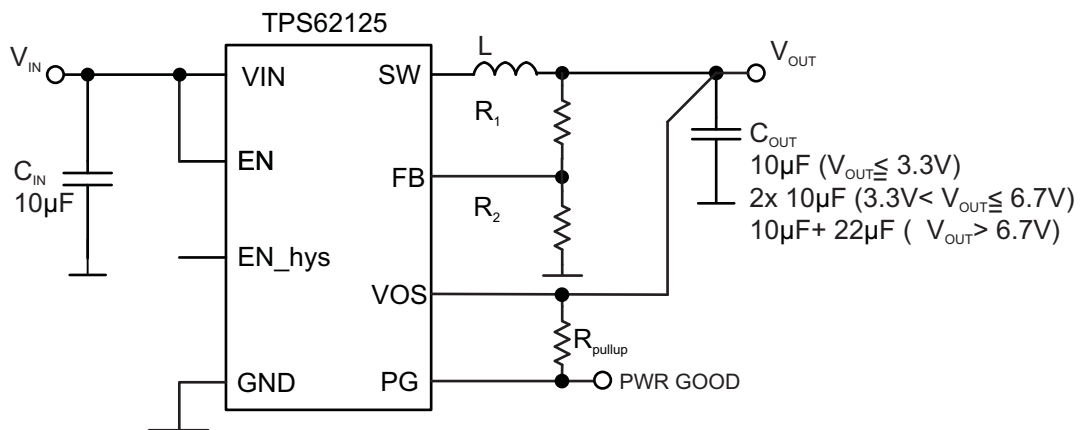| PIN		I/O	DESCRIPTION
NAME	NO.		
GND	1	PWR	GND supply pin.
VIN	2	PWR	V_{IN} power supply pin.
EN	3	IN	Input pin for the enable comparator. Pulling this pin to GND turns the device into shutdown mode. The DC/DC converter is enabled once the rising voltage on this pin trips the enable comparator threshold, $V_{TH\ EN\ ON}$ of typ. 1.2V. The DC/DC converter is turned off once a falling voltage on this pin trips the threshold, $V_{TH\ EN\ OFF}$ of typ. 1.15V. The comparator threshold can be increased by connecting an external resistor to pin EN_hys. See also application section. This pin must be terminated.
EN_hys	4	OUT	Enable Hysteresis Open-Drain Output. This pin is pulled to GND when the voltage on the EN pin is below the comparator threshold $V_{TH\ EN\ ON}$ of typ. 1.2V and the comparator has not yet tripped. The pin is high impedance once the enable comparator has tripped and the voltage at the pin EN is above the threshold $V_{TH\ EN\ ON}$. The pin is pulled to GND once the falling voltage on the EN pin trips the threshold $V_{TH\ EN\ OFF}$ (1.15V typ.). This pin can be used to increase the hysteresis of the enable comparator. If not used, tie this pin to GND, or leave it open.
FB	5	IN	This is the feedback pin for the regulator. An external resistor divider network connected to this pin sets the output voltage. In case of fixed output voltage option, the resistor divider is integrated and the pin need to be connected directly to the output voltage.
VOS	6	IN	This is the output voltage sense pin for the DCS - Control^{TM} circuitry. This pin must be connected to the output voltage of the DC/DC converter.
SW	7	OUT	This is the switch pin and is connected to the internal MOSFET switches. Connect the inductor to this pin. Do not tie this pin to VIN, VOUT or GND.
PG	8	OUT	Open drain power good output. This pin is internally pulled to GND when the device is disabled or the output voltage is below the PG threshold. The pin is floating when the output voltage is in regulation and above the PG threshold. For Power Good indication, the pin van be connected via a pull up resistor to a voltage rail up to 10V. The pin can sink a current up to 0.4mA and maintain the specified high / low voltage levels. It can be used to discharge the output capacitor with up to 10mA. In this case the current into the pin must be limited with an appropriate pull up resistor. More details can be found in the application section. If not used, leave the pin open, or connect to GND.
	Exposed Thermal PAD		Exposed Thermal Pad. This pad must be connected to GND.

FUNCTIONAL BLOCK DIAGRAM

PARAMETER MEASUREMENT INFORMATION

L: LPS3314 10μH, 15μH, LPS4018 22μH, VLF302515 15μH
C_{IN} / C_{OUT}: 10μF 0805/25V GRM21BR61E106
22μF GRM31CR61 16V X5R, 10μF GRM21B 16V X5R

TYPICAL CHARACTERISTICS

Table 1. Table Of Graphs

|	PARAMETER	FIGURE
Efficiency	vs. Output Current V_{OUT} = 1.8V, V_{OUT} = 3.3V, V_{OUT} = 5V, V_{OUT} = 6.8V, V_{OUT} = 8V , V_{OUT} = 10V	Figure 1, Figure 3, Figure 5, Figure 7, Figure 9, Figure 11
	vs. Input Voltage, V_{OUT} = 1.8V, vs. Input voltage, V_{OUT} = 3.3V, V_{OUT} = 5V, V_{OUT} = 6.8V, V_{OUT} = 8V, V_{OUT} = 10V	Figure 2, Figure 4, Figure 6, Figure 8, Figure 10, Figure 12
Output Voltage V_{OUT}	vs. Output Current, V_{OUT} = 3.3V	Figure 13
	vs. Input Voltage, V_{OUT} = 3.3V	Figure 14
	vs. Output current, V_{OUT} = 5.0V	Figure 15
	vs. Input Voltage, V_{OUT} = 5V	Figure 16
	vs. Output current, V_{OUT} = 6.7V	Figure 17
	vs. Input Voltage, V_{OUT} = 6.7V	Figure 18
	vs. Output current, V_{OUT} = 8V	Figure 19
	vs. Input Voltage, V_{OUT} = 8V	Figure 20
peak to peak Output Ripple Voltage V_{OUT}pp	vs. Output Current, V_{OUT} = 3.3V	Figure 21
Switching frequency f_{SW}	vs. Output Current, V_{OUT} = 3.3V	Figure 22
	vs. Output Current, V_{OUT} 5.0V	Figure 23
	vs. Output Current, V_{OUT} = 8V	Figure 24
Shutdown current	vs. Input Voltage	Figure 25
Quiescent Current	vs. Input Voltage	Figure 26
	vs. EN Voltage, rising VEN	Figure 27
	vs. EN Voltage, falling VEN	Figure 28
EN Comparator Thresholds	vs. Input Voltage	Figure 29
R_{DSON}	High Side Switch	Figure 30
	Low Side Switch	Figure 31
Typical Operation	Power Save Mode V_{OUT}=3.3V, I_{OUT} = 1mA	Figure 32
	PWM Mode V_{OUT}= 3.3V, I_{OUT} = 100mA	Figure 33
	Load Transient 5mA to 200mA, V_{OUT} = 3.3V	Figure 34
	AC Load Regulation 5mA to 200mA 10kHz, V_{OUT} = 3.3V	Figure 35
	Load Transient 1mA to 50mA, V_{OUT} = 5V	Figure 36
	Load Transient 10mA to 200mA, V_{OUT} = 5V	Figure 37
	AC Load Regulation V_{OUT} = 5V	Figure 38
Line transient response	V_{IN} = 9V to 12V, I_{OUT} = 100mA	Figure 39
Hotplug	V_{IN} overshoot exceeding Abs Max ratings	Figure 40
	V_{IN} overshoot reduction with additional tantalum polymer capacitor	Figure 41
Short circuit and overcurrent protection		Figure 42
Input SVS Operation	V_{OUT} = 5.0V	Figure 43
No Input SVS Operation	V_{OUT} = 5.0V, V_{IN} tracks V_{OUT}	Figure 44
Operation from a 0.5mA current source	V_{OUT} 3.3V, 20mA pulse load	Figure 45
Startup	1.8V V_{OUT}	Figure 46
	3.3V V_{OUT}	Figure 47
	5V V_{OUT}	Figure 48
	8V V_{OUT}	Figure 49
EN On/Off		Figure 50
Output Discharge	using PG pin, triggered by EN Comparator	Figure 51
	V_{OUT} ramp down with falling VIN	Figure 52
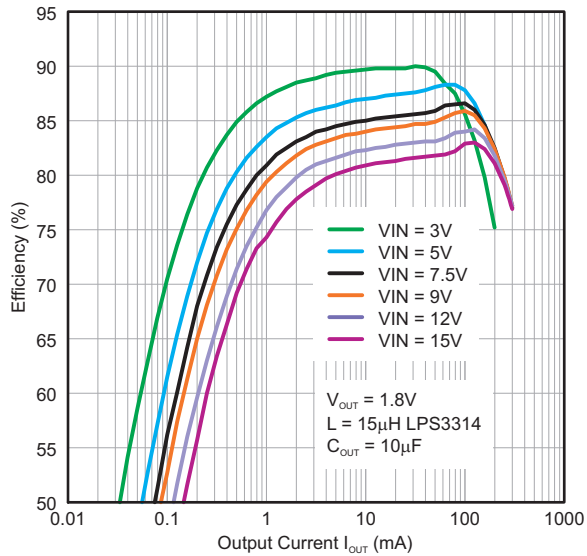
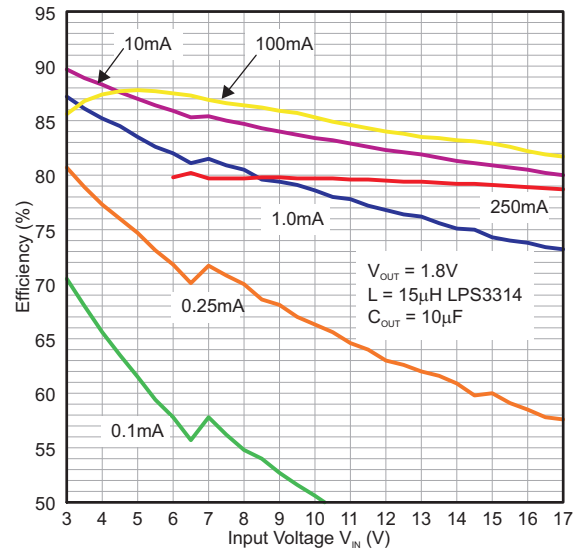**Figure 1. Efficiency vs. Output Current V$_{OUT}$ = 1.8V**

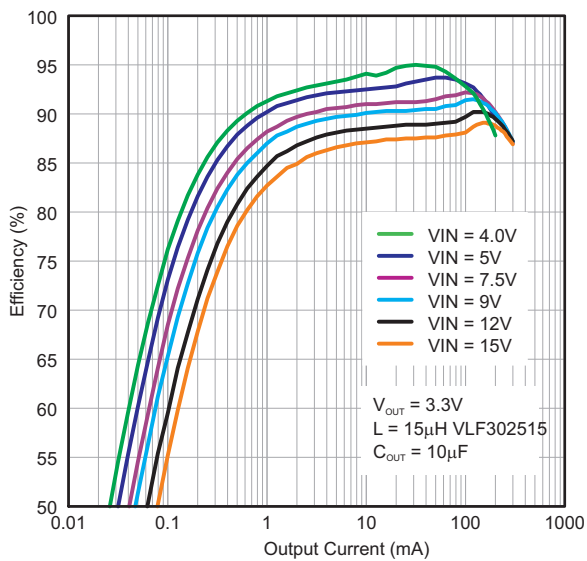**Figure 2. Efficiency vs. Input Voltage, V$_{OUT}$ = 1.8V**

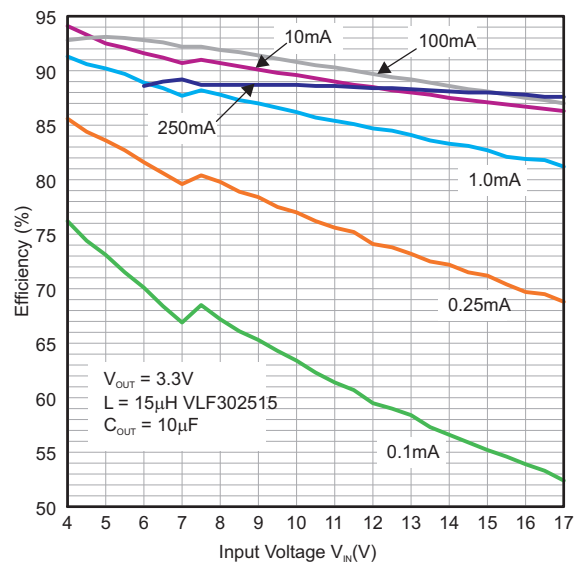**Figure 3. Efficiency vs. Output current, V$_{OUT}$ = 3.3V**

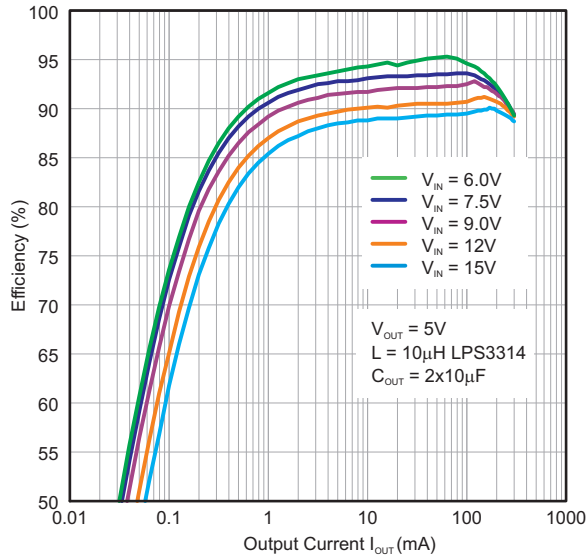**Figure 4. Efficiency vs. Input voltage, V$_{OUT}$ = 3.3V**

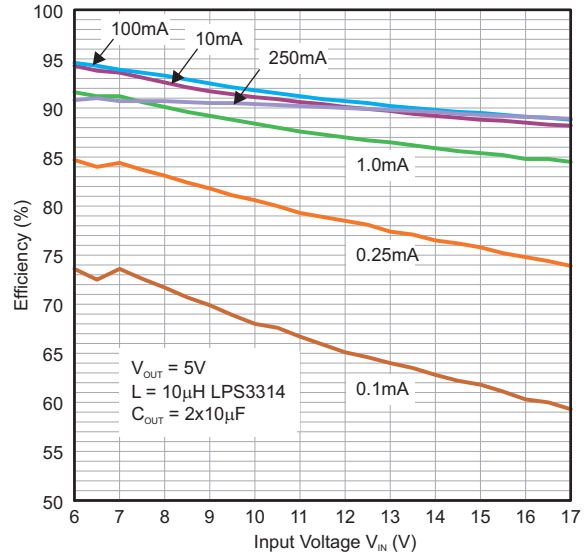**Figure 5. Efficiency vs. Output Current, V_OUT = 5V**

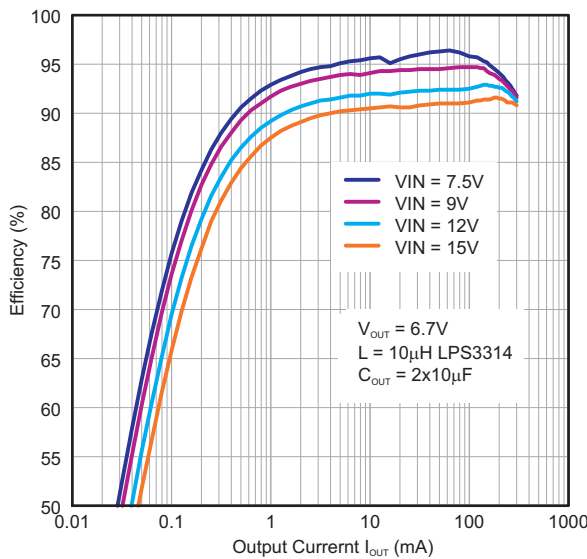**Figure 6. Efficiency vs. Input Voltage, V_OUT = 5V**
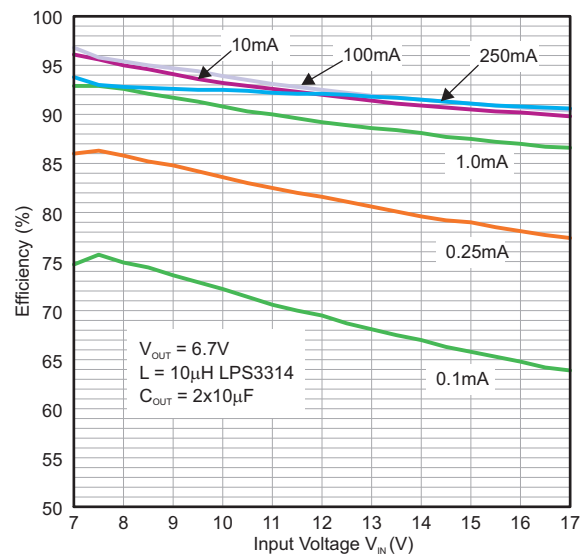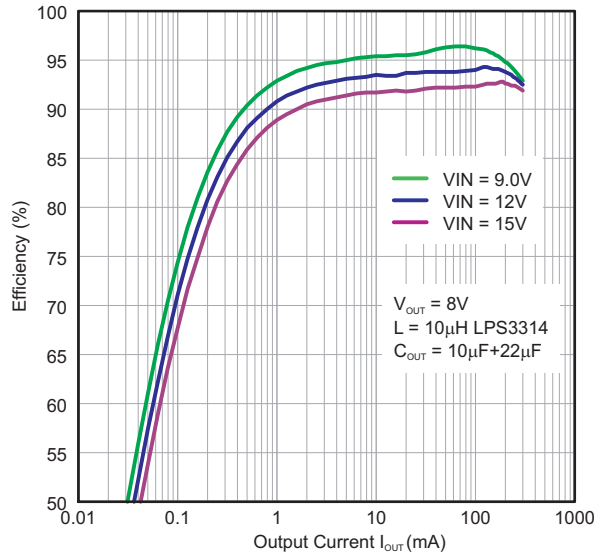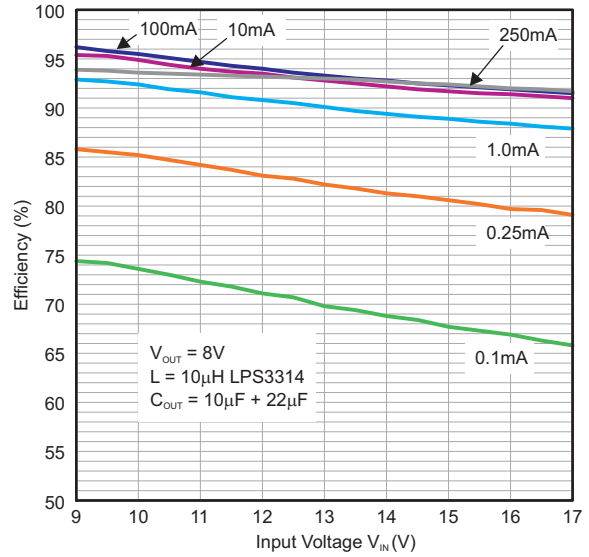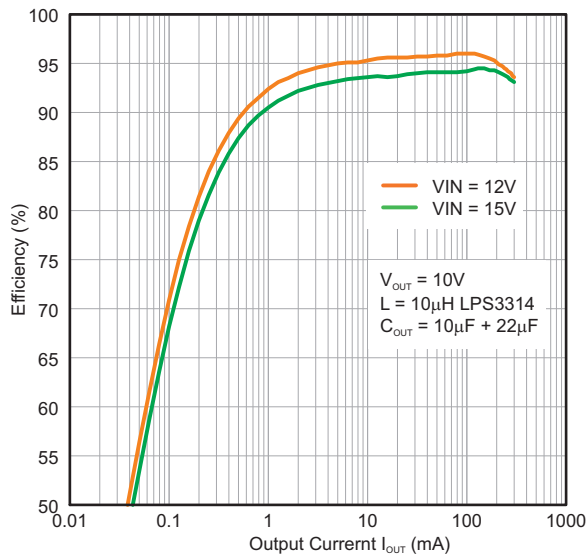

Figure 7. Efficiency vs. Output current, V_OUT = 6.8V

Figure 8. Efficiency vs. Input Voltage, V_OUT = 6.8V

Figure 9. Efficiency vs. Output Current, V_{OUT} = 8V

Figure 10. Efficiency vs. Input Voltage, V_{OUT} = 8V

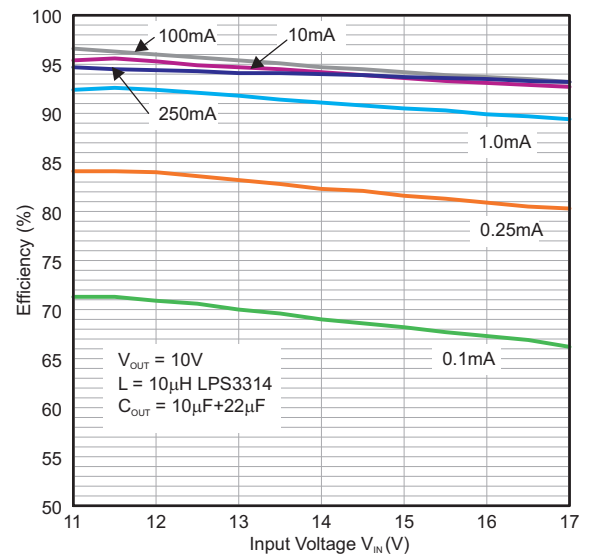Figure 11. Efficiency vs. Output Current, V_{OUT} = 10V

Figure 12. Efficiency vs. Input Voltage, V_{OUT} = 10V
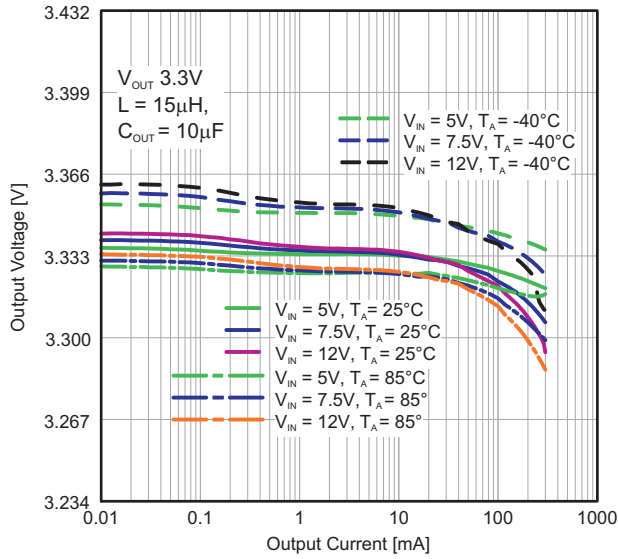
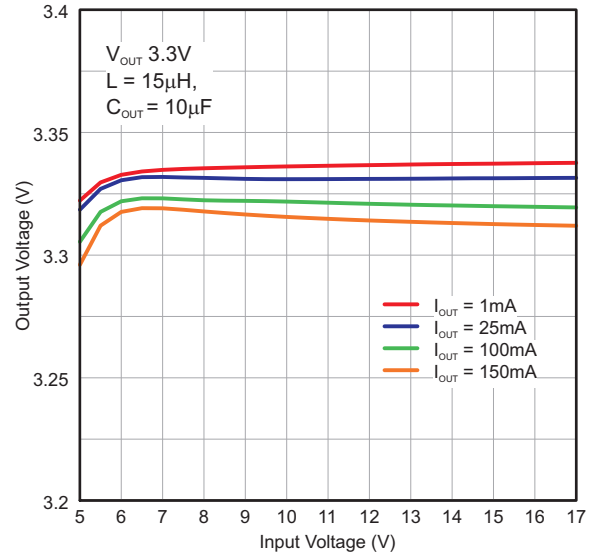**Figure 13. Output Voltage vs. Output Current, V$_{OUT}$ = 3.3V**

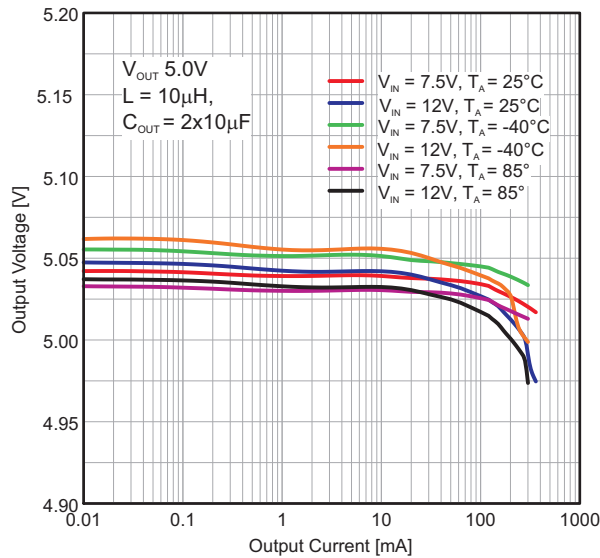**Figure 14. Output Voltage vs. Input Voltage, V$_{OUT}$ = 3.3V**

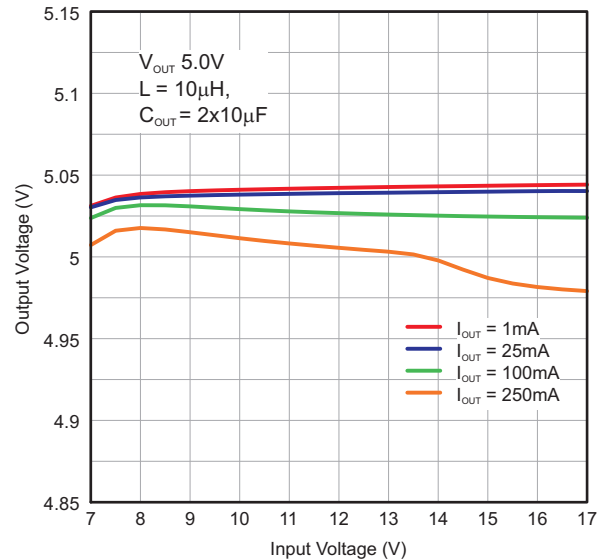**Figure 15. Output Voltage vs. Output current, V$_{OUT}$ = 5.0V**

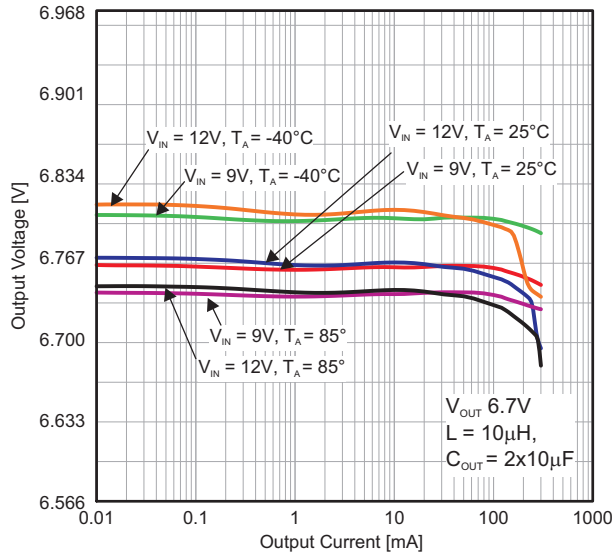**Figure 16. Output Voltage vs. Input Voltage, V$_{OUT}$ = 5V**

Figure 17. Output Voltage vs. Output Current, V_OUT = 6.7V
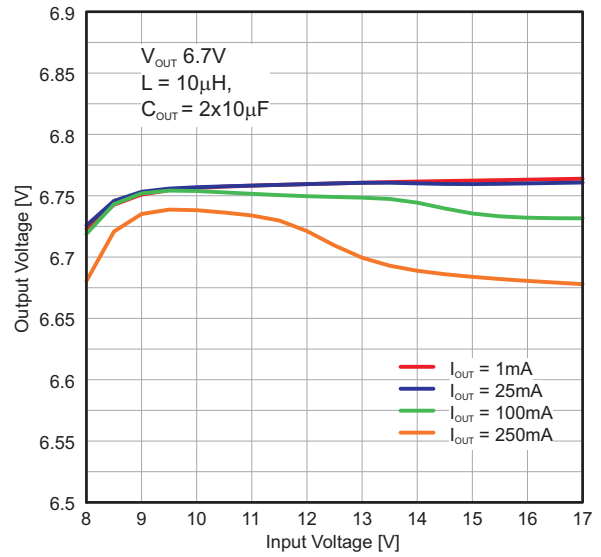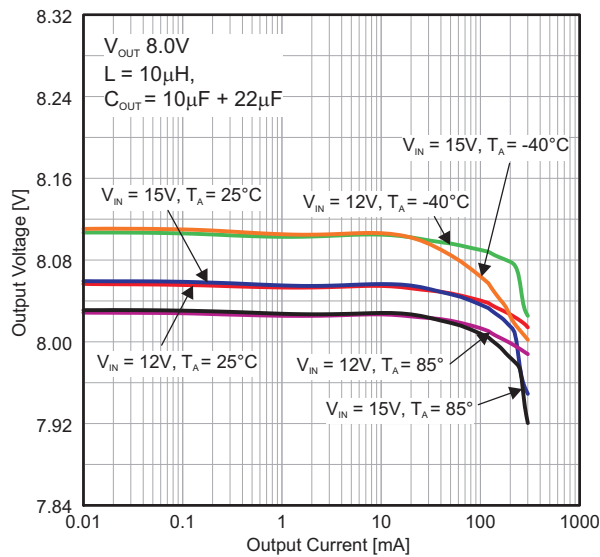

Figure 18. Output voltage vs. Input voltage, V_OUT = 6.7V

Figure 19. Output Voltage vs. Output Current, V_OUT = 8V
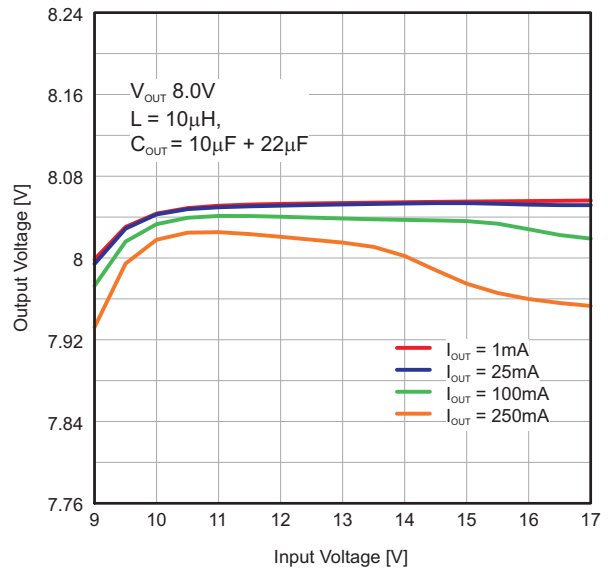
Figure 20. Output Voltage vs. Input Voltage, V_OUT = 8V

Product Folder Link(s) : *TPS62125*
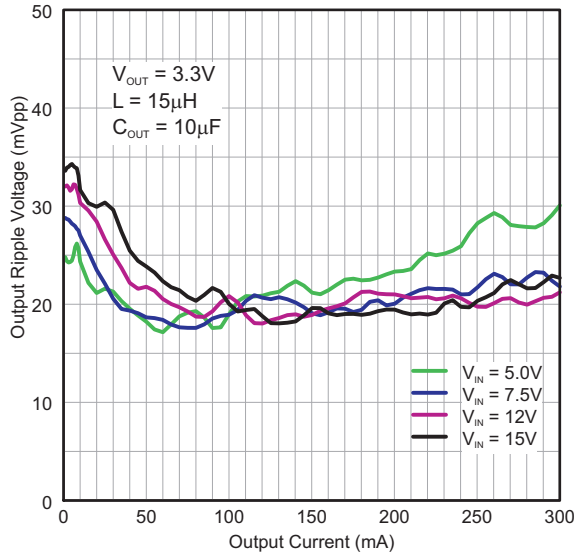
Figure 21. Output Ripple Voltage vs. Output Current, V$_{OUT}$ = 3.3V
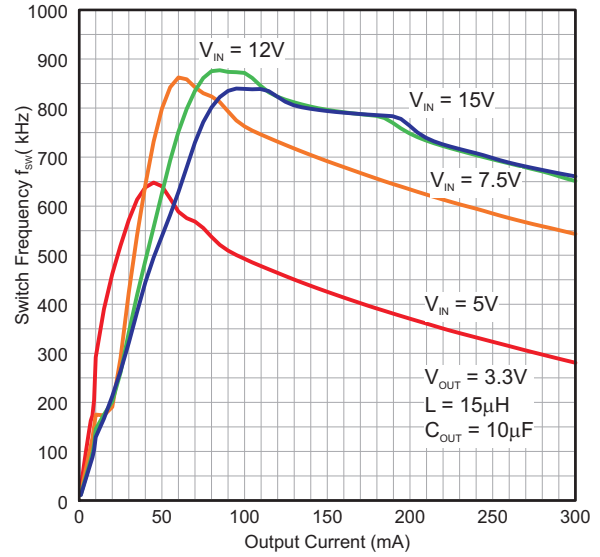
Figure 22. Switch Frequency vs. Output Current, V$_{OUT}$ = 3.3V
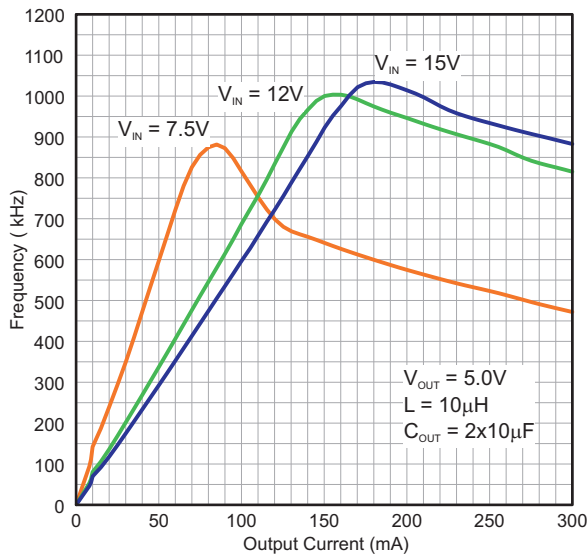
Figure 23. Switch Frequency vs. Output Current, V$_{OUT}$ 5.0V
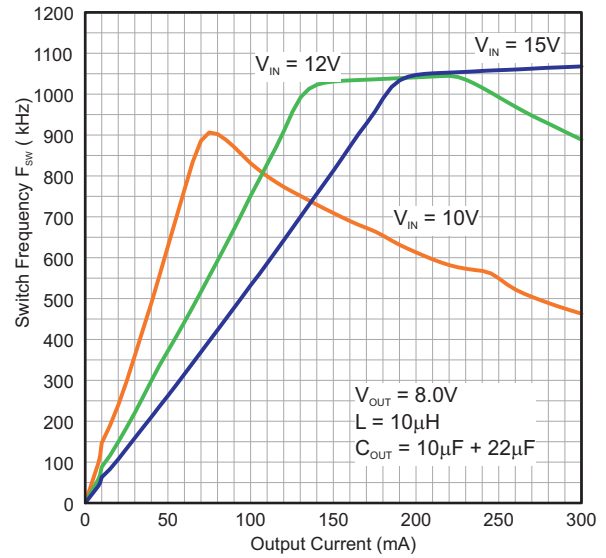
Figure 24. Switch Frequency vs. Output Current, V$_{OUT}$ = 8V

Product Folder Link(s) :*TPS62125*
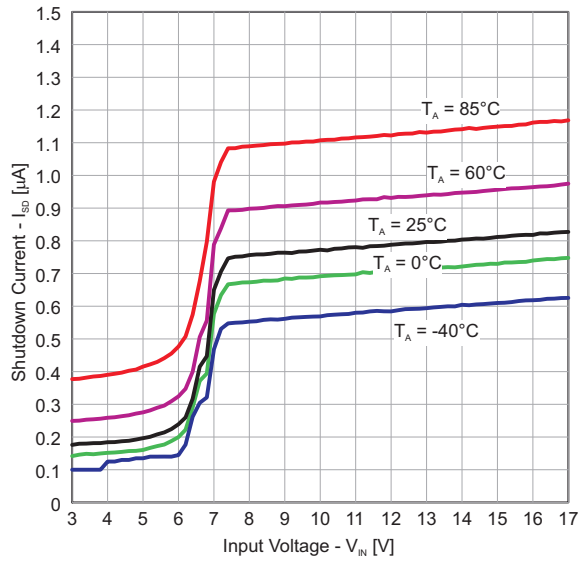
Figure 25. Shutdown Current vs. Input Voltage
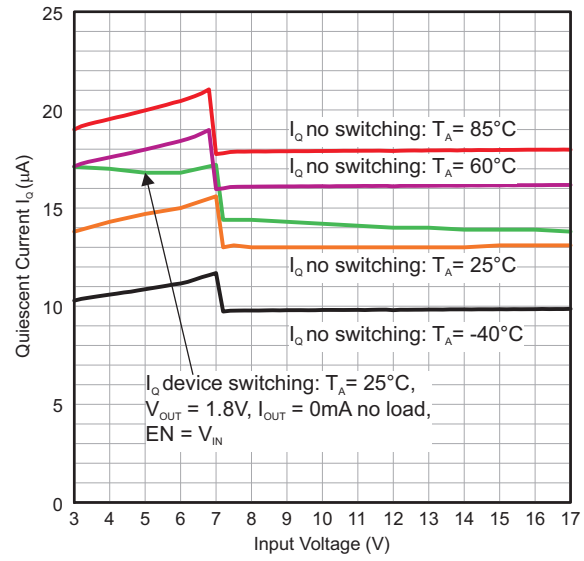
Figure 26. Quiescent Current vs. Input Voltage
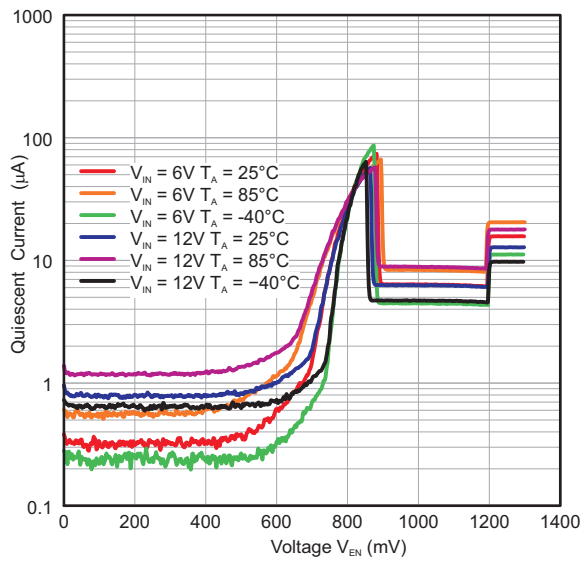
Figure 27. Quiescent Current vs. EN Voltage, rising V$_{EN}$
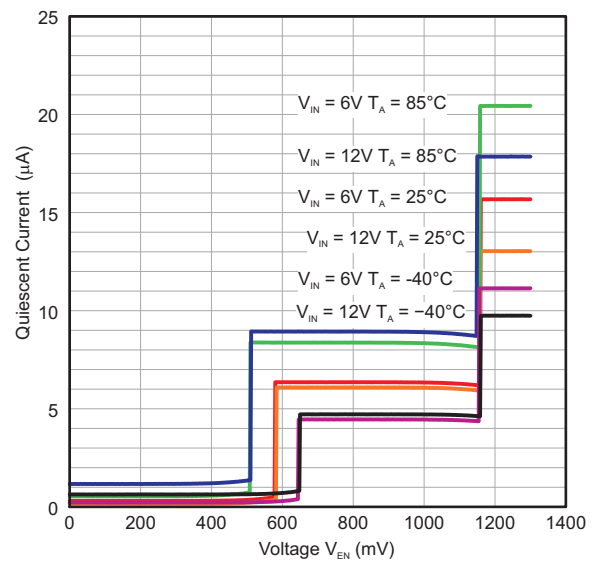
Figure 28. Quiescent Current vs. V$_{EN}$ Voltage, falling V$_{EN}$
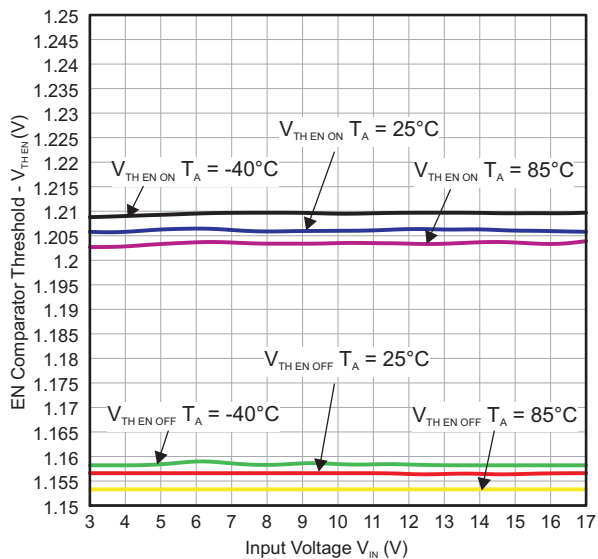
Figure 29. EN Comparator Thresholds vs. Input Voltage
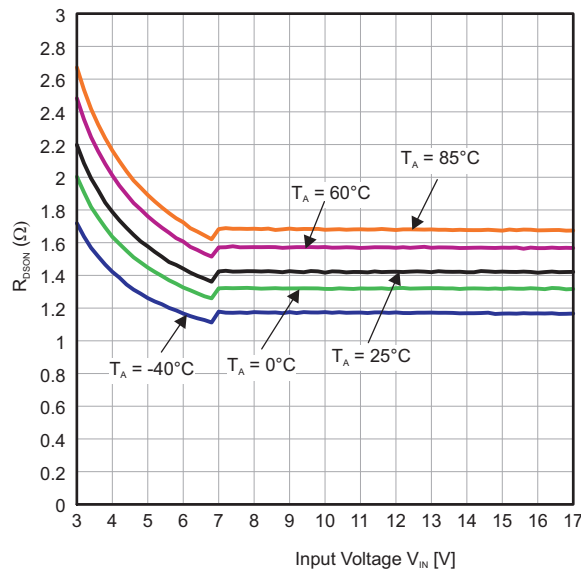
Figure 30. R$_{DSON}$ High Side Switch
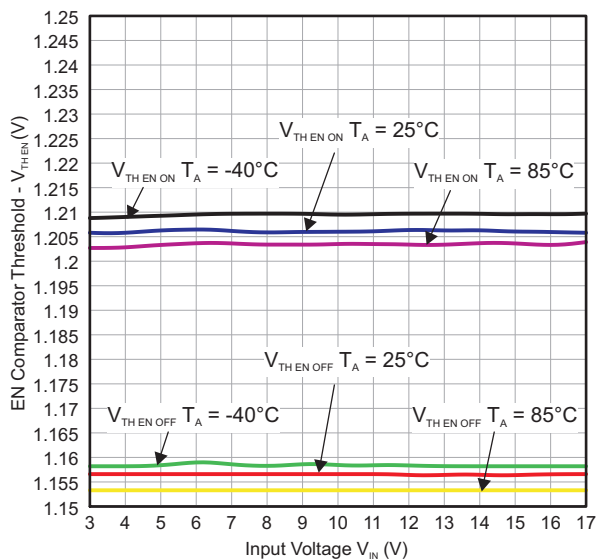
Figure 31. R$_{DSON}$ Low Side Switch (Rectifier)
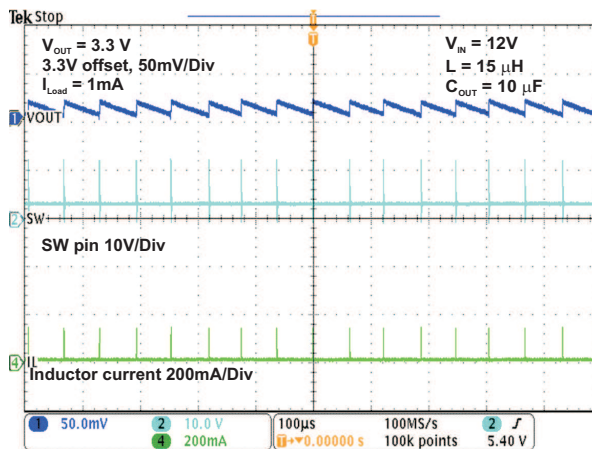
Figure 32. Power Save Mode V$_{OUT}$=3.3V, I$_{OUT}$ = 1mA
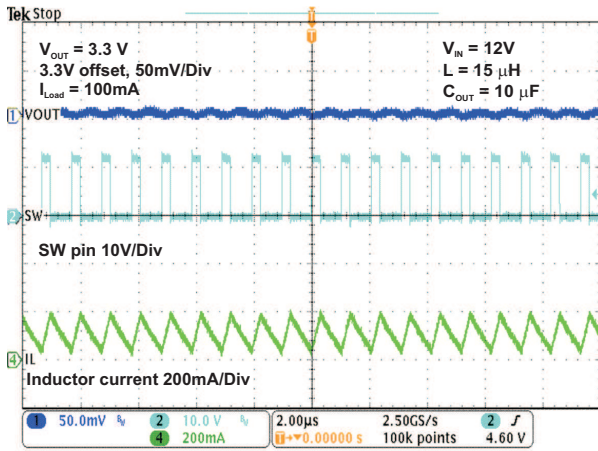
Figure 33. PWM Mode V$_{OUT}$= 3.3V, I$_{OUT}$ = 100mA
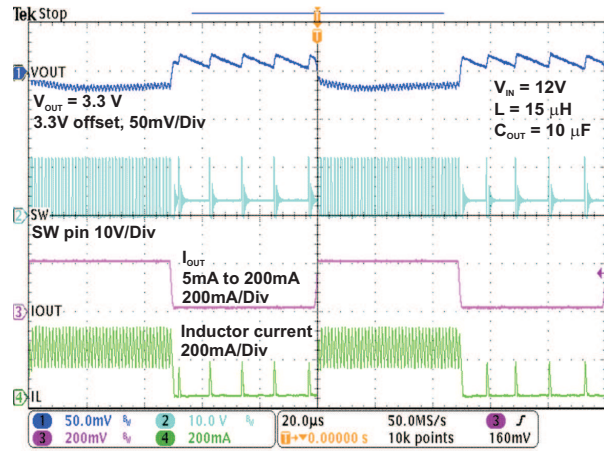
Figure 34. Load Transient 5mA to 200mA, V$_{OUT}$ = 3.3V
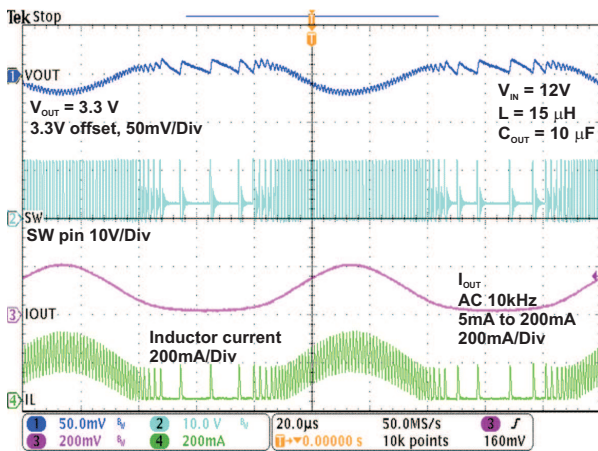
Figure 35. AC Load Regulation, V$_{OUT}$ = 3.3V
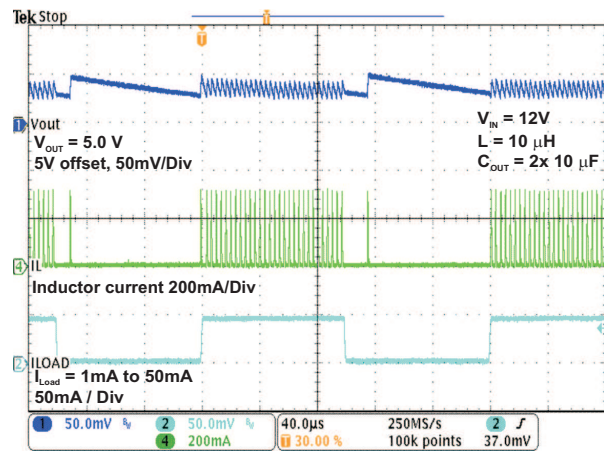
Figure 36. Load Transient 1mA to 50mA, V$_{OUT}$ = 5V
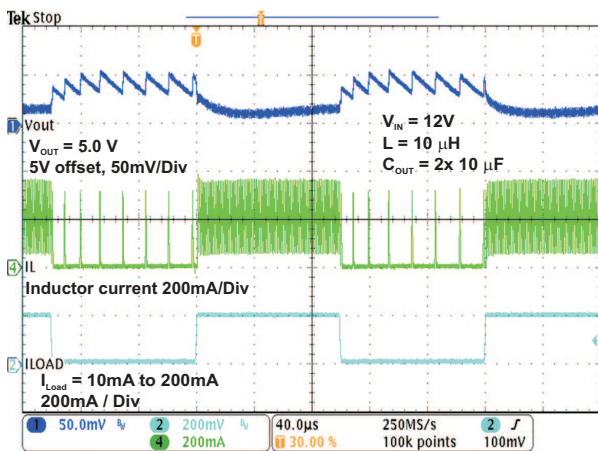
Figure 37. Load Transient 10mA to 200mA, V$_{OUT}$ = 5V
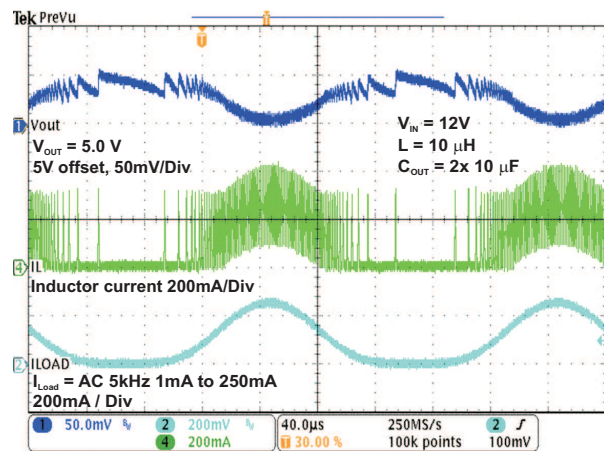
Figure 38. AC Load Regulation V$_{OUT}$ = 5V
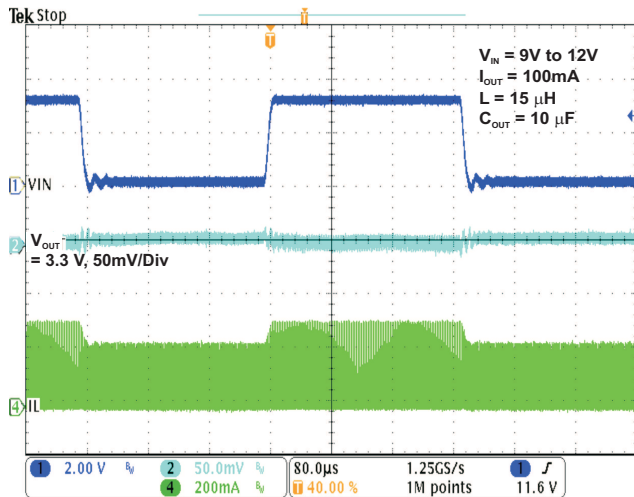
Figure 39. Line transient response V_{IN} = 9V to 12V
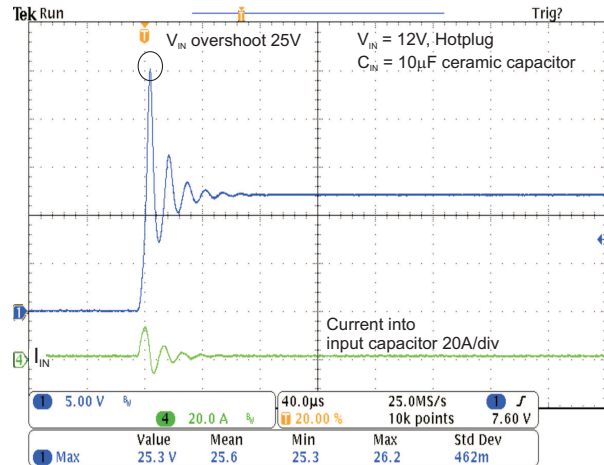
Figure 40. V_{IN} Hotplug overshoot
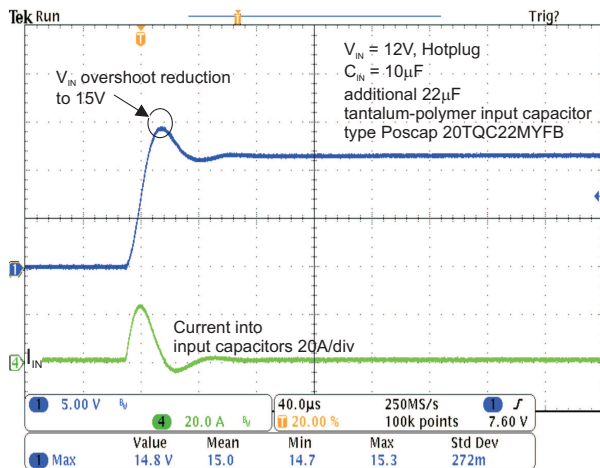
Figure 41. V_{IN} Hotplug overshoot reduction with Poscap
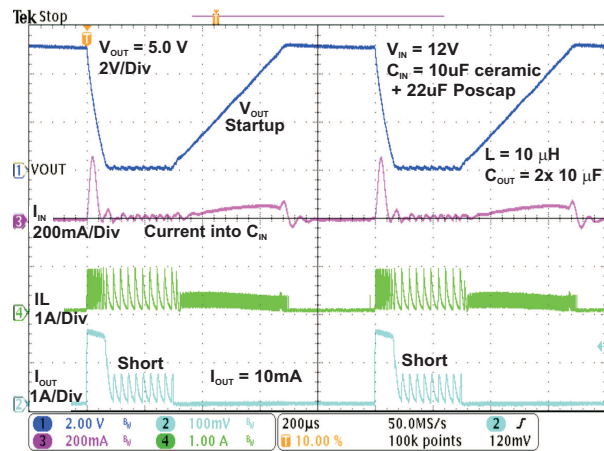
Figure 42. Short circuit and overcurrent protection

Product Folder Link(s) :TPS62125
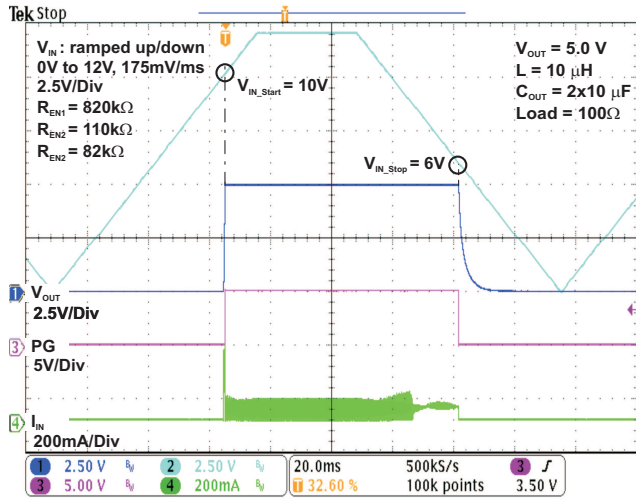
Figure 43. Input supply voltage supervisor (SVS), V_{OUT} = 5.0V
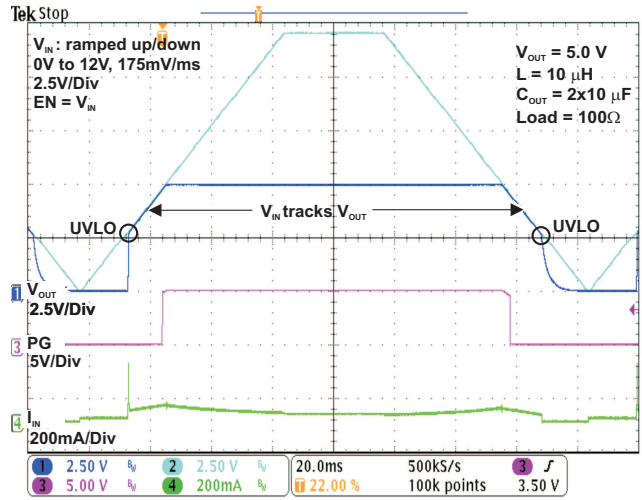
Figure 44. Operation with EN = V_{IN}, V_{IN} tracks V_{OUT}
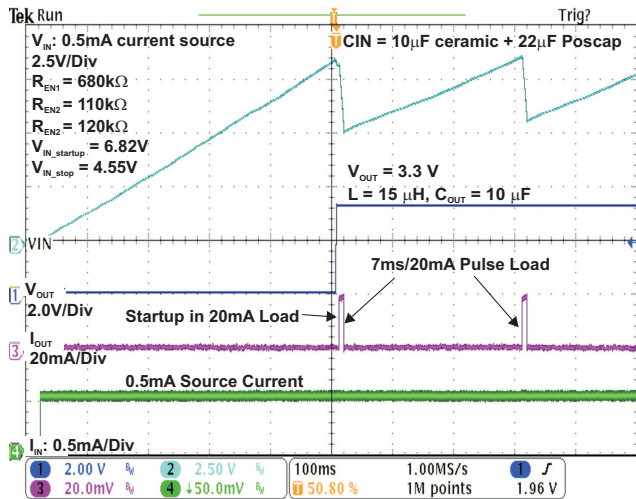
Figure 45. 0.5mA current source, 20mA pulse load
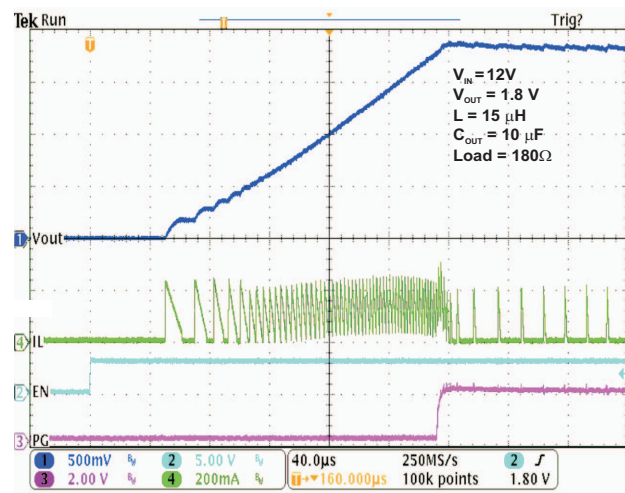
Figure 46. Startup 1.8V V_{OUT}

Product Folder Link(s) : *TPS62125*
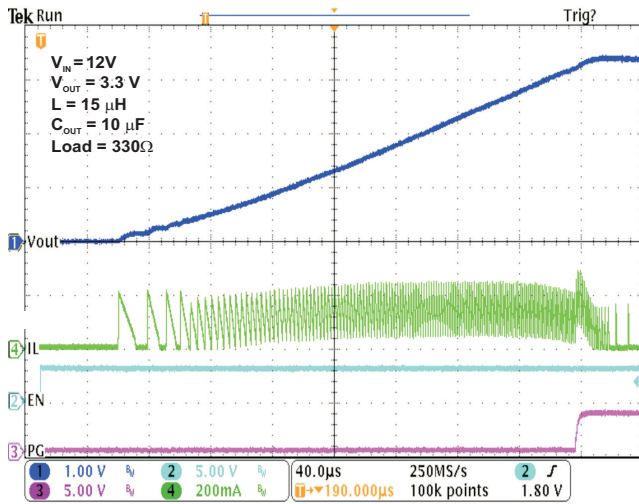
Figure 47. Startup 3.3V V$_{OUT}$
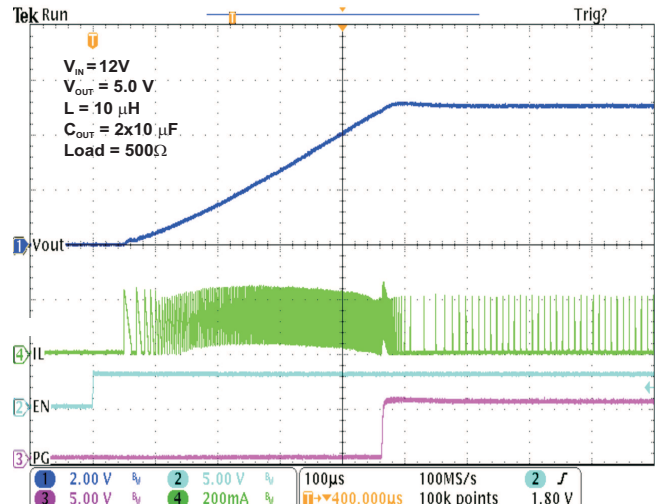
Figure 48. Startup 5.0V V$_{OUT}$
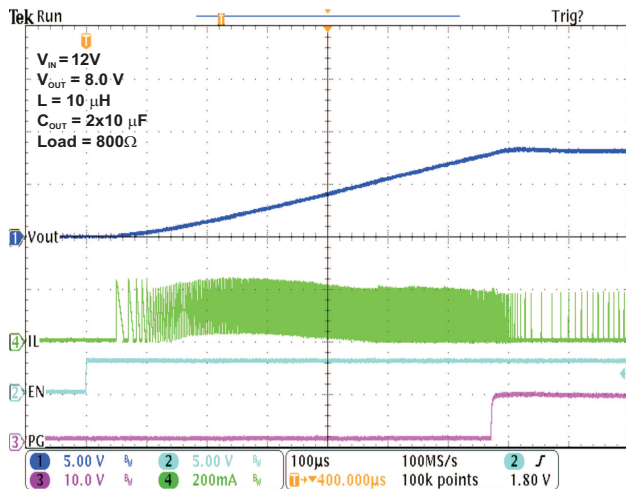
Figure 49. Startup 8V V$_{OUT}$
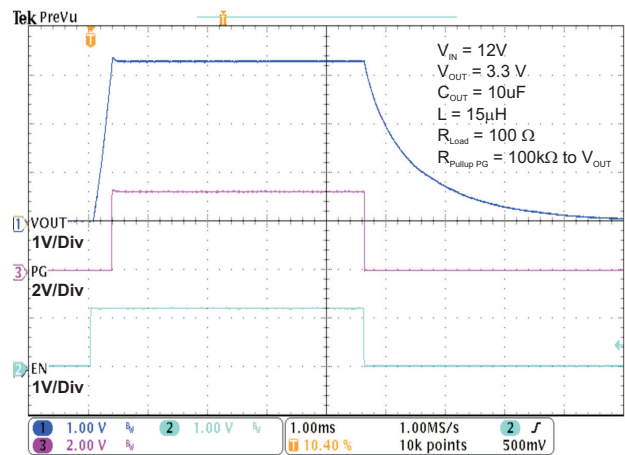
Figure 50. V$_{OUT}$ Ramp up/down with EN on/off
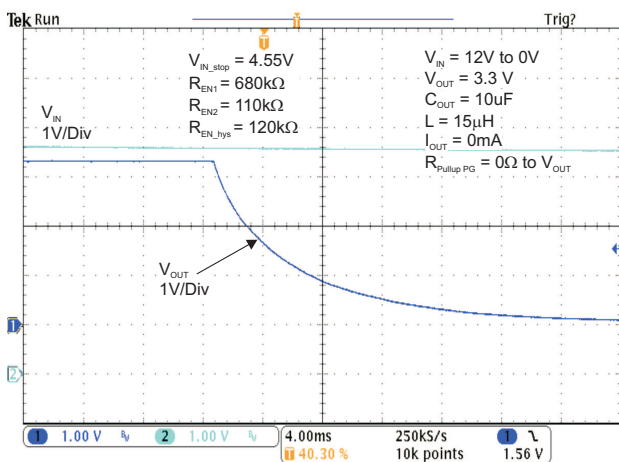
Figure 51. Output discharge using PG pin, triggered by EN Comparator
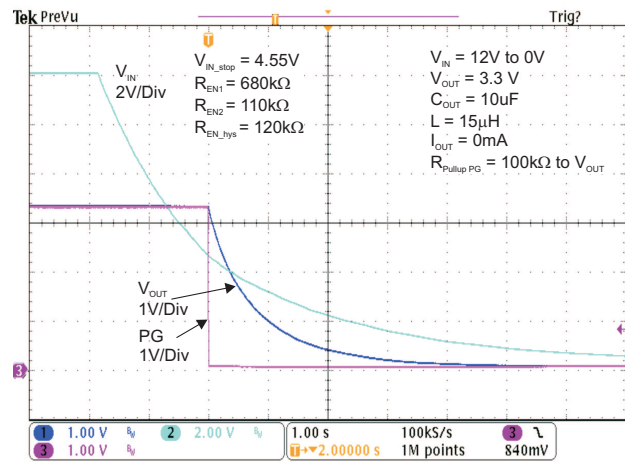
Figure 52. V$_{OUT}$ ramp down with falling V$_{IN}$, schematic Figure Figure 60

DETAILED DESCRIPTION

DCS - Control[TM]

The TPS62125 high efficiency synchronous switch mode buck converter includes TI's DCS - Control™ (Direct Control with Seamless Transition into Power Save Mode), an advanced regulation topology, which combines the advantages of hysteretic and voltage mode control. Characteristics of DCS - Control[TM] are excellent AC load regulation and transient response, low output ripple voltage and a seamless transition between PFM and PWM mode operation.

DCS - Control[TM] includes an AC loop which senses the output voltage (VOS pin) and directly feeds the information to a fast comparator stage. This comparator sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. In order to achieve accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors. The DCS - Control[TM] topology supports PWM (Pulse Width Modulation) mode for medium and high load conditions and a Power Save Mode at light loads. During PWM mode, it operates in continuous conduction. The switch frequency is up to 1MHz with a controlled frequency variation depending on the input voltage. If the load current decreases, the converter seamless enters Power Save Mode to maintain high efficiency down to very light loads. In Power Save Mode the switching frequency varies linearly with the load current. Since DCS - Control[TM] supports both operation modes within one single building block, the transition from PWM to Power Save Mode is seamless without effects on the output voltage. The TPS62125 offers both excellent DC voltage and superior load transient regulation, combined with very low output voltage ripple, minimizing interference with RF circuits.

At high load currents the converter operates in quasi fixed frequency PWM mode operation and at light loads in PFM (Pulse Frequency Modulation) mode to maintain highest efficiency over the full load current range. In PFM Mode, the device generates a single switching pulse to ramp up the inductor current and recharge the output capacitor, followed by a sleep period where most of the internal circuits are shutdown to achieve a quiescent current of typically 13µA. During this time, the load current is supported by the output capacitor. The duration of the sleep period depends on the load current and the inductor peak current.

Pulse Width Modulation (PWM) Operation

The TPS62125 operates with pulse width modulation in continuous conduction mode (CCM) with a nominal switching frequency of about 1MHz. The frequency variation in PWM mode is controlled and depends on VIN, VOUT and the inductance. The device operates in PWM mode as long the output current is higher than half the inductor's ripple current. To maintain high efficiency at light loads, the device enters Power Save Mode at the boundary to discontinuous conduction mode (DCM). This happens if the output current becomes smaller than half the inductor's ripple current.

Power Save Mode

With decreasing load current, the TPS62125 transitions seamlessly from PWM Mode to Power Save Mode once the inductor current becomes discontinuous. This ensures a high efficiency at light loads. In Power Save Mode the converter operates in Pulse Frequency Modulation (PFM Mode) and the switching frequency decreases linearly with the load current. DCS - Control[TM] features a small and predictable output voltage ripple in Power Save Mode. The transition between PWM Mode and Power Save Mode occurs seamlessly in both directions.

The minimum On Time T_{ONmin} for a single pulse can be estimated by:

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \times 1\mu s$$

(1)

Therefore the peak inductor current in PFM mode is approximately:

$$I_{LPFMpeak} = \frac{(V_{IN} - V_{OUT})}{L} \times T_{ON}$$

(2)

The transition from PFM mode to PWM mode operation and back occurs at a load current of approximately ½ $I_{LPFMpeak}$.

With:

T_{ON}: high-side MOSFET switch on time [µs]

V_{IN}: Input voltage [V]

V_{OUT}: Output voltage [V]

L : Inductance [µH]

$I_{LPFMpeak}$: PFM inductor peak current [mA]

The maximum switching frequency can be estimated by:

$$f_{SW\,max} \approx \frac{1}{1\mu s} = 1MHz$$

(3)

100% DUTY CYCLE LOW DROPOUT OPERATION

The device increases the On Time of the high-side MOSFET switch as the input voltage comes close to the output voltage in order to keep the output voltage in regulation. This reduces the switching frequency.

With further decreasing input voltage VIN, the high-side MOSFET switch is turned on completely. In this case, the converter provides a low input-to-output voltage difference. This is particularly useful in applications with a widely variable supply voltage to achieve longest operation time by taking full advantage of the whole supply voltage span.

The minimum input voltage to maintain output voltage regulation depends on the load current and output voltage, and can be calculated as:

$$V_{Imin} = V_{OUT\,min} + I_{OUT} \times (R_{DSON\,max} + R_L)$$

(4)

With:

I_{OUT} = output current

$R_{DS(ON)max}$ = maximum high side switch $R_{DS(ON)}$.

R_L = DC resistance of the inductor

V_{OUTmin} = minimum output voltage the load can accept

UNDER-VOLTAGE LOCKOUT

In addition to the EN Comparator, the device includes an under-voltage lockout circuit which prevents the device from misoperation at low input voltages. Both circuits are fed to an AND gate and prevents the converter from turning on the high-side MOSFET switch or low-side MOSFET under undefined conditions. The UVLO threshold is set to 2.9V typical for rising V_{IN} and 2.8V typical for falling V_{IN}. The hysteresis between rising and falling UVLO threshold ensures proper start up. Fully functional operation is permitted for an input voltage down to the falling UVLO threshold level. The converter starts operation again once the input voltage trips the rising UVLO threshold level and the voltage at the EN pin trips $V_{TH\_EN\_ON}$.

SOFT START

The TPS62125 has an internal soft-start circuit which controls the ramp up of the output voltage and limits the inrush current during start-up. This limits input voltage drop.

The soft-start system generates a monotonic ramp up of the output voltage and reaches an output voltage of 1.8V typ. within 240µs after the EN pin was pulled high. For higher output voltages, the ramp up time of the output voltage can be estimated with a ramp up slew rate of about 12mV/us. TPS62125 is able to start into a pre biased output capacitor. The converter starts with the applied bias voltage and ramps the output voltage to its nominal value. In case the output voltage is higher than the nominal value, the device starts switching once the output has been discharged by an external load or leakage current to its nominal output voltage value.

During start up the device can provide an output current of half of the high-side MOSFET switch current limit I_{LIMF}. Large output capacitors and high load currents may exceed the current capability of the device during start up. In this case the start up ramp of the output voltage will be slower.

ENABLE COMPARATOR (EN / EN_hys)

The EN pin is connected to an On/Shutdown detector (ON/SD) and an input of the Enable Comparator. With a voltage level of 0.4V or less at the EN pin, the ON/SD detector turns the device into Shutdown mode and the quiescent current is reduced to typically 350nA. In this mode the EN comparator as well the entire internal-control circuitry are switched off. A voltage level of typ. 900mV (rising) at the EN pin triggers the ON/Shutdown detector and activates the internal reference VREF (Typ.1.2V), the EN comparator and the UVLO comparator. In applications with slow rising voltage levels at the EN pin, the quiescent current profile before this trip point needs to be considered, see Figure 27. Once the ON/SD detector has tripped, the quiescent current consumption of the device is typ. 6µA. The TPS62125 starts regulation once the voltage at the EN pin trips the threshold $V_{EN\_TH\ ON}$ (typ. 1.2V) and the input voltage is above the UVLO threshold. It enters softstart and ramps up the output voltage. For proper operation, the EN pin must be terminated and must not be left floating. The quiescent current consumption of the TPS62125 is typ. 13µA under no load condition (not switching). See Figure 25. The DC/DC regulator stops operation once the voltage on the EN pin falls below the threshold $V_{EN\_TH\ OFF}$ (typ. 1.15V) or the input voltage falls below UVLO threshold. The enable comparator features a built in hysteresis of typ. 50mV. This hysteresis can be increased with an external resistor connected to pin EN_hys. See more details in application information section.

POWER GOOD OUTPUT / OUTPUT DISCHARGE (PG)

The Power Good Output (PG pin) is an open drain output. The circuit is active once the device is enabled. It is driven by an internal comparator connected to the FB pin voltage and an internal reference. The PG output provides a high level (open drain high impedance) once the feedback voltage exceeds typical 95% of its nominal value. The PG output is driven to low level once the FB pin voltage falls below typ. 90% of its nominal value V_{REF_FB}. The PG output goes high (high impedance) with a delay of typically 2µs. A pull up resistor is needed to generate a high level. The PG pin can be connected via a pull up resistors to a voltage up to 10V. This pin can also be used to discharge the output capacitor. See section Application Information for more details.

The PG output is pulled low if the voltage on the EN pin falls below the threshold $V_{EN\_TH\ OFF}$ or the input voltage is below the undervoltage lockout threshold UVLO.

SHORT-CIRCUIT PROTECTION

The TPS62125 integrates a high-side MOSFET switch current limit, I_{LIMF}, to protect the device against a short circuit. The current in the high-side MOSFET switch is monitored by a current limit comparator and once the current reaches the limit of I_{LIMF}, the high-side MOSFET switch is turned off and the low-side MOSFET switch is turned on to ramp down the inductor current. The high-side MOSFET switch is turned on again once the zero current comparator trips and the inductor current has become zero. In this case, the output current is limited to half of the high-side MOSFET switch current limit, ½ I_{LIMF}, typ. 300mA.

THERMAL SHUTDOWN

As soon as the junction temperature, T_J, exceeds 150°C (typical) the device goes into thermal shutdown. In this mode, the high-side and low-side MOSFETs are turned-off. The device continues its operation when the junction temperature falls below the thermal shutdown hysteresis.

Product Folder Link(s) : *TPS62125*

APPLICATION INFORMATION

OUTPUT VOLTAGE SETTING

The output voltage can be calculated by:

$$V_{OUT} = V_{REF\_FB} \times \left(1 + \frac{R_1}{R_2}\right)$$

$$V_{OUT} = 0.8V \times \left(1 + \frac{R_1}{R_2}\right)$$

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{0.8V} - 1\right)$$

(5)

The internal reference voltage for the error amplifier, V_{REF_FB}, is nominal 0.808V. However for the feedback resistor divider selection, it is recommended to use the value 0.800V as the reference. Using this value, the output voltage sets 1% higher and provides more headroom for load transients as well for line and load regulation. The current through the feedback resistors R_1 and R_2 should be higher than 1µA. In applications operating over full temperature range or in noisy environments, this current may be increased for robust operation. However, higher currents through the feedback resistors impact the light load efficiency of the converter.

Table 2 shows a selection of suggested values for the feedback divider network for most common output voltages.

Table 2. Suggested Values for Feedback Divider Network

Output Voltage	1.2V	1.8V	3.3V	5V	6.7V	8V
R1 [kΩ]	180	300	1800	1100	1475	1800
R2 [kΩ]	360	240	576	210	200	200

Product Folder Link(s) :*TPS62125*

ENABLE THRESHOLD AND HYSTERESIS SETTING
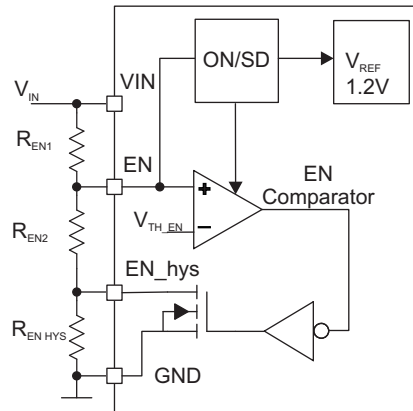
Figure 53. Using the Enable Comparator Threshold and Hysteresis for an input SVS (supply voltage supervisor)

The enable comparator can be used as an adjustable input supply voltage supervisor (SVS) to start and stop the DC/DC converter depending on the input voltage level. The input voltage level, $V_{IN\_startup}$, at which the device starts up is set by the resistors R_{EN1} and R_{EN2} and can be calculated by :

$$V_{IN\_startup} = V_{EN\_TH\_ON} \times \left(1 + \frac{R_{EN1}}{R_{EN2}} \right) = 1.2V \times \left(1 + \frac{R_{EN1}}{R_{EN2}} \right)$$

(6)

The resistor values R_{EN1} and R_{EN2} can be calculated by:

$$R_{EN1} = R_{EN2} \times \left(\frac{V_{IN\_startup}}{V_{EN\_TH\_ON}} - 1 \right) = R_{EN2} \times \left(\frac{V_{IN\_startup}}{1.2V} - 1 \right)$$

(7)

$$R_{EN2} = \frac{R_{EN1}}{\left(\frac{V_{IN\_startup}}{V_{EN\_TH\_ON}} - 1 \right)} = \frac{R_{EN1}}{\left(\frac{V_{IN\_startup}}{1.2V} - 1 \right)}$$

(8)

The input voltage level V_{IN_stop} at which the device will stop operation is set by R_{EN1}, R_{EN2} and $R_{EN\ HYS}$ and can be calculated by:

$$V_{IN\_stop} = V_{EN\_TH\_OFF} \times \left(1 + \frac{R_{EN1}}{R_{EN2} + R_{EN\_hys}} \right) = 1.15V \times \left(1 + \frac{R_{EN1}}{R_{EN2} + R_{EN\_hys}} \right)$$

(9)

The resistor value R_{EN_hys} can be calculated according to:

$$R_{EN\_hys} = \frac{R_{EN1}}{\left(\frac{V_{IN\_stop}}{V_{EN\_TH\_OFF}} - 1 \right)} - R_{EN2} = \frac{R_{EN1}}{\left(\frac{V_{IN\_stop}}{1.15V} - 1 \right)} - R_{EN2}$$

(10)

The current through the resistors R_{EN1}, R_{EN2} and $R_{EN\ HYS}$ should be higher than 1µA. In applications operating over the full temperature range and in noisy environments, the resistor values can be reduced to smaller values.
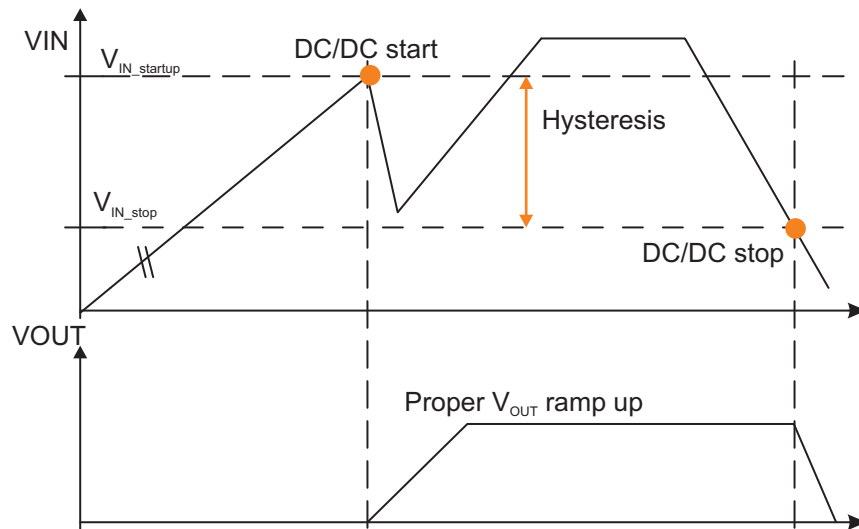
Figure 54. Using the EN comparator as input SVS for proper V_{OUT} ramp up

POWER GOOD (PG) PULL UP / OUTPUT DISCHARGE RESISTOR

The Power Good open collector output needs an external pull up resistor to indicate a high level. The pull up resistor can be connected to a voltage level up to 10V. The output can sink current up to 0.4mA with specifed output low level of less than 0.3V. The lowest value for the pull up resistor can be calculated by:

$$R_{Pullup\,min} = \frac{V_{OUT} - 0.3V}{0.0004A}$$

(11)
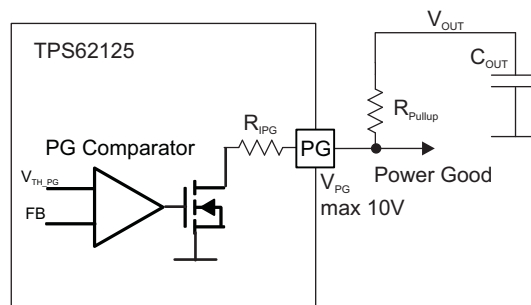
Figure 55. PG open collector output

The PG pin can be used to discharge the output capacitor. The PG output has an internal resistance R_{IPG} of typical 600Ω and minimum 400Ω. The maximum sink current into the PG pin is 10mA. In order to limit the discharge current to the maximum allowable sink current into the PG pin, the external pull up resistor $R_{Pull\,up}$ can be calculated to:

$$R_{Pullup\,min} = \frac{V_{OUT}}{I_{PG\_max}} - R_{IPG\_min} = \frac{V_{OUT}}{0.01A} - 400\Omega$$

(12)

In case a negative value is calculated, the external pull up resistor can be removed and the PG pin can be directly connected to the output.

OUTPUT FILTER DESIGN (INDUCTOR AND OUTPUT CAPACITOR)

The external components have to fulfill the needs of the application, but also the stability criteria of the devices control loop. The TPS62125 is optimized to work within a range of L and C combinations. The LC output filter inductance and capacitance have to be considered together, creating a double pole, responsible for the corner frequency of the converter. Table 3 can be used to simplify the output filter component selection.

Table 3. Recommended LC Output Filter Combinations

Inductor Value [µH][1]	Output Capacitor Value [µF][2]			
	10µF	2 x 10µF	22µF	47µF
V_{OUT} 1.2V - 1.8V				
15	√	√	√	√
22	√[3]	√	√	√
VOUT 1.8V - 3.3V				
15	√[3]	√	√	√
22	√[3]	√	√	√
VOUT 3.3V - 5V				
10		√	√	√
15		√[3]	√[3]	√
22				
VOUT 5V - 10V				
10		√[3]	√[3]	√
15		√	√	√
22		√	√	√

(1)   Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by 20% and -30%.
(2)   Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by 20% and -50%.
(3)   This LC combination is the standard value and recommended for most applications.

More detailed information on further LC combinations can be found in application note SLVA515.

INDUCTOR SELECTION

The inductor value affects its peak-to-peak ripple current, the PWM-to-PFM transition point, the output voltage ripple and the efficiency. The selected inductor has to be rated for its DC resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_{IN} or V_{OUT} and can be estimated according to Equation 13.

Equation 14 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 14. This is recommended because during heavy load transient the inductor current will rise above the calculated value. A more conservative way is to select the inductor saturation current according to the high-side MOSFET switch current limit I_{LIMF}.

$$\Delta I_L = \frac{(V_{IN} - V_{OUT})}{L} \times T_{ON}$$

(13)

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2}$$

(14)

With:

T_{ON} = see equation (3)
L = Inductance
ΔI_L = Peak to Peak inductor ripple current
I_{Lmax} = Maximum Inductor current

Product Folder Link(s) :*TPS62125*

In DC/DC converter applications, the efficiency is essentially affected by the inductor AC resistance (i.e. quality factor) and by the inductor DCR value. To achieve high efficiency operation, care should be taken in selecting inductors featuring a quality factor above 25 at the switching frequency. Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

The total losses of the coil consist of both the losses in the DC resistance (R_{DC}) and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

The following inductor series from different suppliers have been used with the TPS62125.

Table 4. List of Inductors

INDUCTANCE [µH]	DCR [Ω]	DIMENSIONS [mm^3]	INDUCTOR TYPE	SUPPLIER
10 / 15	0.33 max / 0.44 max	3.3 x 3.3 x 1.4	LPS3314	Coilcraft
22	0.36 max	3.9 x 3.9 x 1.8	LPS4018	Coilcraft
15	0.33 max	3.0 x 2.5 x 1.5	VLF302515	TDK
10/15	0.44 max / 0.7 max	3.0 x 3.0 x 1.5	LPS3015	Coilcraft
10	0.38 typ.	3.2 × 2.5 × 1.7	LQH32PN	Murata

OUTPUT CAPACITOR SELECTION

Ceramic capacitors with low ESR values provide the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At light load currents the converter operates in Power Save Mode and the output voltage ripple is dependent on the output capacitor value and the PFM peak inductor current. Higher output capacitor values minimize the voltage ripple in PFM Mode and tighten DC output accuracy in PFM Mode. In order to achieve specified regulation performance and low output voltage ripple, the DC-bias characteristic of ceramic capacitors must be considered. The effective capacitance of ceramic capacitors drops with increasing DC - bias Voltage. Due to this effect, it is recommended for output voltages above 3.3V to use at least 1 x 22µF or 2 x 10µF ceramic capacitors on the output.

INPUT CAPACITOR SELECTION

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. For most applications, a 10µF ceramic capacitor is recommended. The voltage rating and DC bias characteristic of ceramic capacitors need to be considered. The input capacitor can be increased without any limit for better input voltage filtering.

For applications powered from high impedance sources, a tantalum polymer capacitor should be used to buffer the input voltage for the TPS62125. Tantalum polymer capacitors provide a constant capacitance vs. DC bias characteristic compared to ceramic capacitors. In this case, a 10µF ceramic capacitor should be used in parallel to the tantalum polymer capacitor to provide low ESR.

Take care when using only small ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output or V_{IN} step on the input can induce large ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part by exceeding the maximum ratings. In case the power is supplied via a connector e.g. from a wall adapter, a hot-plug event can cause voltage overshoots on the VIN pin exceeding the absolute maximum ratings and can damage the device, too. In this case a tantalum polymer capacitor or overvoltage protection circuit reduces the voltage overshoot, see Figure 41.

Table 5 shows a list of input/output capacitors.

Table 5. List of Capacitor

CAPACITANCE [μF]	SIZE	CAPACITOR TYPE	USAGE	SUPPLIER
10	0805	GRM21B 25V X5R	C_{IN} /C_{OUT}	Murata
10	0805	GRM21B 16V X5R	C_{OUT}	Murata
22	1206	GRM31CR61 16V X5R	C_{OUT}	Murata
22	B2 (3.5x2.8x1.9)	20TQC22MYFB	C_{IN} / input protection	Sanyo

LAYOUT CONSIDERATIONS

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show frequency variations, poor line and/or load regulation, stability issues as well as EMI problems. It is critical to provide a low inductance, low impedance ground path. Therefore, use wide and short traces for the paths conducting AC current of the DC/DC converter. The area of the AC current loop (input capacitor - TPS62125 - inductor - output capacitor) should be routed as small as possible to avoid magnetic field radiation. Therefore the input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor. Use a common Power GND node and a different node for the signal GND to minimize the effects of ground noise. Keep the common path to the GND pin, which returns both the small signal components and the high current of the output capacitors as short as possible to avoid ground noise. A well proven practice is to merge small signal GND and power GND path at the exposed thermal pad. The FB divider network and the FB line should be routed away from the inductor and the SW node to avoid noise coupling. The VOS line should be connected as short as possible to the output, ideally to the VOUT terminal of the inductor. Keep the area of the loop VOS node - inductor - SW node small. The Exposed Thermal Pad must be soldered to the circuit board for mechanical reliability and to achieve appropriate power dissipation.
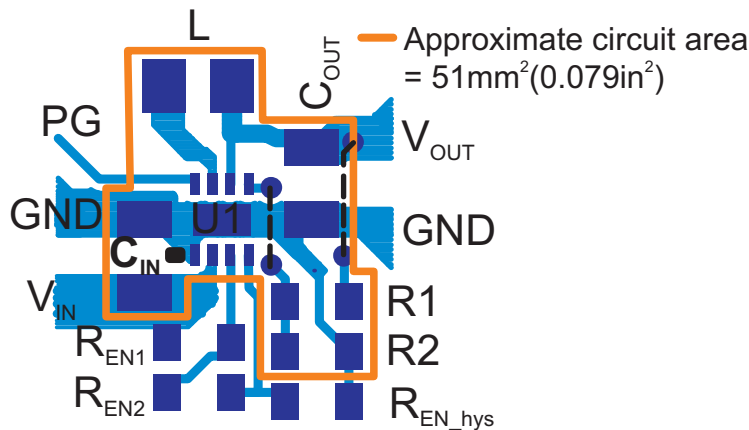
Figure 56. EVM board Layout

TEXAS INSTRUMENTS

TPS62125

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TYPACAL APPLICATIONS
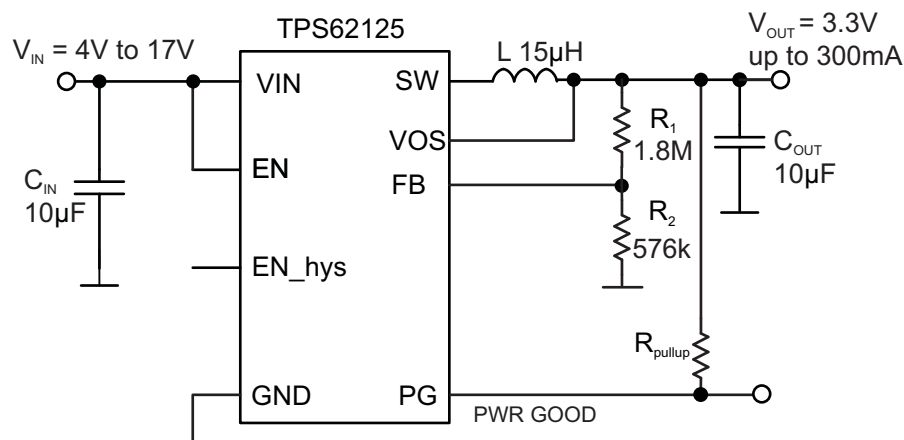
Figure 57. TPS62125 3.3V Output Voltage Configuration

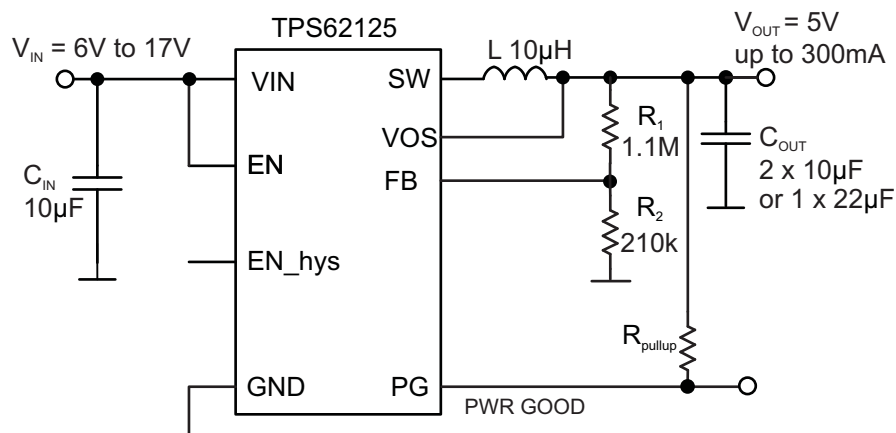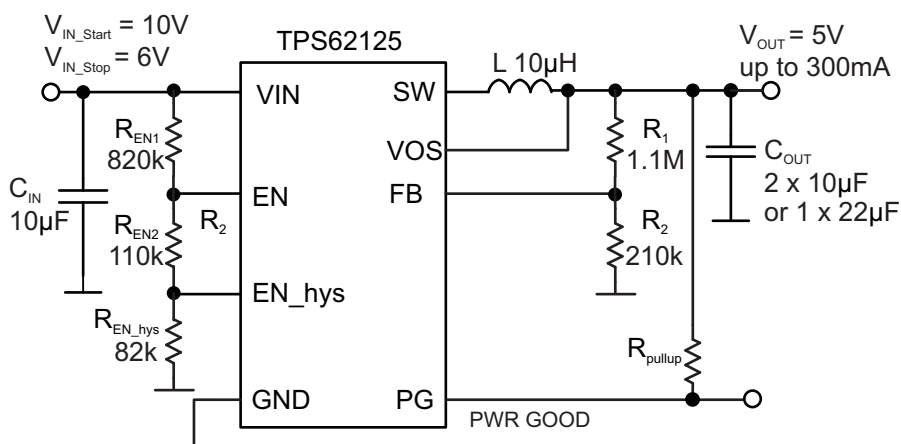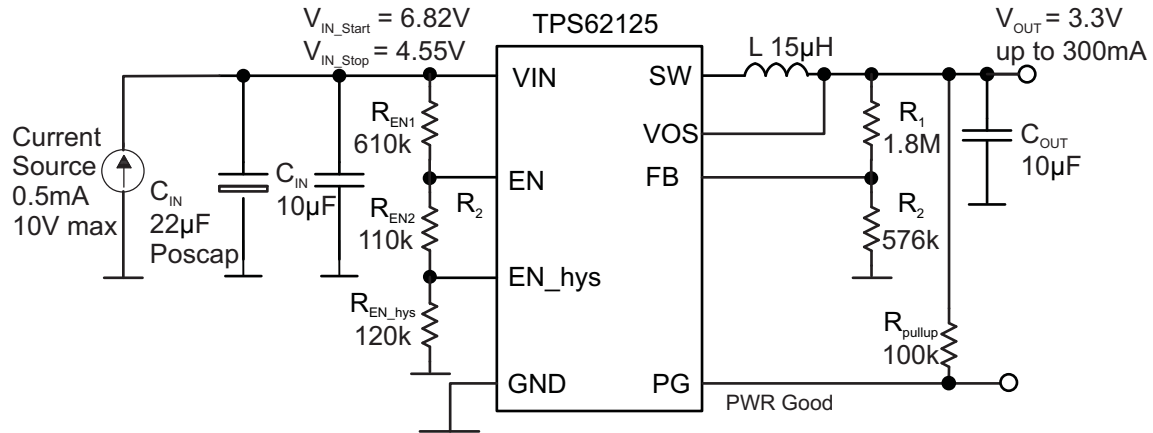Figure 58. TPS62125 5.0V Output Voltage Configuration

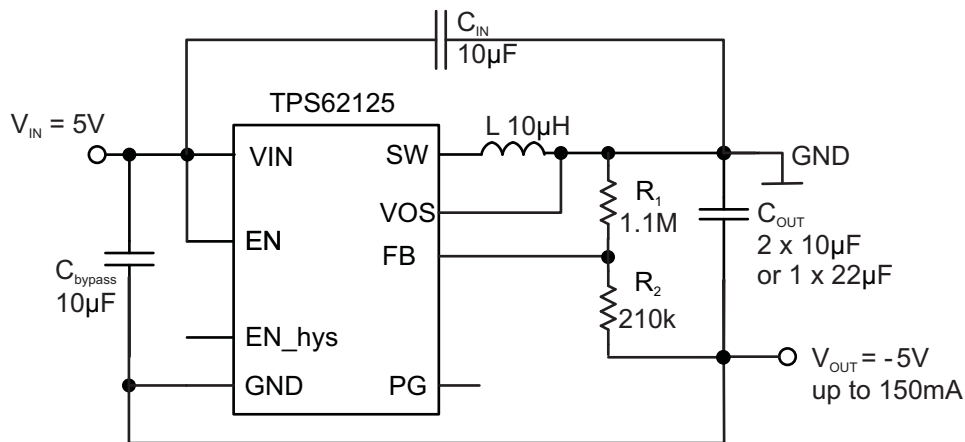Figure 59. TPS62125 5V VOUT, Start up voltage $V_{IN\_Start = 10V}$, Stop voltage V_{IN_Stop} = 6V, see Figure 43

Product Folder Link(s) :TPS62125

Figure 60. TPS62125 operation from a storage capacitor charged from a 0.5mA current source, V_{OUT} = 3.3V, see Figure 45

Figure 61. 5V to -5V inverter configuration, see SLVA514

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
TPS62125DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS62125DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

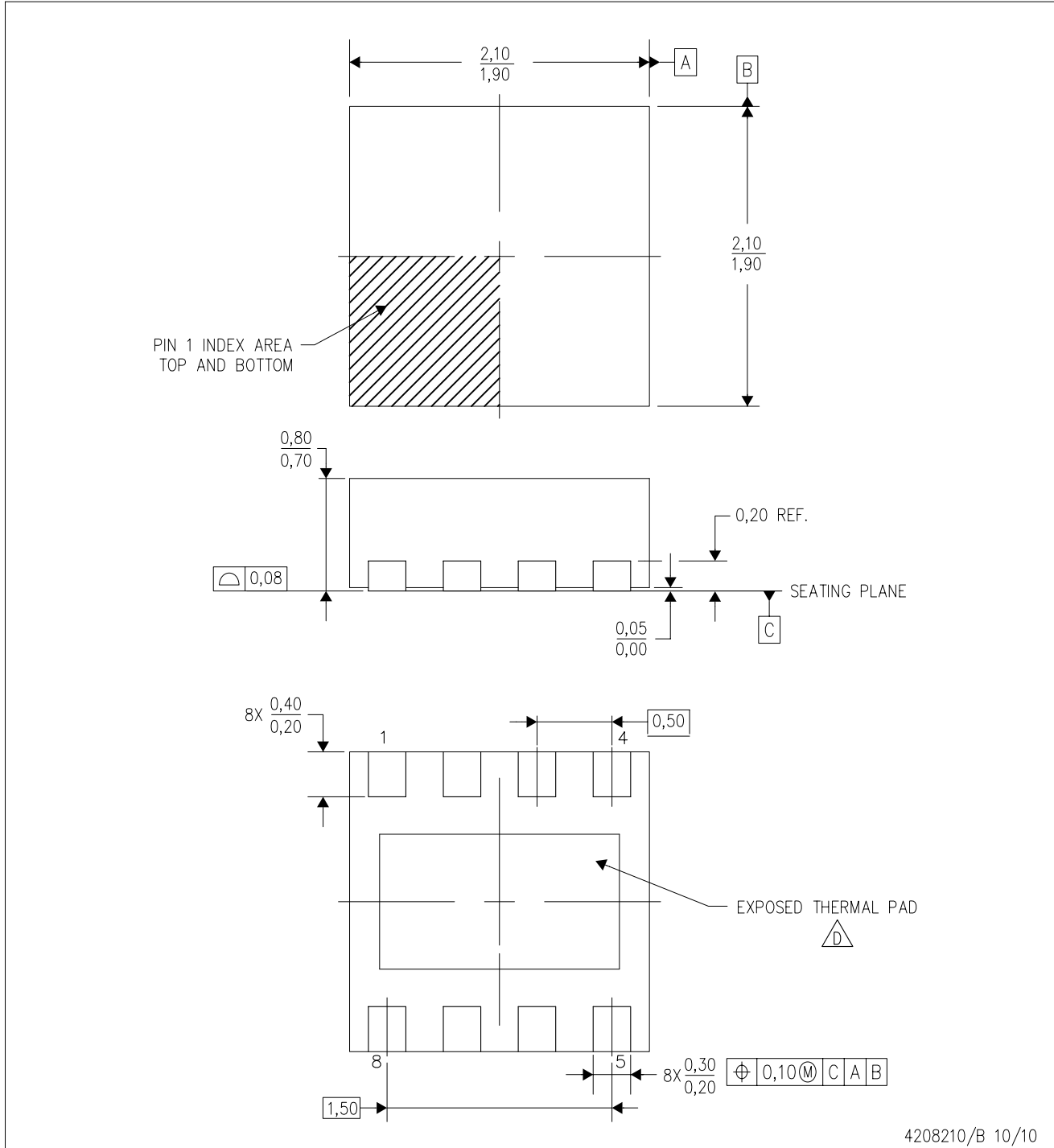| Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62125DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62125DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62125DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS62125DSGT	WSON	DSG	8	250	210.0	185.0	35.0

DSG (S−PWSON−N8)   PLASTIC SMALL OUTLINE NO−LEAD

2,10 / 1,90

A   B

2,10 / 1,90

PIN 1 INDEX AREA
TOP AND BOTTOM

0,80 / 0,70

0,20 REF.

◠ | 0,08

SEATING PLANE

C

0,05 / 0,00

8X 0,40 / 0,20

0,50

1   4

EXPOSED THERMAL PAD

/D\

8   5   8X 0,30 / 0,20   ⊕ | 0,10 Ⓜ | C | A | B

1,50

4208210/B 10/10

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Quad Flatpack, No−Leads (QFN) package configuration.
        /D\   The package thermal pad must be soldered to the board for thermal and mechanical performance.
              See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
         E.   Falls within JEDEC MO−229.

DSG (S−PWSON−N8)   PLASTIC SMALL OUTLINE NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.
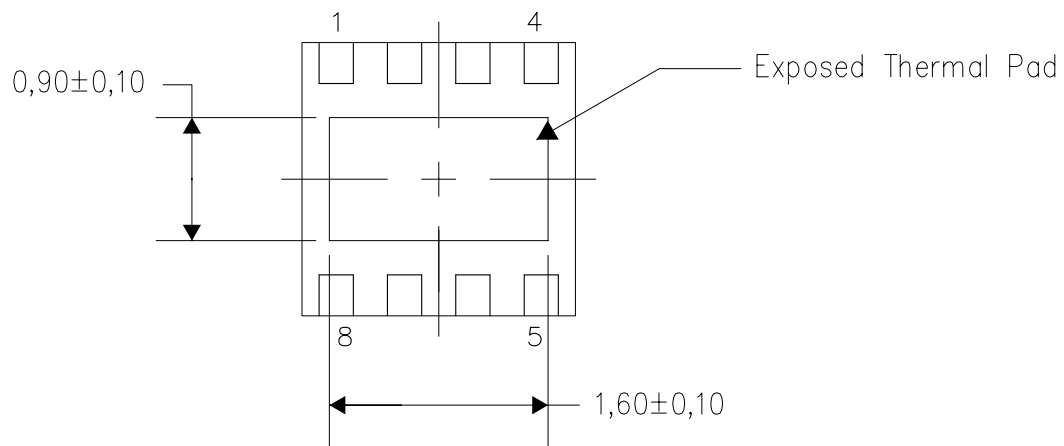
Bottom View

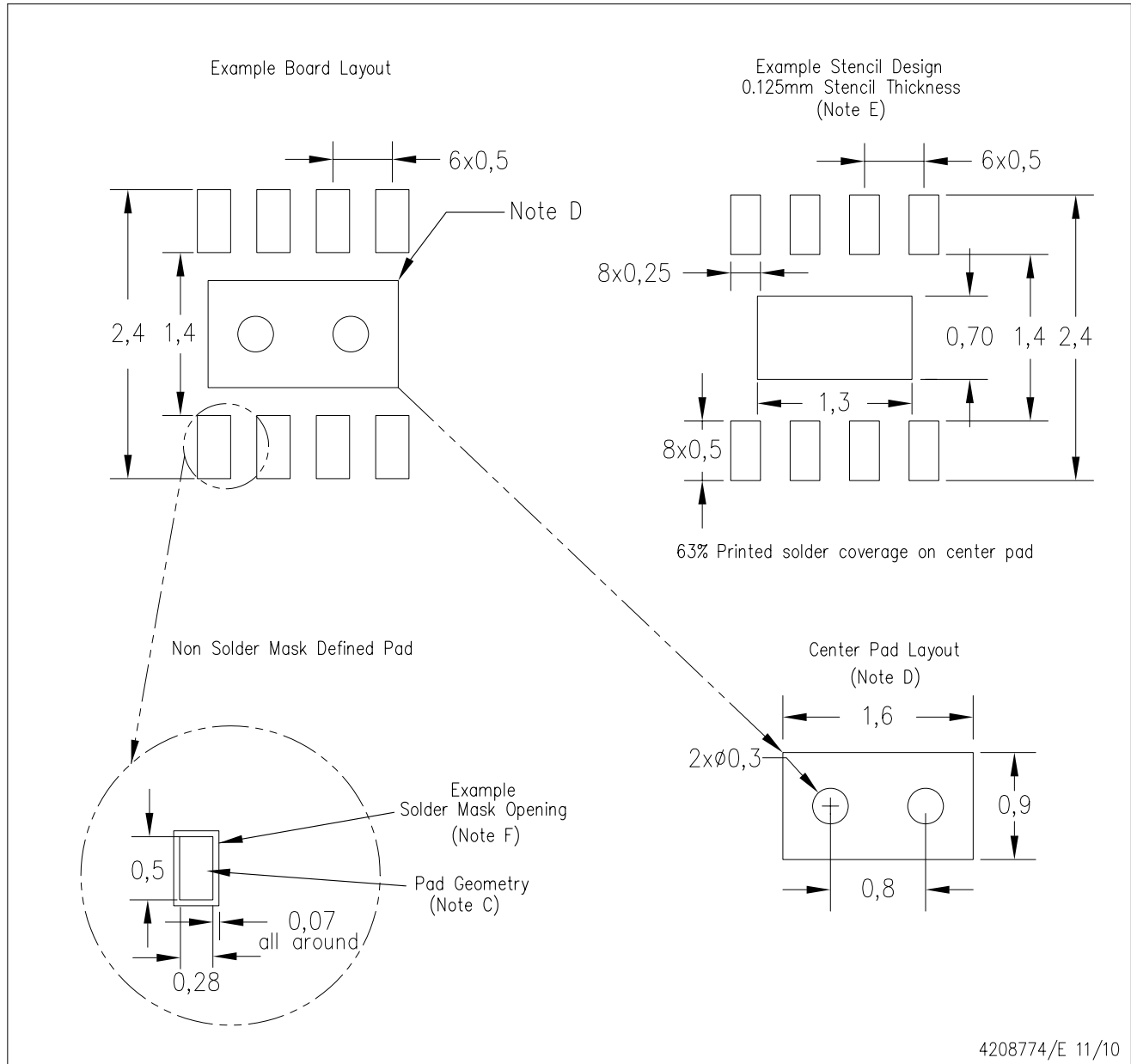Exposed Thermal Pad Dimensions

4208347/E 11/10

NOTE: A.   All linear dimensions are in millimeters

DSG (S−PWSON−N8)   PLASTIC SMALL OUTLINE NO−LEAD

Example Board Layout

6x0,5

Note D

2,4 1,4

Non Solder Mask Defined Pad

Example
Solder Mask Opening
(Note F)

Pad Geometry
(Note C)

0,5

0,07
all around

0,28

Example Stencil Design
0.125mm Stencil Thickness
(Note E)

6x0,5

8x0,25

0,70 1,4 2,4

1,3

8x0,5

63% Printed solder coverage on center pad

Center Pad Layout
(Note D)

1,6

2xØ0,3

0,9

0,8

4208774/E 11/10

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC−7351 is recommended for alternate designs.
        D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note,
            QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
            for specific thermal information, via requirements, and recommended board layout.
            These documents are available at www.ti.com <http://www.ti.com>.
        E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
        F. Customers should contact their board fabrication site for solder mask tolerances.

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