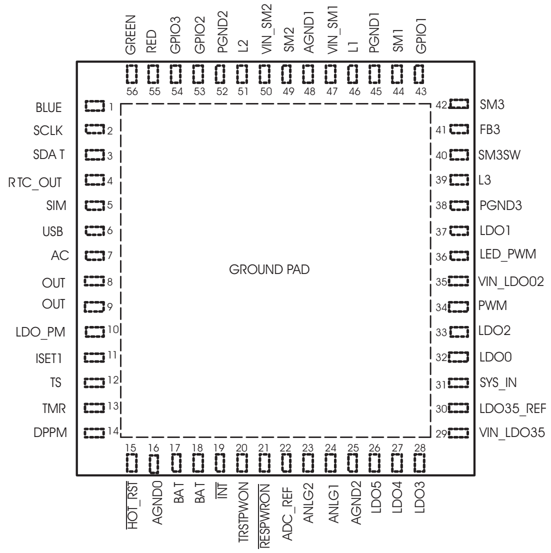
SINGLE-CELL Li-ION BATTERY- AND POWER-MANAGEMENT IC

FEATURES

- BATTERY CHARGER
  - – Complete charge management solution for single Li-Ion/Li-Pol cell with thermal foldback, dynamic power management and pack temperature sensing, supporting up to 1.5-A max charge current
  - – Programmable charge parameters for AC adapter and USB port operation
- INTEGRATED POWER SUPPLIES
  - – A total of 9 LDOs are integrated:
    - Six adjustable output LDOs (1.25-V to 3.3-V)
    - Two fixed-voltage LDOs (3.3-V)
    - One fixed-voltage, always-on LDO (3.3-V)
    - One RTC backup supply with low leakage (3.1-V)
  - – Two 600-mA, programmable dc/dc buck converters (0.6-V to 3.4-V) with enable, standby mode operation and automatic low-power mode setting
- DISPLAY FUNCTIONS
  - – Two open-drain PWM outputs with programmable frequency and duty cycle. Can be used to control keyboard backlight, vibrator, or other external peripheral functions
  - – RGB LED driver with programmable flashing period and individual R/G/B brightness control
  - – Constant-current white LED driver, with programmable current level, brightness control, and over-voltage protection can drive up to 6 LEDs in series configuration
- SYSTEM MANAGEMENT
  - – Dual input power path function with input current limiting and OVP protection
  - – POR function with programmable masking monitors all integrated supplies outputs
  - – Software and hardware reset functions
  - – 8-channel integrated A/D samples system parameters with single conversion, peak detection, or averaging operating modes
- HOST INTERFACE
  - – Host can set system parameters and access system status using I2C interface
  - – Interrupt function with programmable masking signals system status modifiction to host
  - – 3 GPIO ports, programmable as drivers, integrated A/D trigger or buck converters standby mode control

APPLICATIONS

- PDAs
- Smart Phones
- MP3s
- Internet Appliances
- Handheld Devices



QFN 56-Pin, 7 x 7 mm Package
(Top View - Not To Scale)

DESCRIPTION

The TPS65820 provides an easy to use, fully integrated solution for handheld devices, integrating charge management, multiple regulated power supplies, system management and display functions, in a small thermally-enhanced 7x7 package. The high level of integration enables typical board area space savings of 70% when compared to equivalent discrete solutions, while implementing a high-performance and flexible solution, portable across multiple platforms. If required, an external host may control the TPS65820 via I2C interface, with access to all integrated systems. The I2C enables setting output voltages, current thresholds, and operation modes. Internal registers have a complete set of status information, enabling easy diagnostics, and host-controlled handling of fault conditions. The TPS65820 can operate in stand-alone mode, with no external host control, if the internal power-up defaults are compatible with the system requirements

AVAILABLE OPTIONS(1)

T_J	DEVICES(2)(3)(4)	MARKING
–40°C to 125°C	TPS65820RSH	TPS65820

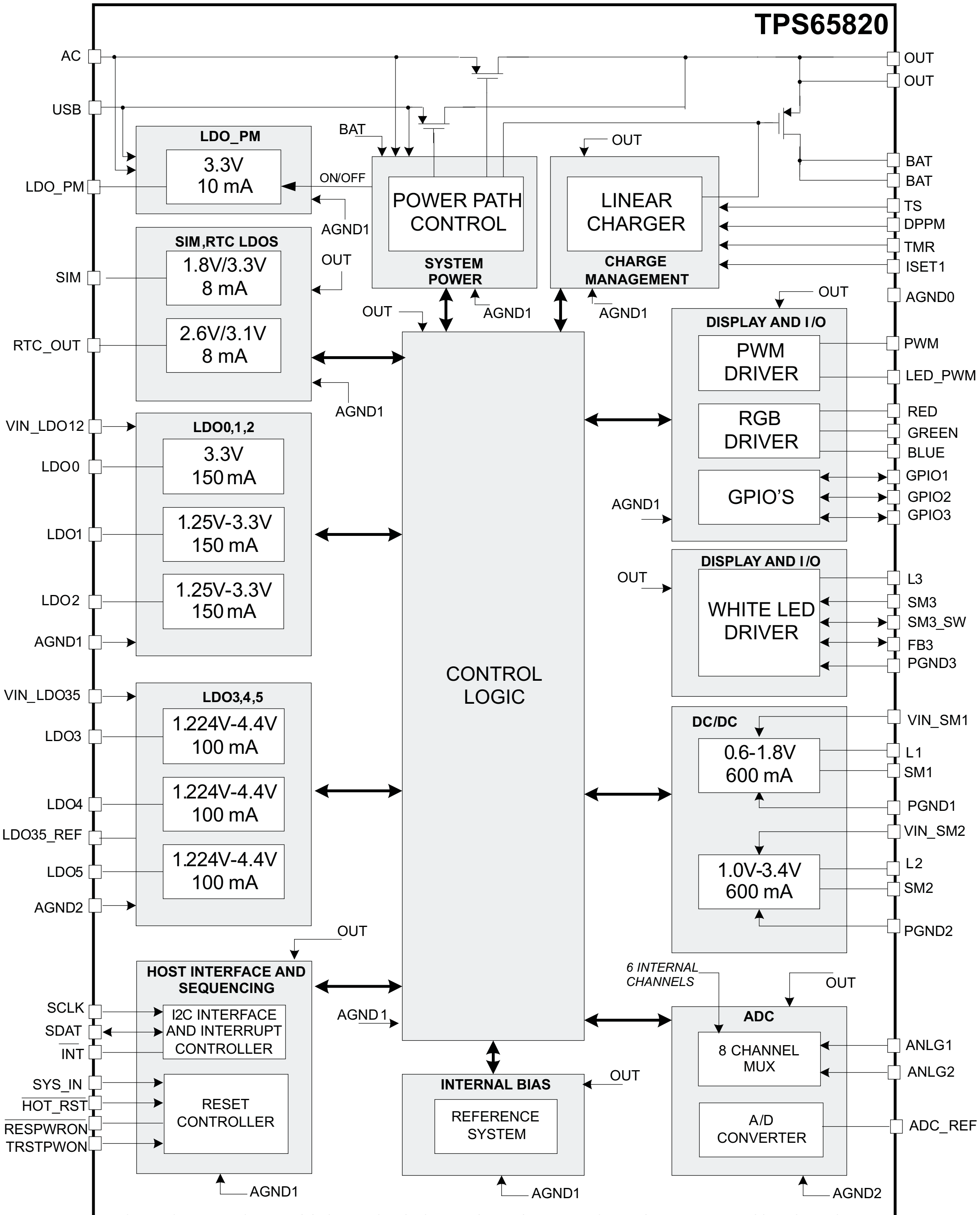
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

(2) The RSH package is available in tape and reel. Add suffix R (TPS65820RSHR) to order quantities of 2000 parts per reel. Add suffix T (TPS65820RSHT) to order quantities of 250 parts per reel.

(3) This product is RoHS compatible, including a lead concentration that does not exceed 0.1% of total product weight, and is suitable for use in specified lead-free soldering processes. In addition, this product uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(4) Other power-up sequences and default power-up states for the supplies can be implemented upon request. Consult factory for available options

FUNCTIONAL BLOCK DIAGRAM



AGND 0, AGND 1 AND AGND 2PINS SHORTED TO EACH OTHER INSIDE TPS 65800 ALL AGND PINS ARE INTERNALLY CONNECTED TO THE TPS 65800 THERMAL PAD AND SUBSTRATE .
PGND 1, PGND 3 AND PGND 3PINS ARE NOT CONNECTED TO EACH OTHER OR TO THE TPS 65800 SUBSTRATE / POWER PAD

Figure 1. TPS65820 Simplified Block Diagram

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)[1]

		VALUE	UNIT
	AC and USB with respect to AGND1	–0.3 to 18	V
	ANLG1, ANLG2 with respect to AGND2	–0.3 to V(OUT)	
	V(OUT) with respect to AGND1	5	
	VIN_LDO12 , VIN_LDO35, LDO3, LDO4, LDO5 with respect to AGND2	–0.3 to V(OUT)	
	LDO35_REF, ADC_REF with respect to AGND2	–0.3 to smaller of: 3.6 or V(OUT)	
	SIM, RTC_OUT with respect to AGND1	–0.3 to smaller of: 3.6 or V(OUT)	
	SM1, L1, VIN_SM1 with respect to PGND1	–0.3 to V(OUT)	
	SM2, L2, VIN_SM2 with respect to PGND2	–0.3 to V(OUT)	
	SM3, L3 with respect to PGND3	–0.3 to 29	
	SM3SW with respect to PGND3	–0.3 to V(OUT)	
	FB3 with respect to PGND3	–0.3 to 0.5	
	All other pins (except AGND and PGND), with respect to AGND1	–0.3 to V(OUT)	
	AGND2, AGND0, PGND1, PGND2, PGND3 with respect to AGND1	–0.3 to +0.3	
	Input Current, AC pin	2750	mA
	Input Current, USB pin	600	
	Output continuous current, OUT pin	3000	
	Output conitnuous current, BAT pin	–3000	
	Continuous Current at L1, PGND1, L2, PGND2	1800	
T_A	Operating free-air temperature	–40 to 85	°C
T_J	Maximum junction temperature	125	
T_{STG}	Storage temperature	–65 to 150	
	Lead temperature 1,6 mm (1/16-inch) from case for 10 seconds	260	
	ESD rating, all pins	1.5	kV

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

PACKAGE	θ_{JA}	$T_A \leq 55°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 55°C$
RSH (1) (2)	21.7°C/W	3.22 W	0.046 W/°C

(1) This data is based on using the JEDEC High-K board and the exposed die pad is connected to a Cu pad on the board. This is connected to the ground plane by a via matrix.
(2) The RSH package MSL Level : HIR3 at 260°C

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
	AC and USB with respect to AGND1	4.35	16.5[1]	V
	ANLG1,ANLG2 with respect to AGND2	0	2.6	V
	VIN_LDO35 with respect to AGND2	Greater of : 3.6 V OR Minimum input voltage required for LDO/Converter operation outside dropout region	4.7	V
	VIN_LDO12 with respect to AGND1		4.7	
	VIN_SM1 with respect to PGND1		4.7	
	VIN_SM2 with respect to PGND2		4.7	
	SM3 with respect to PGND3		28	V
T_A	Operating free-air temperature	–40	85	°C
T_J	Maximum junction temperature, functional operation assured	–40	125	°C
T_J	Maximum junction temperature, electrical characteristics assured	0	125	°C

(1) Thermal operating restrictions are reduced or avoided if input voltage does not exceed 5 V.

ELECTRICAL CHARACTERISTICS – I2C INTERFACE

Over recommended operating conditions (typical values at T_J = 25°C), application circuit as in figure (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I2C TIMING CHARACTERISTICS					
t_R	SCLK/SDATA rise time			300	ns
t_F	SCLK/SDATA fall time			300	
$t_{W(H)}$	SCLK pulse width high	600			
$t_{W(L)}$	SCLK Pulse Width Low	1.3			µs
$t_{SU(STA)}$	Setup time for START condition	600			ns
$t_{H(STA)}$	START condition hold time after which first clock pulse is generated	600			
$t_{SU(DAT)}$	Data setup time	100			
$t_{H(DAT)}$	Data hold time	0			
$t_{SU(STOP)}$	Setup time for STOP condition	600			
$t_{(BUF)}$	Bus free time between START and STOP condition	1.3			µs
FSCL	Clock Frequency			400	kHz
I²C INTERFACE LOGIC LEVELS					
V_{IH}	High level input voltage	1.3		6	V
V_{IL}	Low level input voltage	0		0.6	
I_H	Input bias current		0.01		µA

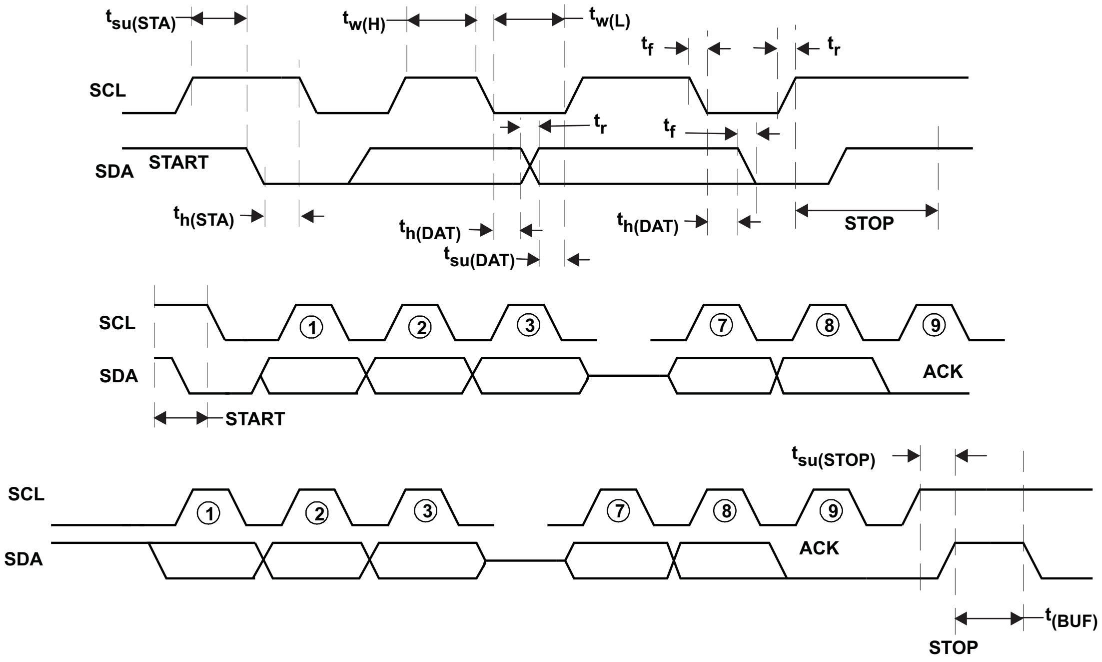


Figure 2. I²C Timing

ELECTRICAL CHARACTERISTICS – SYSTEM SEQUENCING AND OPERATING MODES

Over recommended operating conditions (typical values at T_J = 25°C), application circuit as in Figure 3 (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENT						
$I_{BAT(SLEEP)}$	BAT pin current, sleep mode set	Input power not detected, V(BAT) = 4.2 V, Sleep mode set		370		µA
$I_{BAT(DONE)}$	BAT pin current, charge terminated	Charger function enabled by I2C, termination detected, input power detected and selected		3		µA
$I_{BAT(CHGOFF)}$	BAT pin current, charge function OFF	Charger function disabled by I2C, termination not detected, input power detected and selected		3		µA
$I_{INP(CHGOFF)}$	AC or USB pin current, charge function OFF	Charger function disabled by I2C, termination not detected, input power detected and selected. All integrated supplies and drivers OFF, no load at OUT pin.			200	µA
UNDER-VOLTAGE LOCKOUT						
V_{UVLO}	Internal UVLO detection threshold	NO POWER mode set at V(OUT) < V_{UVLO}, V(OUT) decreasing	–3%	2.5	3%	V
V_{UVLO_HYS}	UVLO detection hysteresis	V(OUT) increasing		120		mV
$t_{DGL(UVLO)}$	UVLO detection deglitch time	Falling voltage only		5		ms
SYSTEM LOW VOLTAGE THRESHOLD						
V_{LOW_SYS}	Minimum system voltage detection threshold	System voltage V(SYS_IN) decreasing, SLEEP mode set if V(SYS_IN) < V_{LOW_SYS}	0.97	1.0	1.03	V
$V_{HYS(LOWSYS)}$	Minimum system voltage detection hysteresis	V(SYS_IN) increasing		50		mV
$t_{DGL(HOTPLUG)}$	Minimum system voltage detection hotplug deglitch time	V(SYS_IN) decreasing, valid only for initial power-up, see state machine diagram		650		ms
$t_{DGL(LOWSYS)}$	Minimum system voltage detection deglitch time	V(SYS_IN) decreasing, hotplug deglitch time expired		5		ms
THERMAL FAULT						
T_{SHUT}	Thermal shutdown	Increasing junction temperature		165		°C
$T_{HYS(SHUT)}$	Thermal shudown hysteresis	Decreasing junction temperature		30		°C
INTEGRATED SUPPLY POWER FAULT DETECTION						
V_{PGOOD}	Power good fault detection threshold	Falling output voltage, applies to all integrated supply outputs. Referenced to the programmed output voltage value	84%	90%	96%	
$V_{HYS(PGOOD)}$	Power good fault detection hysteresis	Rising output voltage, applies to all integrated supply outputs. Referenced to V_{PGOOD} threshold	3%	5%	7%	
HOT RESET FUNCTION						
V_{HRSTON}	Low level input voltage	RESET mode set at $V(\overline{HOT\_RESET}) < V_{HRSTON}$			0.4	V
$V_{HRSTOFF}$	High level input voltage	HOT reset not active at $V(\overline{HOT\_RESET}) > V_{HRSTOFF}$	1.3			V
$t_{DGL(HOTRST)}$	Hot reset input deglitch			5		ms
SYSTEM RESET – OPEN DRAIN OUTPUT $\overline{RESPWRON}$						
V_{RSTLO}	Low level output voltage	I_{IL} = 10 mA, $V(\overline{RESPWRON}) < V_{RSTLO}$	0		0.3	V
$I_{TRSTPWON}$	Pull-up current source	Internally connected to TRSTPWRON pin	0.9	1.0	1.2	µA
K_{RESET}	Reset timer constant	$T_{RESET} = K_{RESET}$° $C_{TRSTPWON}$		1		ms/nF
SEQUENCING DELAYS						
$t_{DLY(D1)}$	Sequencing delay	See sequencing timing diagram		0.24		ms
$t_{DLY(D1)}$	Sequencing delay	See sequencing timing diagram		12		ms

ELECTRICAL CHARACTERISTICS – POWER PATH AND CHARGE MANAGEMENT

Over recommended operating conditions (typical values at T_J = 25°C), application circuit as in Figure 3 (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
VOLTAGE DETECTION THRESHOLDS							
$V_{IN(DT)}$	Input Voltage detection threshold	AC detected at V(AC)– V(BAT) > $V_{IN(DT)}$; USB detected at V(USB)– V(BAT) > $V_{IN(DT)}$		190			mV
$V_{IN(NDT)}$	Input Voltage removal threshold	AC not detected at V(AC)– V(BAT) < $V_{IN(NDT)}$; USB not detected at V(USB)– V(BAT) < $V_{IN(NDT)}$				125	mV
$t_{DGL(NDT)}$	Power not detected deglitch				22.5		ms
$V_{SUP(DT)}$	Supplement detection threshold	Battery switch ON at V(BAT) – V(OUT) > $V_{SUP(DT)}$			60		mV
$V_{SUP(NDT)}$	Supplement not detected threshold	Battery switch OFF at V(BAT)– V(OUT) < $V_{SUP(NDT)}$			20		mV
POWER PATH INTEGRATED MOSFETs CHARACTERISTICS							
V_{ACDO}	AC switch dropout voltage	V_{ACDO} = V(AC)– V(OUT); V(AC) = 4.75 V AC input current limit set to 2.75 A (typ) , $I_{O(OUT)}$ = 1.0 A			350	375	mV
V_{USBDO}	USB switch dropout voltage	V_{USBDO} = V(USB)– V(OUT); V(USB) = 4.6 V USB input current limit set to 2.75 A (typ)	I(OUT)+ I(BAT)= 0.5 A		175	190	mV
			I(OUT)+ I(BAT)= 0.1 A		35	45	mV
$V_{BATDODCH}$	Battery switch dropout voltage, discharge	V(BAT): 3 V → $V_{CH(REG)}$, I(BAT) = –1 A			60	100	mV
$V_{BATDOCH}$	Battery switch dropout voltage, charge	Charger on, V(BAT): 3 V → 4.2 V, I(BAT) = 1 A			60	100	mV
POWER PATH INPUT CURRENT LIMIT							
$I_{INP(LIM1)}$	Selected Input current limit, applies to USB input only	Selected Input switch not in dropout, I^2C settings : ISET2 = LO, PSEL = LO		80		100	mA
$I_{INP(LIM2)}$	Selected Input current limit, applies to USB input only	Selected Input switch not in dropout, I^2C settings: ISET2 = HI, PSEL = LO		400		500	mA
$I_{INP(LIM3)}$	Selected Input current limit, applies to either AC or USB input	Selected Input switch not in dropout, I^2C settings: ISET2 = HI OR LO, PSEL = HI				2.75	A
SYSTEM REGULATION VOLTAGE							
$V_{SYS(REG)}$	Output regulation voltage	$V_{SYS(REG)}$ = V(OUT), DPPM loop not active, selected input current limit not reached. Selected input voltage (AC or USB) > 5.1 V			4.6	4.7	V
POWER PATH PROTECTION AND RECOVERY FUNCTIONS							
$V_{INOUTSH}$	Input to Output short circuit detection threshold	AC and USB switches set to OFF if V(OUT) < $V_{INOUTSH}$			0.6		V
$R_{SH(USBSH)}$	OUT short circuit recovery pull-up resistor	V(OUT) < 1 V, internal resistor connected from USB to OUT			500		Ω
$R_{SH(ACSH)}$	OUT short circuit recovery pull-up resistor	V(OUT) < 1 V, internal resistor connected from AC to OUT			500		Ω
V_{OVP}	Over-voltage detection threshold	Rising voltage, over-voltage detected when V(AC) > V_{OVP} or V(USB) > V_{OVP}		6.0	6.5	6.8	V
	Over-voltage detection hysteresis	Falling voltage, relative to detection threshold			0.1		V
$V_{BATOUTSH}$	Battery to Output short circuit detection threshold	BAT switch set to OFF if V(BAT)-V(OUT)> $V_{BATOUTSH}$			200		mV
$K_{BLK(SHBAT)}$	Battery to Ouput short circuit blanking time constant	$V_{(DPPM)}$ < 1V, $t_{BLK(SHBAT)}$ = $K_{BLK(SHBAT)}$ X C_{DPPM} , C_{DPPM} capacitor is connected from DPPM pin to AGND1			1		mS/nF
$I_{SH(BAT)}$	OUT short circuit recovery pull-up current source	$V_{(BAT)}$– $V_{(OUT)}$ > $V_{BATOUTSH}$, Internal current source connected between OUT and BAT			10		mA
$R_{SHBAT)}$	BAT short circuit recovery resistor	$V_{(BAT)}$ < 1V, Internal resistor connected from OUT to BAT			1		KΩ
$R_{DCH(BAT)}$	BAT pull-down resistor	Internal resistor connected from BAT to AGND1 when battery is not detected by ANLG1			500		Ω

ELECTRICAL CHARACTERISTICS – POWER PATH AND CHARGE MANAGEMENT (Continued)

Over recommended operating conditions (typical values at T_J = 25°C), application circuit as in Figure 3 (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER PATH TIMING CHARACTERISTICS, DPPM AND THERMAL LOOPS NOT ACTIVE, R_{TMR} = 50 kΩ							
t_{BOOT}	Boot-up time	Measured from input power detection		120	150	180	ms
$t_{SW(ACBAT)}$	Switching from AC to BAT	No USB: measured from V(AC)– V(BAT) < $V_{IN(NDT)}$, USB detected:CE=LO (after CE hold-off time)				50	µs
$t_{SW(USBBAT)}$	Switching from USB to BAT	No AC: measured from V(USB)– V(BAT) < $V_{IN(NDT)}$,USB detected:CE=LO (after CE hold-off time)				50	µs
$t_{SW(PSEL)}$	Switching from USB to AC	Toggling I^{2}C PSEL bit				50	µs
$t_{SW(ACUSB)}$	Switching from AC to USB or USB to AC	AC power removed or USB power removed				100	µs
BATTERY REMOVAL DETECTION							
$V_{NOBATID}$	Battery ID resistor detection	ID resistor not detected at V(OUT)– V(ANLG1) < $V_{NOBATID}$			0.5		V
$t_{DGL(NOBAT)}$	Deglitch time for battery removal detection			0.6		1.2	ms
$I_{O(ANLG1)}$	ANLG1 pull-up current	Set via I^{2}C bits (BATID1,BATID2) ADC_WAIT register	00, $V_{(OUT)}$: 2.5 V to 4.4 V		$\frac{V(OUT) - 1.2}{500\ k\Omega}$		µA
			01		10		
			10		50		
			11		60		
		Total accuracy		25%		25%	
FAST CHARGE CURRENT , V(OUT) > V(BAT) + 0.1 V, V(BAT) > V_{LOWV}							
$I_{O(BAT)}$	Charge current range	$I_{O(BAT)} = \frac{K_{(SET)} \times V_{(SET)}}{R_{SET}}$		100		1500	mA
V_{SET}	Battery charge current set voltage	V_{SET} = V(ISET1), (ISET1_1, ISET1_0) =	11, 100% scaling	2.475	2.500	2.525	V
			10, 75% scaling	1.875	1.900	1.925	
			01, 50% scaling	1.225	1.250	1.275	
			00, 25% scaling	0.575	0.600	0.625	
K_{SET}	Battery charge current set factor	100 mA < $I_{O(BAT)} \le$ 1 A		350	400	450	
		1 mA < $I_{O(BAT)} \le$ 100 mA		100	400	1000	
PRE-CHARGE CURRENT, V(OUT) > V(BAT) + 0.1 V, V_{BATSH} < V(BAT) < V_{LOWV}, t < $t_{(PRECHG)}$							
$I_{O(PRECHG)}$	Precharge current range	$I_{O(PRECHG)} = \frac{V_{(PRECHG)} \times K_{(SET)}}{R_{SET}}$		10		150	mA
V_{PRECHG}	Precharge set voltage	V_{PRECHG} = V(ISET1)		220	250	270	mV
V_{LOWV}	Precharge to fast-charge transition	Fast charge at V(BAT) > V_{LOWV}		2.8	3.0	3.2	V
$t_{DGL(PRE)}$	Deglitch time for fast charge to precharge transition	Decreasing battery voltage, R_{TMR} = 50 kΩ			22.5		ms
CHARGE REGULATION VOLTAGE, V(OUT) > $V_{O(BATREG)}$ + 0.1V							
$V_{O(BATREG)}$	Battery charge voltage	Voltage options, Selection via I^{2}C			4.20		
					4.356		
		Accuracy, T_A = 25°C		–0.5%		0.5%	
		Total accuracy		–1%		1%	
CHARGE TERMINATION, V(BAT) > V_{RCH} , VOLTAGE REGULATION MODE SET							
I_{TERM}	Charge termination current range	$I_{(TERM)} = \frac{V_{(TERM)} \times K_{(SET)}}{R_{SET}}$		10		150	mA
V_{TERM}	Battery termination detection set voltage	V_{TERM} = V(ISET1), (ISET1_1, SET1_0) =	11, 100% scaling	240	260	280	mV
			10, 75% scaling	145	160	175	
			01, 50% scaling	90	110	130	
			00, 25% scaling	40	60	75	
$t_{DGL(TERM)}$	Deglitch time for termination detection	V(ISET1) < V_{TERM} , R_{TMR} = 50 kΩ			22.5		ms

ELECTRICAL CHARACTERISTICS – POWER PATH AND CHARGE MANAGEMENT (Continued)

Over recommended operating conditions (typical values at T_J = 25°C), application circuit as in Figure 3 (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BATTERY RECHARGE DETECTION						
V_{RCH}	Recharge threshold voltage	New charge cycle starts if V(BAT) < $V_{O(BATREG)}$– V_{RCH}, after termination was detected	80	100	130	mV
$t_{DGL(RCH)}$	Deglitch time for recharge detection	R_{TMR} = 50 kΩ		22.5		ms
DPPM FUNCTION						
V_{DPPM}	DPPM regulation point range	$V_{(DPPM)} = R_{DPPM}$ x K_{DPPMM} x $I_{O(DPPM)}$	2.6		4.4	V
$I_{O(DPPM)}$	DPPM pin current source	AC or USB Present	95	100	105	µA
K_{DPPM}	DPPM scaling factor		1.139	1.15	1.162	
$t_{DGL(DPPM)}$	DPPM de-glitch time	Status bit set indicating DPPM loop active after deglitch time, R_{TMR} = 50 kΩ		500		µs
PACK TEMPERATURE SENSING						
V_{LTF}	Low temperture threshold	Pack low temperature fault at V(TS) > V_{LTF}	2.465	2.500	2.535	V
V_{HTF}	High temperture threshold	Pack low temperature fault at V(TS) < V_{HTF}	0.485	0.500	0.515	V
$I_{O(TS)}$	Temperature sense current source	Thermistor bias current	18.8	20	21.2	µA
$t_{DLG(TFAULT)}$	Deglitch time for temperature fault detection	R(TMR) = 50 kΩ, V(TS) > V_{LTF} OR V(TS) < V_{HTF}		22.5		ms
CHARGE AND PRE-CHARGE SAFETY TIMER						
t_{CHG}	Charge safety timer programmed value	Safety timer range, thermal/DPPM loop not active, $t_{CHG} = R_{TMR}$ x K_{TMR}	3	5	10	hours
K_{TMR}	Charge Timer set factor		0.313	0.360	0.414	s/Ω
t_{CHGADD}	Total elapsed time when DPPM or thermal loop are active	fast charge on, t_{CHGADD} is the maximum add-on time added to t_{CHG}		2 x t_{CHG}		hours
t_{PRECHG}	Precharge safety timer programmed value	Pre charge safety timer range, thermal/DPPM loop not active, $t_{PRECHG} = K_{PRE}$ x R_{TMR} x K_{TMR}	18	30	60	min
K_{PRE}	Pre-charge timer set factor		0.09	0.1	0.11	
$t_{PCHGADD}$	Total elapsed time when DPPM or thermal loop are active	pre-charge on, $t_{PCHGADD}$ is the maximum add-on time added to t_{PRECHG}		2 x t_{PRECHG}		hours
R_{TMR}	External timer resistor limits		30		100	kΩ
$R_{TMR(FLT)}$	Timer fault recovery pull-up resistor	Internal resistor connected from OUT to BAT after safety timer timeout		1		kΩ
THERMAL REGULATION LOOP						
T_{THREG}	Temperature regulation limit	Charge current decreasesd and timer extended when T_J > T_{THREG}	115		135	°C
CHARGER THERMAL SHUTDOWN						
T_{THCHG}	Charger thermal shutdown	Charger turned off when T_J> T_{THCHG}		150		°C
$T_{THCHGHYS}$	Charger thermal shutdown hysteresis			30		°C

ELECTRICAL CHARACTERISTICS – LINEAR REGULATORS

Over recommended operating conditions (typical values at T_J = 25°C), application circuit as in Figure 3 (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SELECTABLE OUTPUT VOLTAGE LDO'S : LDO1, LDO2							
$I_{Q(LDO12)}$	Quiescent current, either LDO1 or LDO2 enabled, LDO0 disabled	$I_{Q(LDO12)}$ = I(VIN_LDO02)	$I_{(LDO1,2)}$ = –1 mA		15		µA
			$I_{(LDO1,2)}$ = –150 mA		160		
$I_{O(LDO1,2)}$	Output current range					150	mA
$V_{O(LDO1,2)}$	LDO1, LDO2 Output Voltage	Output Voltage, Selectable via I^2C.			Available output voltages: $V_{O(LDO1,2)}$ TYP = 1.25, 1.5, 1.8, 2.5, 2.85, 3, 3.2, 3.3		V
		Dropout voltage, 150 mA load				300	mV
		Total accuracy, V(VIN_LDO02) = 3.65 V		–3%		3%	
		Line Regulation, 100 mA load, V(VIN_LDO02): $V_{(LDO1,2)TYP}$ + 0.5 V → 4.7 V		–1%		1%	
		Load regulation, load: 10 mA → 150 mA V(VIN_LDO02) > $V_{O(LDO1,2)\ TYP}$ + 0.5V		–1.5%		1.5%	
$P_{SR(LDO12)}$	PSRR at 20 kHz	150mA load at output, V(VIN_LDO02) – $V_{O(LDO1,2)}$=1V			40		dB
$I_{SC(LDO1,2)}$	LDO1&2 short circuit current limit	Output grounded			300		mA
$R_{DCH(LDO1,2)}$	Discharge resistor	LDO disabled by I^2C command			300		Ω
$I_{LKG(LDO1,2)}$	Leakage current	LDO off			2		µA
SIM LINEAR REGULATOR							
$I_{Q(SIM)}$	Quiescent current	Internally connected to OUT pin			20		µA
$I_{O(SIM)}$	Output current range					8	mA
$V_{O(SIM)}$	SIM LDO output voltage	Output voltage, Selectable via I^2C.			Available output voltages: $V_{O(SIM)TYP}$ = 1.8 or 3.0		V
		Dropout voltage , 8 mA load				0.2	V
		Total accuracy, V(OUT): 3.2 V to 4.7 V, 8 mA		–5%		5%	
		Load regulation, load: 1 mA → 8 mA, V(OUT) > $V_{O(SIM)\ TYP}$ + 0.5 V		–3%		3%	
		Line regulation, 5 mA load, V(OUT): $V_{O(SIM)\ TYP}$ + 0.5 V → 4.7 V		–2%		2%	
$I_{SC(SIM)}$	Short Circuit current limit	Output grounded			20		mA
$I_{LKG(SIM)}$	Leakage current	LDO off			1		µA
PROGRAMMABLE OUTPUT VOLTAGE LDO'S: LDO3, LDO4, LDO5							
$I_{Q(LDO35)}$	Quiescent current, only one of LDO3, LDO4, LDO5 is enabled	$I_{Q(LDO35)}$ = I(VIN_LDO35)			70		µA
$I_{O(LDO35)}$	Output current range					100	mA
$V_{O(LDO35)}$	LDO3, LDO4, LDO5 output voltage	Output Voltage, Selectable via I^2C			Available output voltages : $V_{O(LDO35)TYP}$ = 1.224 V to 4.46 V, 25 mV steps		V
		Dropout voltage, 100-mA load				240	mV
		Total accuracy, 100 mA load $V_{(VIN\_LDO35)}$ = 5 V		–3%		3%	
		Load regulation, V(VIN_LDO35) > $V_{O(LDO35)TYP}$ + 0.5 V	load: 1 mA → 50 mA	–1%		1%	
		Line regulation, 10 mA load, V(VIN_LDO35): $V_{O(LDO35)TYP}$ + 0.5 V → 4.7 V		–1%		1%	
$I_{SC(LDO35)}$	Short circuit current limit	Output grounded			250		mA
$PSR_{(LDO35)}$	PSRR at 10 kHz	V(VIN_LDO35) > $V_{O(LDO3,5)}$ +1 V , 50 mA load at output			40		dB
$R_{DCH(LDO35)}$	Discharge resistor	LDO is disabled by I^2C command			400		Ω
$I_{LKG(LDO35)}$	Leakage current	LDO off			1		µA

ELECTRICAL CHARACTERISTICS – LINEAR REGULATORS (continued)

Over recommended operating conditions (typical values at T_J = 25°C), application circuit as in Figure 3 (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
RTC_OUT LINEAR REGULATOR							
$I_{Q(RTC\_OUT)}$	Quiescent current for RTC LDO	Internally connected to OUT pin			20		µA
$I_{O(RTC\_OUT)}$	Output current range					8	mA
$V_{O(RTC\_OUT)}$	RCT_OUT output voltage	Output voltage value, Selectable via I^2C.		Available output voltages: 2.6 V or 3.1 V			V
		Dropout voltage , I(RTC_OUT) = –8 mA				200	mV
		Total accuracy, V(OUT): 2 V to 4.7 V, 8 mA load, sleep mode not set		–5%		5%	
		Load regulation, load: 1 mA → 8 mA , 2 V < V(OUT) < 4.7 V		–3%		3%	
		Line regulation, 5 mA load V(OUT): 2 V → 4.7 V		–2%		2%	
$I_{SH(RTC\_OUT)}$	Short circuit current limit	V(RTC_OUT) = 0 V			20		mA
$I_{LKG(RTC\_OUT)}$	Leakage current	V(RTC_OUT) = 1.5 V, V(OUT) = 0 V	T_J = 85°C		880		nA
			T_J = 25°C		250		
LDO0 LINEAR REGULATOR							
$I_{Q(LDO0)}$	Quiescent current	Internally connected to VIN_LDO12 pin	I(LDO0) = –1 mA		15		µA
			I(LDO0) = –150 mA		160		
$I_{O(LDO0)}$	Output current range					150	mA
$V_{O(LDO0)}$	Output voltage	Fixed output voltage value			3.3		V
		Dropout voltage , I(LDO0) = –150 mA				300	mV
		Total accuracy		–3%		3%	
		Line regulation, V(OUT): $V_{O(LDO0)}$+ 0.5 → 4.7 V, I(LDO0) =– 100 mA		–1%		1%	
		Load regulation, I(LDO0) = –10 mA →– 150 mA		–1.5%		1.5%	
$PSR_{(LDO0)}$	PSRR at 20 kHz	150 mA load at output , V(VIN_LDO12) – $V_{O(LDO1,2)}$=1V			40		dB
$I_{SC(LDO0)}$	Short circuit current limit	V(LDO0) = 0 V			300		mA
$I_{LKG(LDO0)}$	Leakage current	LDO off			1		µA
LDO_PM LINEAR REGULATOR							
$I_{Q(LD0\_PM)}$	Output current range					20	mA
$V_{O(LDO\_PM)}$	Output voltage	Fixed output voltage value, V(OUT) > 4V			3.3		V
		Dropout voltage, I(LDOPM) = -12 mA			0.5	0.7	V
		Total accuracy		–5%		5%	
$I_{LKG(LDOPM)}$	Leakage current	LDO off			1		µA

ELECTRICAL CHARACTERISTICS – SWITCHED MODE SM1 STEP DOWN CONVERTER

Over recommended operating conditions (typical values at T_J = 25°C), $V_{O(SM1)}$ = 1.24 V, application circuit as in Figure 3 (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{Q(SM1)}$	Quiescent current for SM1	$I_{Q(SM1)}$ = I(VIN_ SM1), no output load	Not switching		10		µA
		SM1 OFF, set via I^2C			0.1		
$I_{O(SM1)}$	Output current range					600	mA
$V_{O(SM1)}$	Output voltage, PWM mode	Output voltage , selectable via I^2C, Standby OFF		Available output voltages: $V_{O(SM1)TYP}$ = 0.6 V to 1.8 V, adjustable in 40 mV steps			V
		$V_{O(SM1)} = V_{SBY(SM1)}$, Output voltage range, Standby ON		Available output voltages: $V_{SBY(SM1)}$ = 0.6 V to 1.8 V, adjustable in 40 mV steps			
		Total accuracy, $V_{O(SM1)TYP} = V_{SBY(SM1)}$ = 1.24 V, V(VIN_SM1) = 3.0 V to 4.7 V; 0 mA ≤ $I_{O(SM1)}$ ≤ 600 mA		–3%		3%	
		Line Regulation, V(VIN_SM1): 3.0 → 4.70 V, $I_{O(SM1)}$ = 10 mA			0.027		%/V
		Load Regulation, V(VIN_SM1) = 4.7 V, $I_{O(SM1)}$: 60 mA → 540 mA			0.139		%/A
$R_{DSON(PSM1)}$	P-channel MOSFET on-resistance	V(VIN_SM1) = 3.6 V, 100% duty cycle set			310	500	mΩ
$I_{LKG(PSM1)}$	P-channel leakage current				0.1		µA
$R_{DSON(NSM1)}$	N-channel MOSFET on-resistance	V(VIN_SM1) = 3.6 V, 0% duty cycle set			220	330	mΩ
$I_{LKG(PSM1)}$	N-channel leakage current				5		µA
$I_{LIM(SM1)}$	P&N -channel current limit	3.0 V < V(VIN_SM1) < 4.7 V		900	1050	1200	mA
$f_{S(SM1)}$	Oscillator frequency	PWM mode set		1.3	1.5	1.7	MHz
$EFF_{(SM1)}$	Efficiency	V(VIN_SM1) = 4.2 V, PWM mode, $I_{O(SM1)}$ = 300 mA, $V_{O(SM1)}$ = 3 V			90%		
$t_{SS(SM1)}$	Soft start ramp time	Converter OFF→ON, $V_{O(SM1)}$: 5% → 95% of target value			750		µs
$t_{DLY(SM1)}$	Converter turn-on delay	GPIO1 pin programmed as SM1 converter enable control. Measured from V(GPIO1): LO → HI			170		µ s

ELECTRICAL CHARACTERISTICS – SWITCHED MODE SM2 STEP DOWN CONVERTER

Over recommended operating conditions (typical values at T_J = 25°C), $V_{O(SM1)}$ = 1.24 V , application circuit as in Figure 3 (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{Q(SM2)}$	Quiescent current for SM2	$I_{Q(SM2)}$ = I(VIN_ SM2), no output load	Not switching		10		µA
		SM2 OFF, set via I^2C			0.1		
$I_{O(SM2)}$	Output current range					600	mA
$V_{O(SM2)}$	Output voltage	Output voltage , selectable via I^2C, Standby OFF			Available output voltages: $V_{O(SM2)TYP}$ = 1.0 V to 3.4 V, adjustable in 80 mV steps		V
		$V_{O(SM2)}$ = $V_{SBY(SM2)}$, Output voltage range, Standby ON			Available output voltages: $V_{SBY(SM2)}$ = 1.0 V to 3.4 V, adjustable in 80 mV steps		
		Total accuracy, $V_{O(SM2)TYP}$ = $V_{SM2(SBY)}$ = 1.8 V, V(VIN_SM2) = greater of [3.0 V or ($V_{O(SM2)}$ + 0.3 V)] to 4.7 V; 0 mA ≤ $I_{O(SM2)}$≤ 600 mA		–3%		3%	
		Line regulation, V(VIN_SM2) = greater of [3.0 V or ($V_{O(SM2)}$ + 0.3 V)] to 4.7 V; 0 mA ≤ $I_{O(SM2)}$≤ 600 mA			0.027		%/V
		Load regulation, V(VIN_SM2) = 4.7 V, $I_{O(SM2)}$: 60 mA → 540 mA			0.139		%/A
$R_{DSON(PSM2)}$	P-channel MOSFET on-resistance	V(VIN_SM2) = 3.6 V, 100% duty cycle set			310	500	mΩ
$I_{LKG(PSM2)}$	P-channel leakage current				0.1		µA
$R_{DSON(NSM2)}$	N-channel MOSFET on-resistance	V(VIN_SM2) = 3.6 V, 0% duty cycle set			220	330	mΩ
$I_{LKG(PSM2)}$	N-channel leakage current				5		µA
$I_{LIM(SM2)}$	P&N -channel current limit	3.0 V < V(VIN_SM2) < 4.7 V		900	1050	1200	mA
$f_{S(SM2)}$	Oscillator frequency	PWM mode set		1.3	1.5	1.7	MHz
$EFF_{(SM2)}$	Efficiency	V(VIN_SM2) = 4.2 V, $I_{O(SM2)}$ = 300 mA, $V_{O(SM2)}$ = 3 V			90%		
$t_{SS(SM2)}$	Soft start ramp time	Converter OFF→ON, $V_{O(SM2)}$: 5% → 95% of target value			750		µs
$t_{DLY(SM2)}$	Converter turn-on delay	GPIO2 pin programmed as SM2 converter enable control. Measured from V(GPIO2): LO → HI			170		µ s

ELECTRICAL CHARACTERISTICS – GPIOs

Over recommended operating conditions (typical values at T_J = 25°C), application circuit as in Figure 3 (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GPIO1–3						
V_{OL}	Low level output voltage GPIO0	I_{OL} = 20 mA			0.5	V
I_{OGPIO}	Low level sink current into GPIO1,2,3	V(GPIOn) = V(OUT)	20			mA
V_{IL}	Low level input voltage				0.4	V
$I_{LKG(GPIO)}$	Input leakage current	V(GPIOn) = V(OUT)		1		µA

ELECTRICAL CHARACTERISTICS – ADC

Over recommended operating conditions (typical values at T_J = 25°C), V(ADC_REF) =2.535v if external reference voltage is used,application circuit as in Figure 3 (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG INPUTS							
$V_{RNG(CH1\_5)}$	Full scale input range Ch1 to Ch5	Positive inputs (active clamp) Full scale ~ 2.535 V		0		V(ADC _REF)	V
$V_{RNG(CH6\_8)}$	Full scale input range Ch6 to Ch8	Positive inputs (active clamp) Full scale ~4.7 V		0		V_{INTREF} x 1.854	V
$C_{IN(ADC)}$	Input capacitance (all channels)				15		pF
$R_{INADC(CH1\_5)}$	Input resistance	(Ch1 to Ch5)		1			MΩ
$I_{LKGADC(CH1\_5)}$	Leakage current	(Ch1 to Ch5)				100	nA
$R_{INADC(CH6\_8)}$	Input resistance	(Ch6 to Ch8)		430	540		kΩ
$I_{LKGADC(CH6\_8)}$	Leakage current	(Ch6 to Ch8)				10	µA
$V_{CH5(ADC)}$	Internal voltage proportional to junction temperature	T_J = 25°C, ADC channel 5 input voltage			1.895		V
		Temperature coefficient			6.5		mV/°C
DC ACCURACY							
$RES_{(ADC)}$	Resolution	SAR ADC			10		Bits
$MCD_{(ADC)}$	No missing codes				SPECIFIED		
$INL_{(ADC)}$	Integral linearity error				±3		LSB
$DNL_{(ADC)}$	Differential non-linearity error				±1		LSB
$OFF_{ZERO(ADC)}$	Offset error	Deviation from the first code transition (00..00) to (00.001) from the ideal AGND + 1 LSB				5	LSB
$OFF_{CH(ADC)}$	Offset error match between channels					5	LSB
$GAIN_{ADC}$	Gain error	Deviation in code from the ideal full scale code (11…111) for the full scale voltage			±8		LSB
$GAIN_{CH(ADC)}$	Gain error match	Any two channels			2		LSB
THROUGHPUT SPEED							
ADC_{CLK}	Sampling clock			600	750	900	kHz
ADC_{TCONV}	Conversion time	Sampling, convertion and setting Rs ≤ 200 K for CH1,CH2,CH3 ; Rs ≤ 500 Ω for CH6, CH7, CH8		44	59	68	µ s
REFERENCE VOLTAGES							
V_{INTREF}	Internal ADC reference voltage	T_A = 25°C, V(ADC_REF)=V_{INTREF} when internal ADC reference is selected		2.53	2.535	2.54	V
$I_{SHRT(INTREF)}$	Internal reference short circuit limit	V(ADC_REF)= AGND1, internal reference enabled via I^2C			6		mA
$V_{REF(DRIFT)}$	ADC internal reference temperature drift				50	100	ppm/°C
$I_{Q(ADC)}$	ADC Internal reference quiescent current	Measured at OUT pin (internal reference) or ADC_REF pin (external reference)			40		µA
$I_{(ANLG2)}$	ANLG2 pin internal pull-up current source	ADC channel 2 bias current, set via I^2C register ADC_WAIT bits (ADC_CH2I_D1_1, ADC_CH2I _D2)	00 =		0		µA
			01 =		10		
			10 =		50		
			11 =		60		
		Total accuracy, relative to selected value		–25%		25%	

ELECTRICAL CHARACTERISTICS – ADC (continued)

Over recommended operating conditions (typical values at T_J = 25°C), V(ADC_REF) =2.535v if external reference voltage is used,application circuit as in Figure 3 (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{(ANLG1)}$	ANLG1 pin internal pull-up current source	ADC channel 1 bias current, set via I^{2}C register ADC_WAIT bits (BATIDI_D1, BATIDI _D2)	00 =		$\frac{V(OUT)\ -\ 1.2}{500\ k\Omega}$		µA
			01 =		10		
			10 =		50		
			11 =		60		
		Total accuracy		10%		10%	
INTERNAL REFERENCE POWER CONSUMPTION							
PD_{ACTIVE}	Power dissipation	Conversion active			2.3		mW
PD_{ARMED}	Power dissipation	Not converting			0.43		mW
TRIGGER TIMING CHARACTERISTICS							
$t_{DELAY(TRG)}$	Trigger delay time accuracy	Time range, set via I^{2}C register ADC_DELAY		0		750	uS
		Relative to typical value set via I^{2}C		-20%		20%	
$t_{WAIT(TRG)}$	Trigger wait time accuracy	Time range, set via I^{2}C register ADC_WAIT		0		20.48	mS
		Relative to typical value set via I^{2}C		-20%		20%	

ELECTRICAL CHARACTERISTICS – LED AND PWM DRIVERS

Over recommended operating conditions (typical values at T_J = 25°C), application circuit as in Figure 3 (unless otherwise noted)

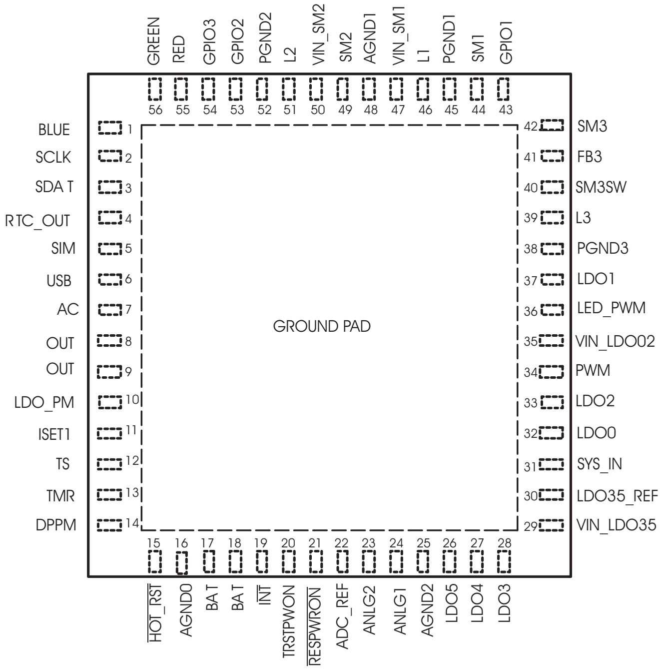
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SM3 BOOST CONVERTER, WHITE LED CONSTANT CURRENT DRIVER							
$V_{VIN(SM3)}$	Input Voltage range	V(OUT) = 3.3 V		3.0		4.7	V
V_{OVP3}	Output over-voltage trip	OVP detected at V(SM3) > V_{OVP3}		26.5	29	30	V
$V_{HYS(OVP3)}$	Output over-voltage hysteresis	OVP not detected at V(SM3) < V_{OVP3}– $V_{HYS(OVP3)}$			1.8		V
V_{SM3REF}	LED current sense threshold	LED current below regulation point at V(FB3) < V_{SM3REF}		244	252	260	mV
$I_{O(SM3)}$	LED current	Current range, Vin = 3.3 V, $I_{O(SM3)} = \frac{V(SM3REF)}{R_{FB3}}$		0		25	mA
		Total accuracy, $I_{O(SM3)}$ = 10mA		–10%		10%	
D_{SM3SW}	LED switch duty cycle	Duty cycle range		D_{SM3SW} = 0% to 99.6%, set via I^{2}C, 256 steps 0.4% minimum step			--
F_{REP_SM3}	LED switch duty cycle pattern repetition rate	256 pulses within repetition rate time	SM3_LF_OSC = 0		122		Hz
			SM3_LF_OSC = 1		183		
$R_{DSON(SM3SW)}$	LED switch MOSFET on-resistance	V(OUT)=3.6 V; I(SM3SW)=20 mA			1	2	Ω
$I_{LKG(SM3SW)}$	LED switch MOSFET leakage				1		µA
$R_{DSON(L3)}$	Power stage MOSFET on-resistance	V(OUT) = 3.6 V; I(L3) = 200 mA			300	600	mΩ
$I_{LKG(L3)}$	Power stage MOSFET leakage				1		µA
$I_{MAX(L3)}$	Power stage MOSFET current limit	3 V < V(OUT) < 4.7 V		400	500	600	mA
PWM DRIVER , PWM OPEN DRAIN OUTPUT							
$V_{OL(PWM)}$	Low level output voltage	I(PWM)= 150 mA				0.5	V
F_{PWM}	PWM driver frequency	Frequency range		Set via I^{2}C, F_{PWM} = 0.5/1/1.5/2/3/4.5/7.8/15.6			Hz
		Total accuracy, relative to selected value		-20%		20%	

ELECTRICAL CHARACTERISTICS – LED AND PWM DRIVERS (continued)

Over recommended operating conditions (typical values at T_J = 25°C), application circuit as in Figure 3 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
D_{PWM}	PWM driver duty cycle	Duty cycle range		D_{PWM} = 6.25% to 100%, set via I^2C, 6.25% minimum step			--
LED_PWM DRIVER, LED_PWM OPEN DRAIN OUTPUT							
D_{LEDPWM}	LED_PWM driver duty cycle	Duty cycle range		D_{LEDPWM} = 0% to 99.6%, set via I^2C, 256 steps 0.4% minimum step			
$F_{REP(LEDPWM)}$	LED_PWM driver duty cycle pattern repetition rate	256 pulses within repetition rate time	SM3_LF_OSC = 0		122		Hz
			SM3_LF_OSC = 1		180		
$V_{OL(LEDPWM)}$	Low level output voltage	I(LED_PWM) = 150 mA				0.5	V
$V_{OH(LEDPWM)}$	High level output voltage					6	V
RGB DRIVER, RED/GREEN/BLUE OPEN DRAIN OUTPUTS							
$t_{FLASH(RGB)}$	Flashing period	Flashing period range		$t_{FLASH(RGB)}$ = 1 to 8 sec, set via I^2C, 0.5 sec minimum step, 8 steps			sec
		Total accuracy		-20%		20%	
$t_{FLASH(ON)}$	Flash on time	Flash on time range, value selectable by I^2C		Set via I^2C , $t_{FLASH(ON)}$ = 0.1/0.15/0.2/0.25/0.3/0.4/ 0.5/0.6 Sec			sec
		Total accuracy, relative to selected value		-20%		20%	
D_{RGB}	Duty cycle	Duty cycle range, value selectable via I^2C		D_{RGB} = 0% to 99.98%, set via I^2C, 3.23% minimum step			
$I_{SINK(RGB)}$	RGB output sink current	V(RED) = V(GREEN) = V(BLUE) = 2 V, set via I2C RGB_ISET1,0	00 = (Driver set to OFF)				mA
			01 =	2.4	4	5.6	
			10 =	4.8	8	11.2	
			11 =	7	12	16.6	
$V_{OL(RGB)}$	Low level output voltage	Output low voltage, 8 mA load, RED/GREEN/BLUE PINS		0.3			V
$I_{LKG(RGB)}$	Output off leakage current	V(RED)=V(GREEN)=V(BLUE) = 4.7 V, all drivers disabled			1		µA

PIN ASSIGNMENT



PIN DESCRIPTION, REQUIRED EXTERNAL COMPONENTS

NAME	PIN	I/O	DESCRIPTION	EXTERNAL REQUIRED COMPONENTS (SEE APPLICATION DIAGRAM)
BLUE	1	O	Programmable blue driver, open drain output, current sink output when active.	Connect to BLUE input of RGB LED
SCLK	2	I	I^2C interface clock line	2-kΩ pull-up resistor to OUT pin
SDAT	3	I/O	I^2C interface data line	2-kΩ pull-up resistor to OUT pin
RTC_OUT	4	O	Low leakage LDO output. Can be connected to a super-capacitor or secondary cell, if used as a RTC backup output.	1 µF (minimum) capacitor to AGND1 pin or supercap
SIM	5	O	General purpose LDO output	1 µF (minimum) capacitor to AGND1 pin
USB	6	I	USB charge input voltage , connect to USB port positive power output	1 µF(minimum) capacitor to AGND1 pin, to minimize over-voltage transients during USB power hot-plug events.
AC	7	I	Adapter Charge Input Voltage, connect to AC_DC adapter positive output terminal (DC voltage)	1 µF(minimum) capacitor to AGND1 pin to minimize over-voltage transients during AC power hot-plug events.
OUT	8, 9	O	Power path output. Connect to System main power rail (system power bus)	10 µF capacitor to AGND1 pin
LDO_PM	10	O	General purpose LDO output	1 µF(minimum) capacitor to AGND1 pin
ISET1	11	I	Current set point when charging in auto mode with AC selected. Pre-charge and charge termination set point for all charge modes	External resistor from ISET1 pin to AGND1 pin sets charge current value
TS	12	I/O	Temperature Sense Input, current source output	Connect to battery pack thermistor to sense battery pack temperature
TMR	13	I	Charge Safety Timer Program Input	External resistor from TMR pin to AGND1 pin sets the charge safety timer time-out value
DPPM	14	I	Dynamic Power Path Management set-point	External resistor from DPPM pin to AGND1 pin sets the DPPM regulation threshold. 1 nF (minimum) capacitor to from DPPM to AGND1 sets BAT to OUT short circuit blanking delay when battery is hot-plugged into system

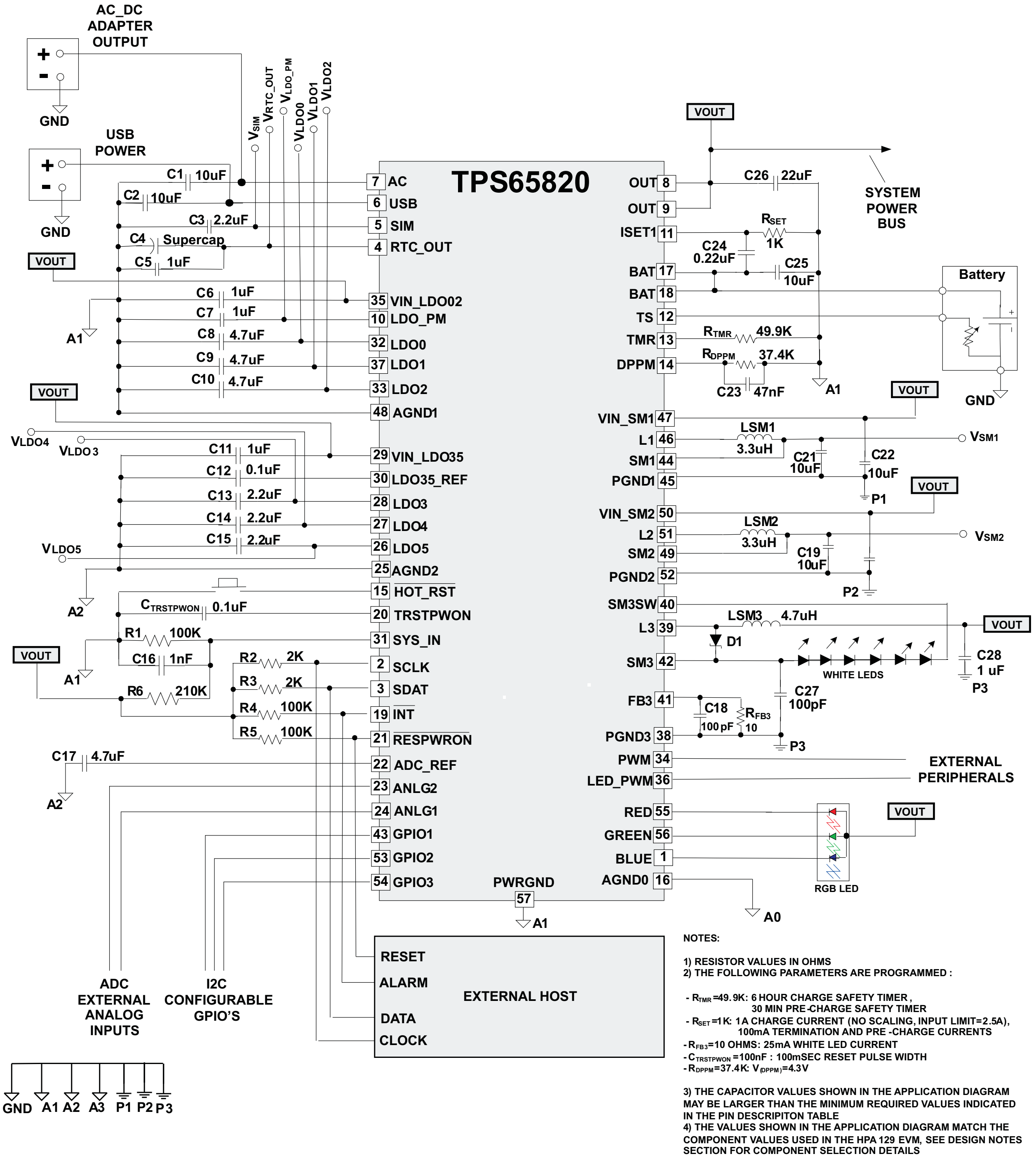
PIN ASSIGNMENT (continued)

NAME	PIN	I/O	DESCRIPTION	EXTERNAL REQUIRED COMPONENTS (SEE APPLICATION DIAGRAM)
HOT_RST	15	I/O	Hardware reset input, reset generated when connected to ground	Connect to an external push-button switch
AGND0	16	I	Analog ground connection	Connect to analog ground plane
BAT	17, 18	I/O	Battery power	Connect to battery positive terminal. Connect 10 µF capacitor (minimum) from BAT pin to AGND1 pin
$\overline{\text{INT}}$	19	O	Interruption pin, open-drain output	Connect 100K external pull-up resistor between $\overline{\text{INT}}$ and OUT $\overline{\text{INT}}$ pin is LO when interrupt is requested by TPS65820.
TRSTPWON	20	I	System Reset pulse width setting	100 nF (minimum) capacitor to AGND1. External capacitor from TRSTPWON pin to AGND1 pin sets $\overline{\text{RESPWRON}}$ pulse width
$\overline{\text{RESPWRON}}$	21	O	System Reset, open drain output	100K external pull-up resistor to OUT. $\overline{\text{RESPWRON}}$ pin is LO when TPS65820 is resetting the system.
ADC_REF	22	I/O	ADC internal reference filter or ADC external reference input	4.7 µF (minimum) to 10 µF (maximum) capacitor connected to AGND2 pin
ANLG2	23	I	Analog input to ADC, programmable current source output	Can be used to monitor additional system or pack parameters
ANLG1	24	I	Analog input to ADC, programmable current source output	Can be used to monitor additional system or pack parameters
AGND2	25	I	Analog ground pin	Connect to analog ground plane
LDO5	26	O	LDO5 Output	2.2 µF (minimum) capacitor to AGND2
LDO4	27	O	LDO4 Output	2.2 µF (minimum) capacitor to AGND2
LDO3	28	O	LDO3 Output	2.2 µF (minimum) capacitor to AGND2
VIN_LDO35	29	I	Input to LDO'S 3 to 5	1 µF (minimum) decoupling capacitor to AGND2
LDO35_REF	30	I	Linear regulators LDO3-5 reference filter	100 nF capacitor to AGND2
SYS_IN	31	I	System power bus low voltage detection	External resistive divider sets minimum system operational voltage. TPS65820 enters sleep mode when voltage below minimum system voltage threshold is detected. 1 nF filter capacitor to AGND1 recommended.
LDO0	32	O	LDO0 output, fixed voltage	1 µF(minimum) capacitor to AGND1
LDO2	33	O	LDO2 output	1 µF(minimum) capacitor to AGND1
PWM	34	O	PWM driver output, open drain.	Can be used to drive a vibrator or other external functions
VIN_LDO02	35	I	Positive supply input for LDO0,LDO1, LDO2	1 µF (minimum) decoupling capacitor to AGND1
LED_PWM	36	O	PWM driver output, open drain.	Can be used to drive a keyboard backlight LED
LDO1	37	O	LDO1 output	1 µF (minimum) capacitor to AGND1
PGND3	38	I	White LED driver power ground input.	Connect to a power ground plane
L3	39	O	Drain of the integrated boost power stage switch	4.7 µH inductor to OUT pin, external Schottky diode to SM3 pin
SM3SW	40	I	Integrated White LED duty cycle switch input	Connect to negative side of external LED ladder
FB3	41	I/O	White LED duty cycle switch output, LED current setting	External resistor from FB3 pin to PGND3 pin sets LED peak current. Connect 100 pF (minimum) filter capacitor to PGND3 pin.
SM3	42	I	White LED driver output over-voltage detection	Connect 1 µF capacitor to PGND3 pin. Connect SM3 pin to the positive side of white LED ladder.
GPIO1	43	I/O	General purpose programmable I/O	Example: External Interrupt request to host ($\overline{\text{INT}}$:HI→LO)
SM1	44	I	SM1 synchronous buck converter output voltage sense	LC filter: 10 µF capacitor to PGND1 pin
PGND1	45	I	SM1 synchronous buck converter power ground	Connect to Power ground plane
L1	46	O	SM1 synchronous buck converter power stage output	3.3 H inductor to SM1 pin

PIN ASSIGNMENT (continued)

NAME	PIN	I/O	DESCRIPTION	EXTERNAL REQUIRED COMPONENTS (SEE APPLICATION DIAGRAM)
VIN_SM1	47	I	SM1 synchronous buck converter positive supply input	10 µF capacitor to PGND1 pin
AGND1	48	I	Analog ground pin	Connect to analog ground plane
SM2	49	I	SM2 synchronous buck converter output voltage sense	LC filter: 10 µF capacitor to PGND2 pin
VIN_SM2	50	I	SM2 synchronous buck converter positive supply input	10 µF capacitor to PGND2 pin
L2	51	O	SM2 synchronous buck converter power stage output	3.3 µH inductor to SM2 pin
PGND2	52		SM1 synchronous buck converter power ground	Connect to Power ground plane
GPIO2	53	I/O	General purpose programmable	I/O Example: Set SM1 and SM2 converters in stand-by mode
GPIO3	54	I/O	General purpose programmable I/O.	Example: ADC conversion start trigger.
RED	55	O	Programmable LED driver, open drain output, current sink output when active.	Connect to RED input of RGB LED
GREEN	56	O	Programmable LED driver, open drain output, current sink output when active.	Connect to GREEN input of RGB LED
Exposed Thermal Pad	57	I	There is an internal electrical connection between the exposed thermal pad and AGNDn pins of the IC. The exposed thermal pad must be connected to the same potential as the AGND1 pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the IC. AGNDn pins must be connected to a clean ground plane at all times.	

APPLICATION DIAGRAM



NOTES:

1) RESISTOR VALUES IN OHMS
2) THE FOLLOWING PARAMETERS ARE PROGRAMMED :

- R_{TMR}=49.9K: 6 HOUR CHARGE SAFETY TIMER, 30 MIN PRE-CHARGE SAFETY TIMER
- R_{SET}=1K: 1A CHARGE CURRENT (NO SCALING, INPUT LIMIT=2.5A), 100mA TERMINATION AND PRE-CHARGE CURRENTS
- R_{FB3}=10 OHMS: 25mA WHITE LED CURRENT
- $C_{TRSTPWON}$=100nF : 100mSEC RESET PULSE WIDTH
- R_{DPPM}=37.4K: $V_{(DPPM)}$=4.3V

3) THE CAPACITOR VALUES SHOWN IN THE APPLICATION DIAGRAM MAY BE LARGER THAN THE MINIMUM REQUIRED VALUES INDICATED IN THE PIN DESCRIPITON TABLE
4) THE VALUES SHOWN IN THE APPLICATION DIAGRAM MATCH THE COMPONENT VALUES USED IN THE HPA 129 EVM, SEE DESIGN NOTES SECTION FOR COMPONENT SELECTION DETAILS

Figure 3. TPS65820 Application Diagram, Recommended External Components

TYPICAL CHARACTERISTICS – POWER PATH MANAGEMENT

Measured with Application Circuit shown in Figure 3, unless otherwise noted

SWITCHING FROM AC TO BATTERY ON AC REMOVAL

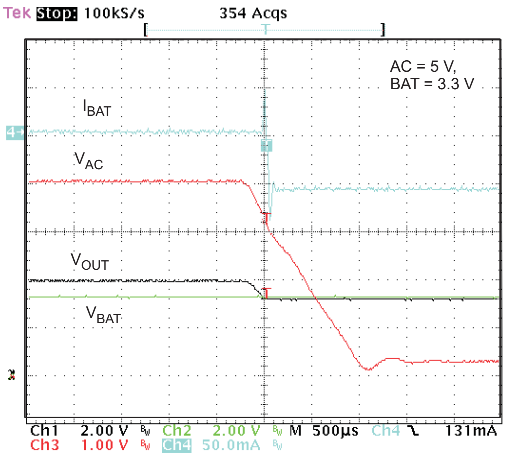


Figure 4.

SWITCHING FROM USB TO BATTERY ON AC REMOVAL

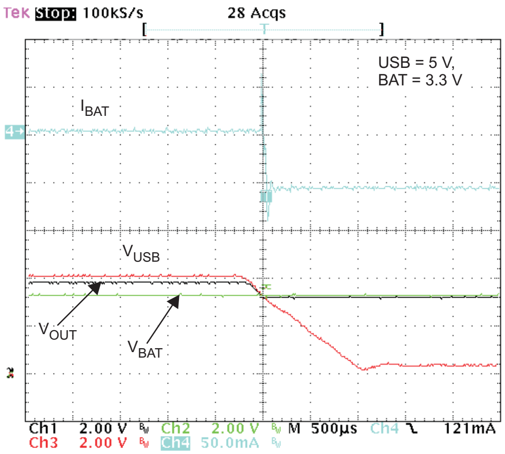


Figure 5.

TYPICAL CHARACTERISTICS – LINEAR REGULATORS 0, 1, 2

Measured with Application Circuit shown in Figure 3, unless otherwise noted

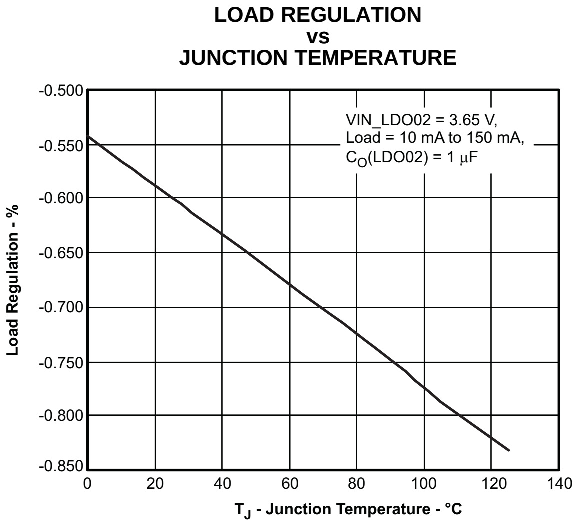


Figure 6.

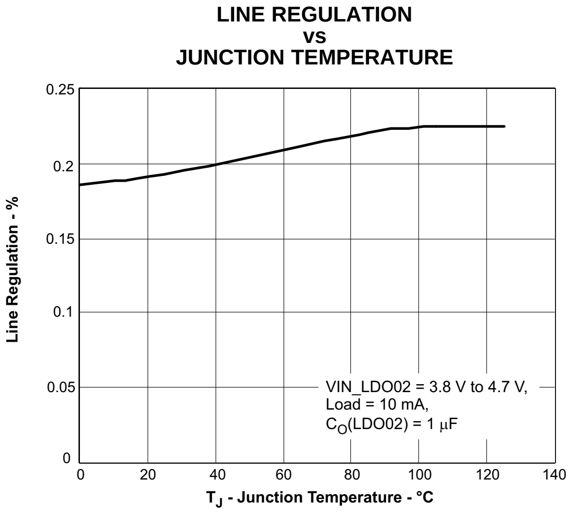


Figure 7.

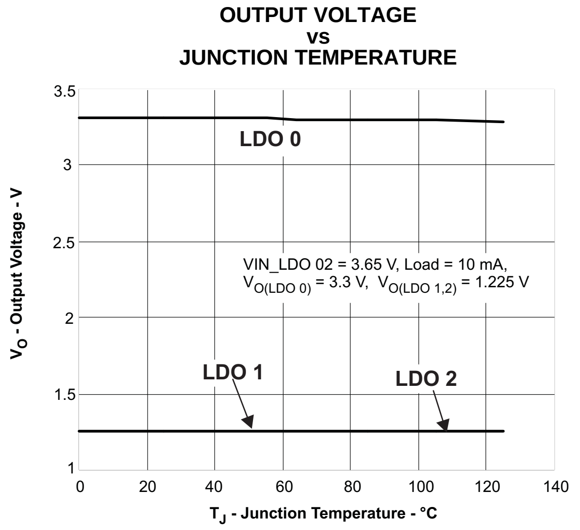


Figure 8.

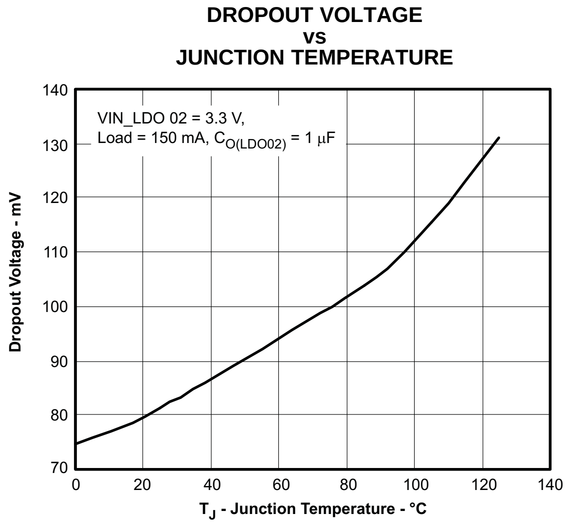


Figure 9.

TYPICAL CHARACTERISTICS – LINEAR REGULATORS 3, 4, 5

Measured with Application Circuit shown in Figure 3, unless otherwise noted

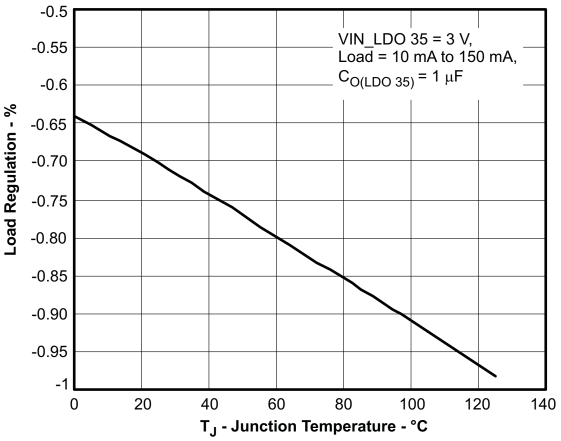

LOAD REGULATION
vs
JUNCTION TEMPERATURE

Figure 10.

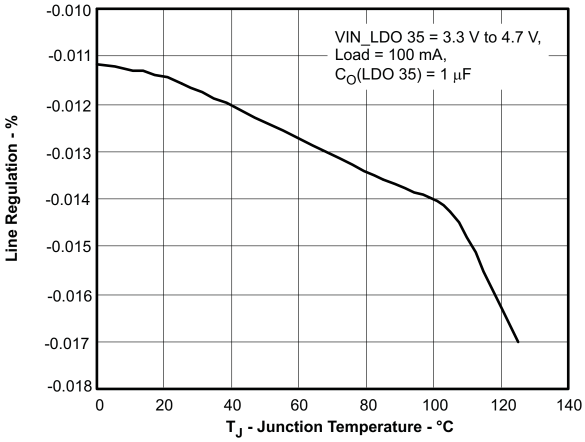

LINE REGULATION
vs
JUNCTION TEMPERATURE

Figure 11.

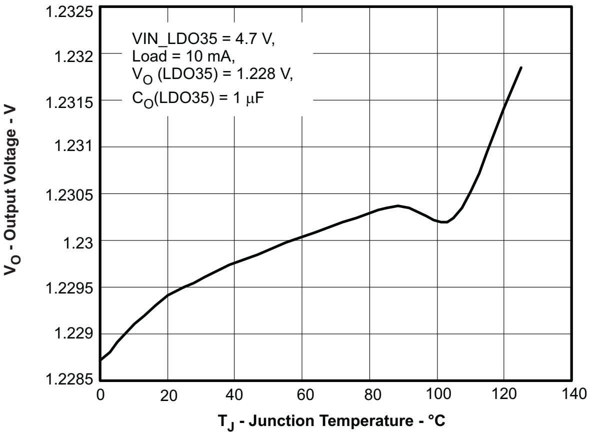

OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

Figure 12.

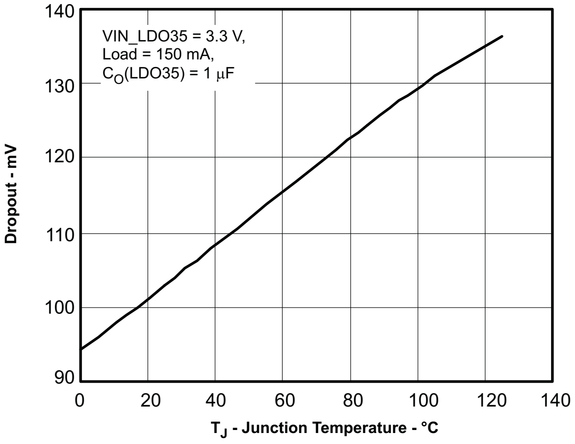

DROPOUT VOLTAGE
vs
JUNCTION TEMPERATURE

Figure 13.

TYPICAL CHARACTERISTICS – SM1 AND SM2 BUCK CONVERTERS

Measured with Application Circuit shown in Figure 3, unless otherwise noted

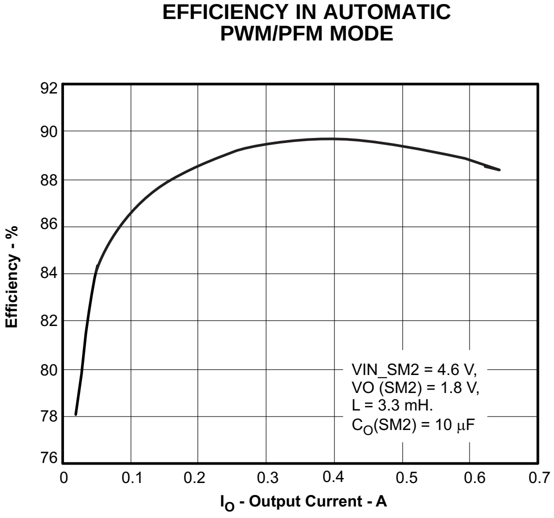


Figure 14.

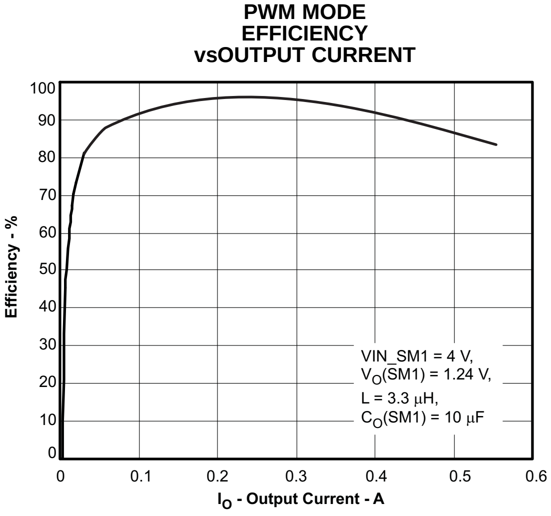


Figure 15.

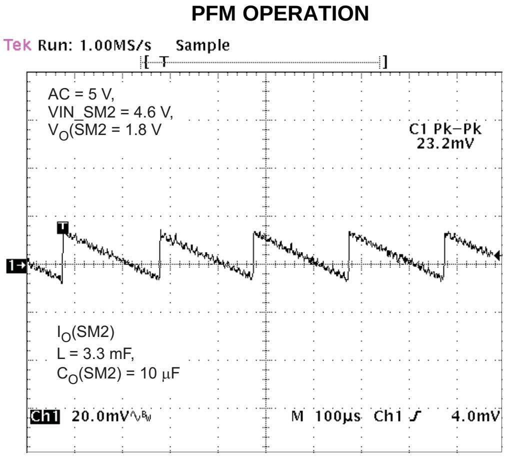


Figure 16.

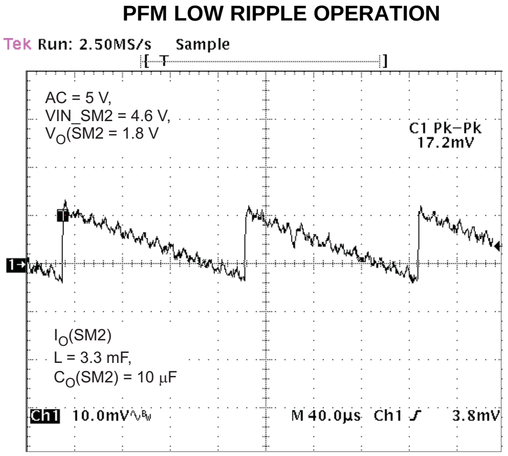


Figure 17.

TYPICAL CHARACTERISTICS – DRIVERS

Measured with Application Circuit shown in Figure 3, unless otherwise noted

LINE TRANSIENT

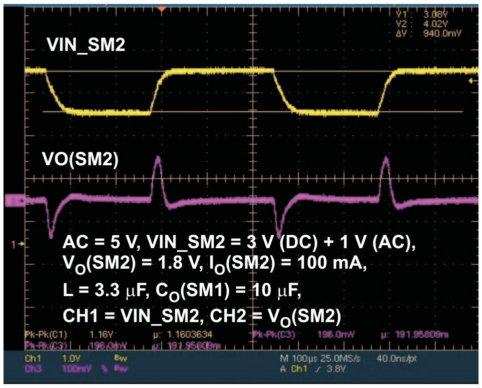


Figure 18.

LOAD TRANSIENT

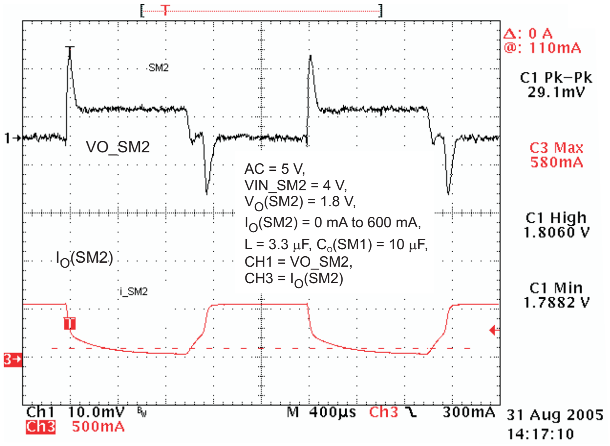


Figure 19.

TRANSIENT - SM1 STARTUP

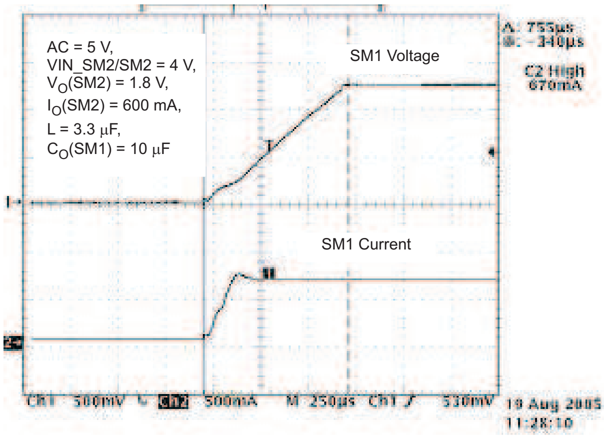


Figure 20.

TRANSIENT - SM2 STARTUP

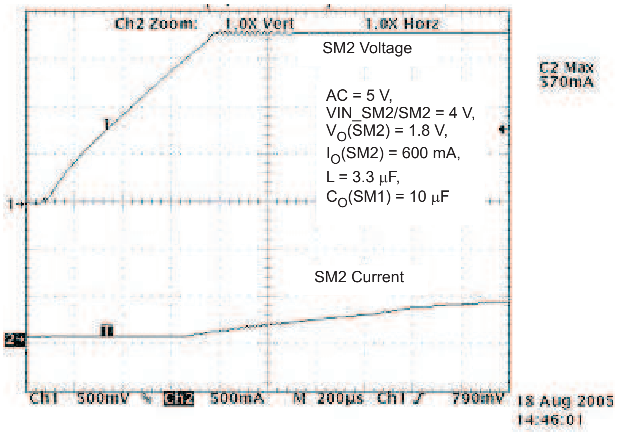


Figure 21.

TYPICAL CHARACTERISTICS – DRIVERS (continued)

Measured with Application Circuit shown in Figure 3, unless otherwise noted

**SM3 WHITE LED DRIVER
SOFT START**

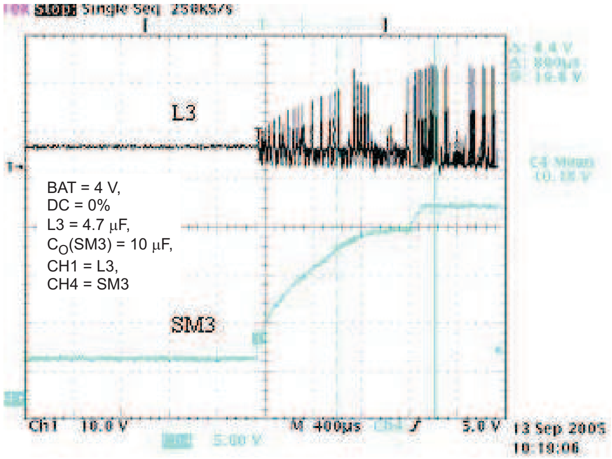


Figure 22.

**SM3 LED CURRENT
vs
PWM DUTY CYCLE**

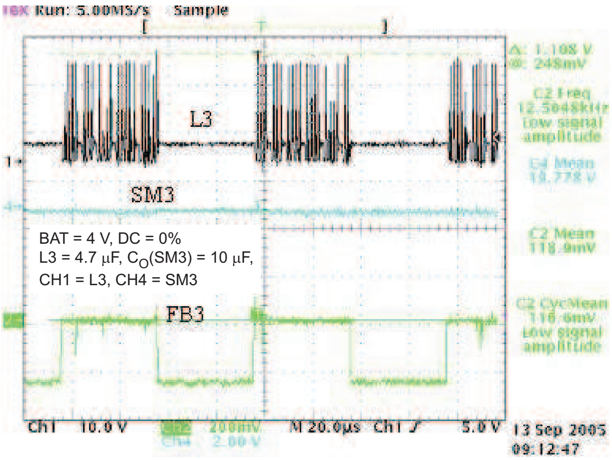


Figure 23.

SERIAL INTERFACE

Overview

The TPS65820 is compatible with a host-controlled environment, with internal parameters and status information accessible via an I2C interface. An I2C communication port provides a simple way for an I2C compatible host to access system status information and reset fault modes, functioning as a SLAVE port enabling I2C compatible hosts to WRITE to or to READ from internal registers. The TPS65820 I2C port is a 2-wire bidirectional interface using SCL (clock) and SDA (data) pins; the SDA pin is open drain and requires an external pull-up. The I2C is designed to operate at SCL frequencies up to 400 kHz. The standard 8 bit command is supported, the CMD part of the sequence is the 8 bit register address to READ from or to WRITE to.

Register Default Values

The internal TPS65820 registers are loaded during the initial power-up from an internal , non-volatile memory bank. The power-up default values are described in the sections detailing the registers functionality.

The register contents remain intact as long as OUT pin voltage remains above the internal UVLO threshold, V_{UVLO} When the OUT pin voltage falls below the VUVLO threshold all register bits are reset to the internal power up default.

I^{2}C Address

The I2C specification contains several global addresses, which the slaves on the bus are required to respond to. The TPS65820 will only respond (ACK) to addresses: 0x90 and 0x91 and will not respond (NACK) to any other address.

Table 1. TPS65820 I^{2}C Read/Write Address

BYTE	BIT							
	MSB	6	5	4	3	2	1	LSB
TPS65820 I2C WRITE ADDRESS	1	0	0	1	0	0	0	0
TPS65820 I2C READ ADDRESS	1	0	0	1	0	0	0	1
I/O DATA BUS	B7	B6	B5	B4	B3	B2	B1	B0

Incremental Read

The TPS65820 does not support incremental read operations. Each register must be accessed in a single read operation.

I^{2}C Bus Release

The TPS65820 I2C engine does not create START or STOP states on the I2C bus during normal operation.

Sleep Mode Operation

When the sleep mode is set SDAT is held LO by the TPS65820. The overall system operation is not affected, as in sleep mode all TPS65820 integrated supplies are disabled and no power is available for any external devices connected to the TPS65820 SDAT pin. When sleep mode ends the SDAT pin is released before the TPS65820 integrated regulated supplies are enabled. See section on **TPS65820 operating modes** for additional details on sleep mode operation .

I^{2}C Bus Error Recovery

The I2C bus specification does not define a method to be used when recovering from a host side bus error. During a read operation the SDA pin can be left in a LO state if the host has not sent enough SCL pulses to complete a transaction (i.e., host side bus error). The TPS65820 will clear any SDA LO condition if 10 SCL pulses are sent by the host, enabling recovery from host side bus error events.

I2C Communication Protocol

The following conventions will be used when describing the communication protocol:

Table 2. I^{2}C Naming Conventions Used

CONDITION	CODE
START sent from host	S
STOP sent from host	P
TPS65820 I2C slave address sent from host, bus direction set from host to TPS65820 (WRITE)	hA0
TPS65820 register address sent from TPS65820, bus direction is from TPS65820 to host (READ)	hA1
Non-valid I2C slave address sent from host	hA_N
Valid TPS65820 register address sent from host	HCMD
Non-valid TPS65820 register address sent from host	HCMD_N
I/O data byte (8 bits) sent from host to TPS65820	hDATA
I/O data byte (8 bits) sent from TPS65820 to host	bqDATA
Acknowledge (ACK) from host	hA
Not acknowledge (NACK) from host	hN
Acknowledge (ACK) from TPS65820	bqA
Not acknowledge (NACK) from TPS65820	bqN

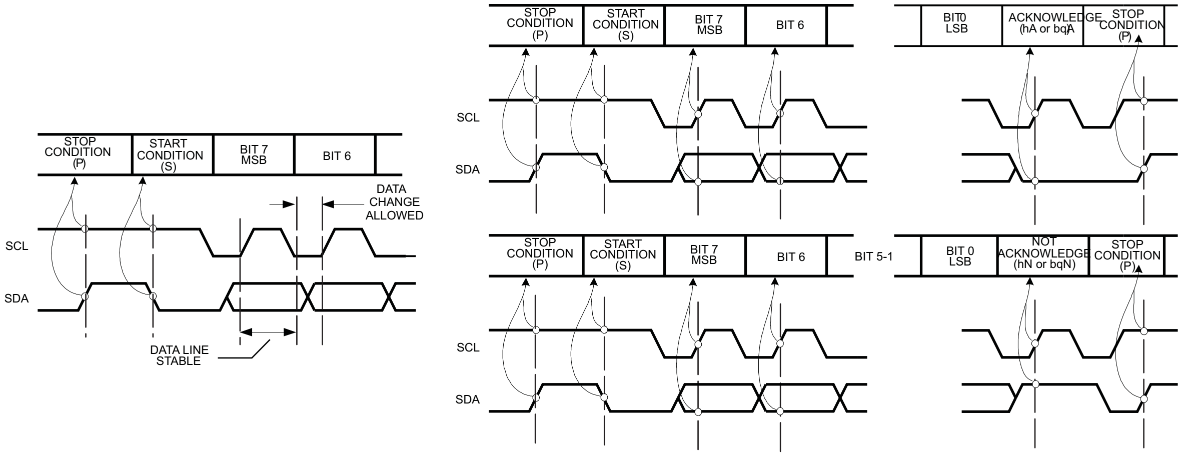


Figure 24. I^{2}C operation waveforms

For normal data transfers, SDA is allowed to change only when SCL is low, and one clock pulse is used per bit of data. The SDA line must remain stable whenever the SCL line is high, as SDA changes when SCL is high are reserved for indicating the start and stop conditions. Each data transfer is initiated with a start condition and terminated with a stop condition.

When addressed, the TPS65820 device generates an acknowledge bit after the reception of each byte by pulling the SDA line Low. The master device (microprocessor) must generate an extra clock pulse that is associated with the acknowledge bit. After the acknowledge/not acknowledge bit the TPS65820 leaves the data line high, enabling a STOP condition generation.

I^{2}C Read and Write Operations

The TPS65820 supports the standard I2C one byte Write. The basic I2C read protocol has the following steps:

- Host sends a start and sets TPS65820 I2C slave address in write mode
- TPS65820 ACKs that this is a valid I2C address and that the bus is configured for write
- Host sends TPS65820 register address
- TPS65820 ACKs that this is a valid register and stores the register address to be read
- Host sends a repeated start and TPS65820 i2c slave address, reconfiguring the bus for read
- TPS65820 ACKs that this is a valid address and that bus is reconfigured
- Bus is in read mode, TPS65820 starts sending data from selected register

The I2C write protocol is similar to the read, without the need for a repeated start and bus being set in write mode. In a WRITE it is not necessary to end each 1 byte WRITE command with a STOP, a START will have the same effect (repeated start).

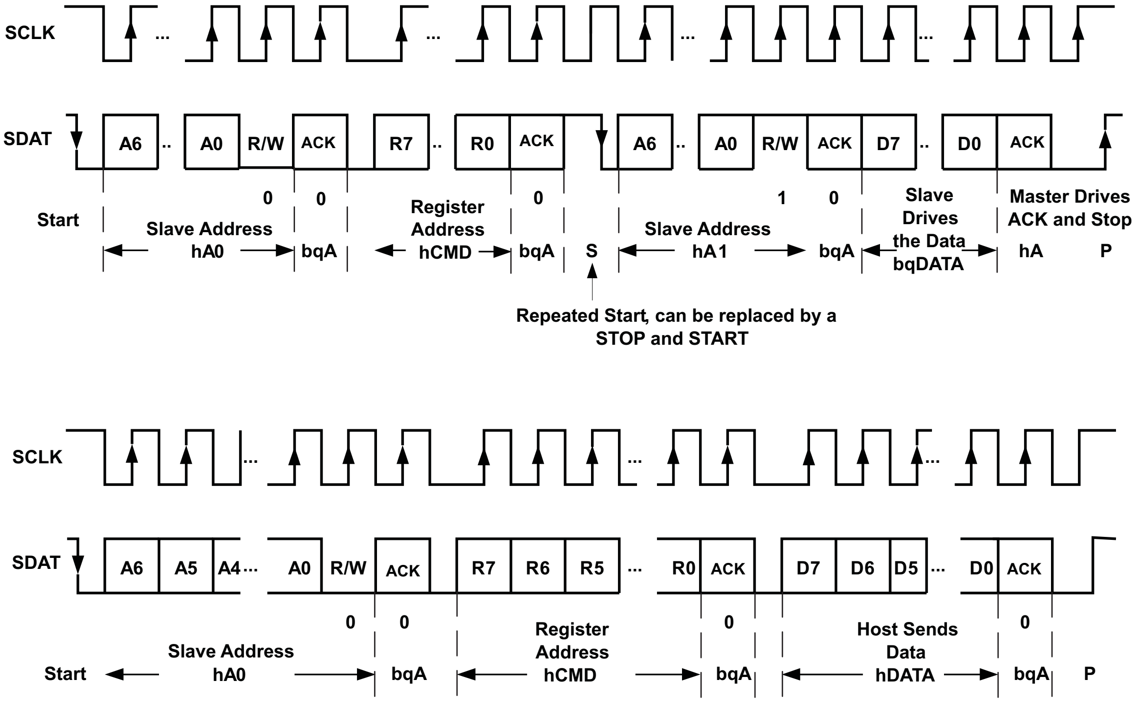


Figure 25. I^{2}C read and write operations

The host can complete a READ or a WRITE sequence with either a STOP or a START.

Valid Write Sequences

The TPS65820 always ACKs its own address. If the CMD points to an allowable READ or WRITE address, the bq writes the address into its RAM address register and sends an ACK. If the CMD points to a non-allowed address, bq does NOT write the address into its RAM address register, and sends an NACK.

S	hA0	bqA		
S	hA0	bqA	hCMD	bqA
S	hA0	bqA	hCMD_N	bqN

One Byte Write

The data is written to the addressed register when the bq ACK ending the one byte write sequence is received. The host can cancel a WRITE by sending a STOP or START before the trailing edge of the bq ACK clock pulse.

S	hA0	bqA	hCMD	bqA	hDATA	bqA

Valid Read Sequences

The TPS65820 always ACKs its own address.

S	hA1	bqA

Upon receiving hA1, TPS65820 starts at wherever the RAM address register is pointing. The START and the STOP both act as priority interrupts. If the host has been interrupted and is not sure where it left off it can send a STOP and reset the TPS65820 state machine to the WAIT state; once in WAIT state TPS65820 will ignore all activity on the SCL and SDA lines until it receives a START. A repeated START and START in the I2C specification are both treated as a START.

S	hA0	bqA	hCMD	bqA	P					
S	hA0	bqA	hCMD	bqA	S	hA1	bqA	bqDATA	hN	P
S	hA1	bqA	bqDATA	hN	P					

Non-Valid Sequences

Incremental read sequences

S	hA1	bqA	bqDATA	hA	bqDATA	hA	bqDATA	hA	bqDATA	hA	...	bqDATA	hA	P

START and non-hA0 or non-hA1 Address

A START followed by an address which is not bqA0 or bqA1 will be NACKED

S	hA_N	bqN

Attempt to Specify Non-Allowed READ Address

If the CMD points to a non-allowed READ address (reserved registers) , bq will send a NACK back to the host and it will not load the address in the RAM address register. Note that TPS65820 NACKS whether a stop is sent or not.

S	hA0	bqA	hCMD_N	bqN	P
S	hA0	bqA	hCMD_N	bqN	

Attempt to Specify Non-Allowed WRITE Address

If the host attempts to WRITE to a READ-ONLY or non-accessible address TPS65820 ACKS the CMD containing the allowed READ address, loads the address into the address register and NACKS after the host sends the next data byte. After issuing the NACK TPS65820 returns to WAIT state. A subsequent hA1 READ could read this address.

S	hA0	bqA	hCMD	bqA	hDATA	bN

TPS65820 INTERNAL REGISTER MAP

hex	NAME	DESCRIPTION	ADDITIONAL DETAILS
0	RESERVED_01	RESERVED	FACTORY ONLY
1	RESERVED_02	RESERVED	FACTORY ONLY
2	PGOOD	Output voltage status for linear regulators and dc/dc buck converters	
3	INTMASK1	Interrupt request masking settings	
4	INTMASK2	Interrupt request masking settings	
5	INT_ACK1	Masked interrupt request register, latched	
6	INT_ACK2	Masked interrupt request register, latched	
7	PGOODFAULT_MASK	System Reset masking settings	
8	SOFT_RESET	Generates a software reset	
9	CHG_CONFIG	Battery charger configuration	
A	CHG_STAT	Battery charger status	
B	EN_LDO	Linear regulator ON/OFF control	
C	LDO12	LDO1 and LDO2 output voltage setting	
D	LDO3	LDO3 output voltage settings	
E	LDO4	LDO4 output voltage settings	
F	LDO5	LDO5 output voltage settings	
10	SM1_SET1	SM1 Buck converter ON/OFF control and output voltage setting, normal mode	
11	SM1_SET2	SM1 Buck converter configuration	
12	SM1_STANDBY	SM1 Buck converter standby mode ON/OFF and standby output voltage setting	
13	SM2_SET1	SM2 Buck converter ON/OFF control and output voltage setting, normal mode	
14	SM2_SET2	SM2 Buck converter configuration	
15	SM2_STANDBY	SM2 Buck converter standby mode ON/OFF and standby output voltage setting	
16	SM3_SET	SM3 White LED driver ON/OFF control and settings	
17	RGB_FLASH	Overall RGB driver timing settings	
18	RGB_RED	RGB driver : RED duty cycle and output current setting	
19	RGB_GREEN	RGB driver : GREEN duty cycle and output current setting	
1A	RGB_BLUE	RGB driver : BLUE duty cycle and output current setting	
1B	GPIO12	GPIO1 and GPIO2 configuration	
1C	GPIO3	GPIO2 and GPIO3 configuration, battery charge voltage selection	
1D	PWM	PWM output configuration	
1E	ADC_SET	ADC On/OFF control, ADC configuration	
1F	ADC reading_hi	ADC data output	
20	ADC reading_lo	ADC data output	
21	DHILIM1	ADC Maximum threshold setting	
22	DHILIM2	ADC Maximum threshold setting	
23	DLOLIM1	ADC Minimum threshold setting	
24	DLOLIM2	ADC Minimum threshold setting	
25	ADC_DELAY	ADC configuration: conversion delay	
26	ADC_WAIT	ADC configuration: wait and repeat operation	
27	LED_PWM	LED_PWM configuration	
2E	RESERVED_03	RESERVED	FACTORY ONLY

FUNCTIONALITY REFERENCE GUIDE – HOST INTERFACE AND SYSTEM SEQUENCING

INTERRUPT CONTROLLER , OPEN-DRAIN OUTPUT (INT)					
System Parameters Monitored by Interrupt Controller					Power up default
Supply Output Power Good Fault Detection[1]	System Status Modification	ADC status	Charger Status Transition	Input and Output Power Transition	
SM1, SM2, SM3, LDO1, LDO2, LDO3, LDO4, LDO5	Thermal Fault or GPIO 1,2 configured as external interrupt request	ADC conversion end ADC Input out of range External resistive load connected to ANLG1	Charge: Pre↔ Fast ↔Done DPPM:on ↔ off Charge Suspend: on ↔ off Thermal Foldback: on ↔ off	AC detected: yes ↔ no USB detected: yes ↔ no Input OVP: yes ↔ no System Power: AC ↔ USB	All interrupt controller inputs set to non-masked
Can be masked Individually via I2C. Blanked during initial power up	Can be masked Individually via I2C		Can be masked as a group via a single I2C mask register bit		

[1] For all supplies (except) for SM3 an output fault is detected if the output voltage is below 90% of the programmed regulation voltage. In the SM3 converter an output fault indicates that the output OVP threshold was reached.

EVENTS TRIGGERING TPS65820 OPERATING MODE CHANGES				
EVENT	POWER GOOD FAULT DETECTION[1]	THERMAL FAULT	HARDWARE RESET	SOFTWARE RESET
How transition is triggered	Integrated regulator output voltage below target value: SM1, SM2, SM3, LDO1, LDO2,LDO3, LDO4, LDO5	Internal IC junction temperature	Using $\overline{\text{HOT\_RST}}$ control pin	I2C register control bit
Operating mode change	Sets Sleep mode or starts a new power-up cycle when power good fault is detected (see state machine diagram).	Sets Sleep mode when thermal fault is detected	Generates external host reset pulse at pin $\overline{\text{RESPWON}}$ when $\overline{\text{HOT\_RST}}$=LO.	Generates external host reset pulse at pin $\overline{\text{RESPWON}}$ when I2C control bit is set.
	Power good fault detection comparators are blanked during initial power-up.	Input and Battery power cycling required to exit sleep	Pulse duration set by external capacitor.	Pulse duration set by external capacitor.
Controls	Can be masked Individually via I2C.	Fixed Internal Threshold	External Input	Set via I2C

[1] For all supplies (except) for SM3 an output fault is detected if the output voltage is below 90% of the programmed regulation voltage. In the SM3 converter an output fault indicates that the output OVP threshold was reached.

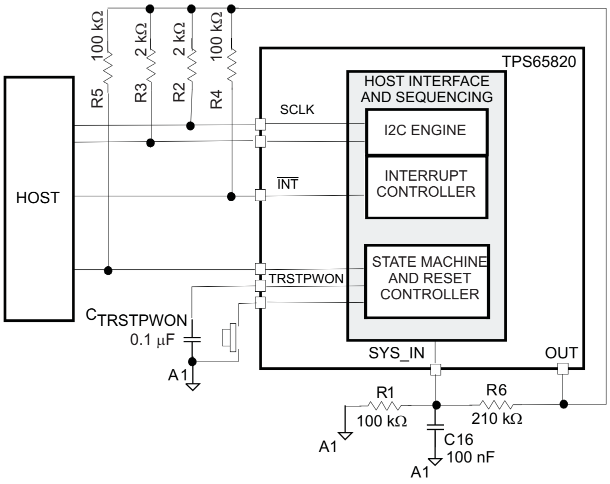


Figure 26. Required External Components, Recommended Values, External Connections

INTERRUPT CONTROLLER AND SYSTEM SEQUENCING

Overview

The TPS65820 has two dedicated internal controllers that execute the host interface and system sequencing tasks: a sequencing controller and an interrupt controller.

The sequencing controller monitors internal and system parameters and defines the sequencing of the internal power supplies during power up and power down / power fault events, and executes specific internal power supply reset operations under external hardware control or host software commands.

The following parameters are monitored by the sequencing controller :

- System power bus voltage (at SYS_IN pin) , input supply voltage, battery pack voltage
- TPS65820 thermal fault status
- Integrated supply status

The interrupt controller monitors multiple system status parameters and signals to the host when one of the monitored parameters toggled, as a result of a system status change. The interrupt controller inputs include all the parameters monitored by the sequencing controller plus:

- Charger status
- Battery pack status
- ADC status

Internal I2C registers enable masking of all the monitored parameters. Using those registers the host can select which parameters will trigger an interrupt or a power good fault. Power good faults trigger a change in the TPS65820 operating mode, as detailed in the next sections.

A simplified block diagram for the TPS65820 sections that interface to the external host is shown in Figure 27.

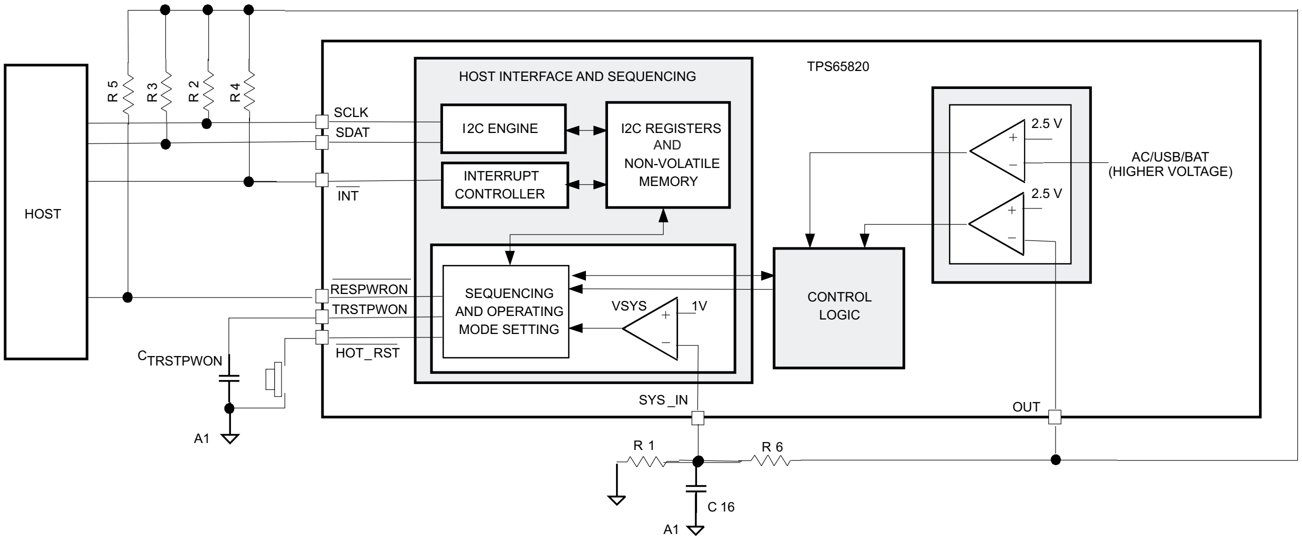
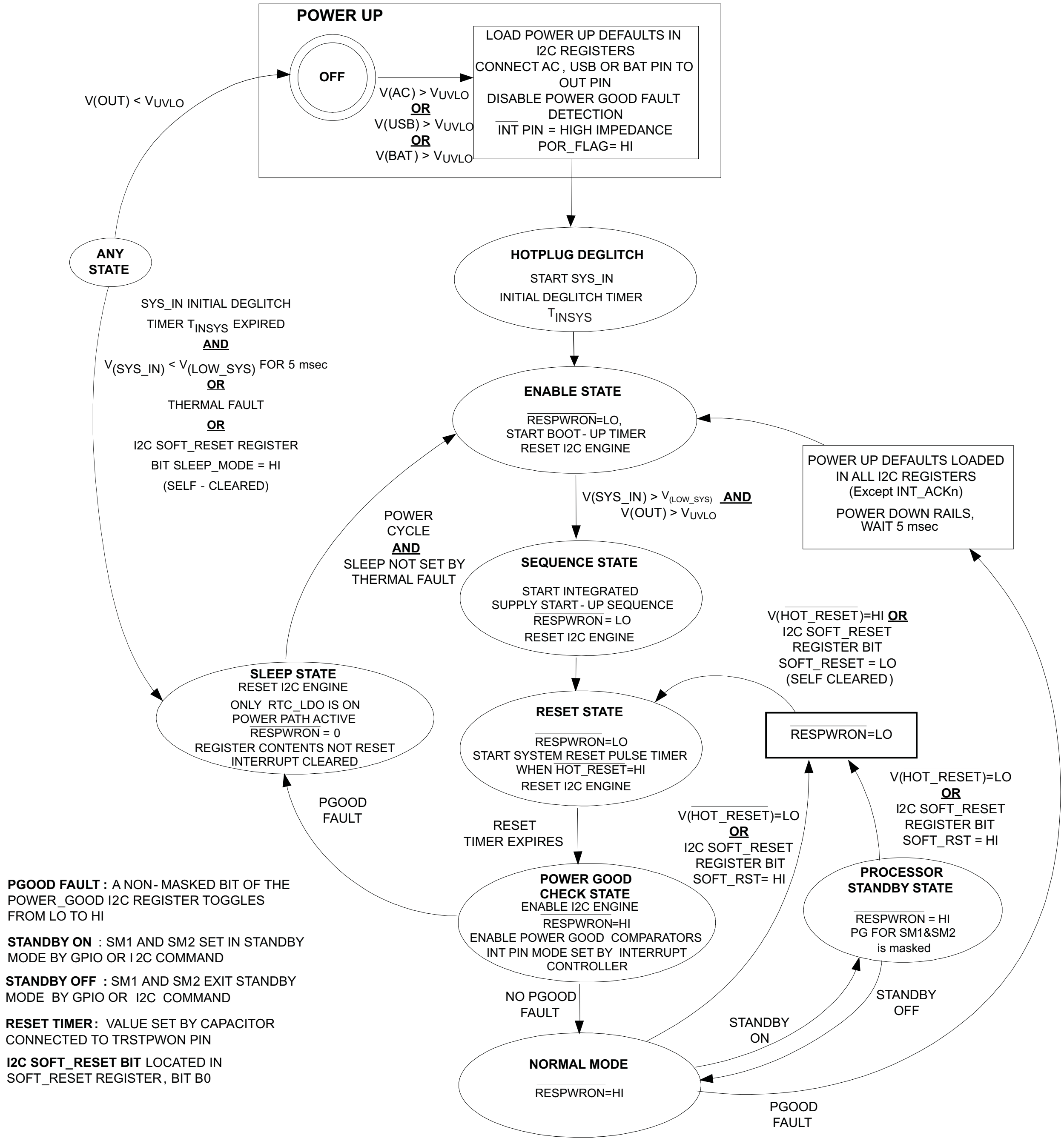


Figure 27. Simplified Block Diagram

SYSTEM SEQUENCING AND TPS65820 OPERATING MODES

The TPS65820 has a state machine that controls the device power up and power down sequencing. The main operating modes are shown in the state diagram below:



PGOOD FAULT : A NON- MASKED BIT OF THE POWER_GOOD I2C REGISTER TOGGLES FROM LO TO HI

STANDBY ON : SM1 AND SM2 SET IN STANDBY MODE BY GPIO OR I 2C COMMAND

STANDBY OFF : SM1 AND SM2 EXIT STANDBY MODE BY GPIO OR I2C COMMAND

RESET TIMER: VALUE SET BY CAPACITOR CONNECTED TO TRSTPWON PIN

I2C SOFT_RESET BIT LOCATED IN SOFT_RESET REGISTER, BIT B0

Figure 28. TPS65820 State Diagram

POWER-UP– If the AC, USB and BAT pin voltages are below the internal UVLO threshold V_{UVLO} (2.5 V typ) all IC blocks are disabled and the TPS65820 is not operational, with all functions OFF. When an external power source or battery with voltage greater than the V_{UVLO} voltage threshold is applied to AC/USB or BAT pins the internal TPS65820 references are powered up, biasing internal circuits. When all the main internal supply rails are active the TPS65820 I2C registers are set to the power-up default values, shown in Table 3:

Table 3. Integrated Supply and Drivers Power-Up Defaults

SUPPLY	POWER-UP DEFAULT	OTHER BLOCKS	POWER-UP DEFAULT
LDO0	OFF, 3.3 V	POWER PATH	INPUT TO SYSTEM
LDO1	2.85V, ON	PWM	OFF
LDO2	3.3 V, ON	PWM_LED	OFF
LDO3	1.25 V, ON	GPIO1	INPUT
LDO4	2.75 V, ON	GPIO2	INPUT
LD05	2.81 V, ON	GPIO3	INPUT
SIM	1.8 V, OFF	ADC	OFF
RTC_OUT	ON, 3.1 V	SM3 (WHITE LED)	OFF
LDO_PM	3.3 V, ON @ OUT POWERED	RGB DRIVER	OFF
SM1	ON, 1.24 V	INTERRUPT MASK	NONE MASKED
SM2	ON, 1.8 V	POWER GOOD MASK	ALL MASKED
CHARGER	ON		

After the internal I2C register power-up defaults are loaded the power path control logic is enabled, connecting the external power source to the OUT pin. A status flag (nRAMLOAD) is set to LO in the SOFT_RESET register, indicating that the I2C registers were loaded with the power-up defaults, and the TPS65820 enters the HOTPLUG mode.

HOTPLUG: In the HOTPLUG state an independent timer, TDGL(HOTPLUG) is started. The hotplug deglitch timer, when active (not expired), will prevent the TPS65820 from entering the SLEEP mode. This functionality guarantees avoids potential system lockup conditions caused by contact bouncing events, when the TPS65820 is initially powered by a battery pack insertion. After the hotplug deglitch timer is started the TPS65820 enters the ENABLE mode.

ENABLE : In the ENABLE mode the R$\overline{\text{ESPWRON}}$ output is set to the LO level, the $\overline{\text{INT}}$ pin mode is set to high impedance and all the power good comparators that monitor the integrated supply outputs are disabled. The ENABLE mode is used by the TPS65820 to detect when the main system power rail (OUT pin) is powered and ready to be used on the internal supply power-up. The OUT pin voltage is sensed by an internal low system voltage comparator which will hold the IC in the ENABLE mode until the system power bus voltage (OUT pin) has reached a minimum operating voltage, defined by the user. The internal comparator senses the system voltage at pin SYS_IN, and the threshold for the minimum system operating voltage at the OUT pin is set by the external divider connected from OUT pin to SYS_IN pin. The threshold voltage is calculated as follows:

$$V(OUT) = V_{(LOW\_SYS)} \times \left(1 + \frac{R6}{R1}\right): \quad \text{where R6 and R1 are external resistors, } V_{(LOW\_SYS)} = 1\text{ V typical} \tag{1}$$

The minimum system operating voltage should always be set above the internal UVLO threshold V_{UVLO}. In normal application conditions the minimum system operating voltage is usually set to a value that assures that the TPS65820 integrated regulators are not operating in the dropout region.

When the voltage at the SYS_IN pin exceeds the internal threshold $V_{(LOW\_SYS)}$ the TPS65820 is ready to start the system power sequencing, and the SEQUENCING mode is entered.

SEQUENCING– The sequencing state starts immediately after the enable state . In this mode of operation the integrated supplies are turned ON, according to the sequencing steps loaded from the internal non-volatile memory during the power-up phase. The TPS65820 sequencing timing diagram shown in figure details the internal timing delays and supply sequencing. At the end of the sequencing state the user-programmable reset timer is started, and the TPS65820 enters the reset state.

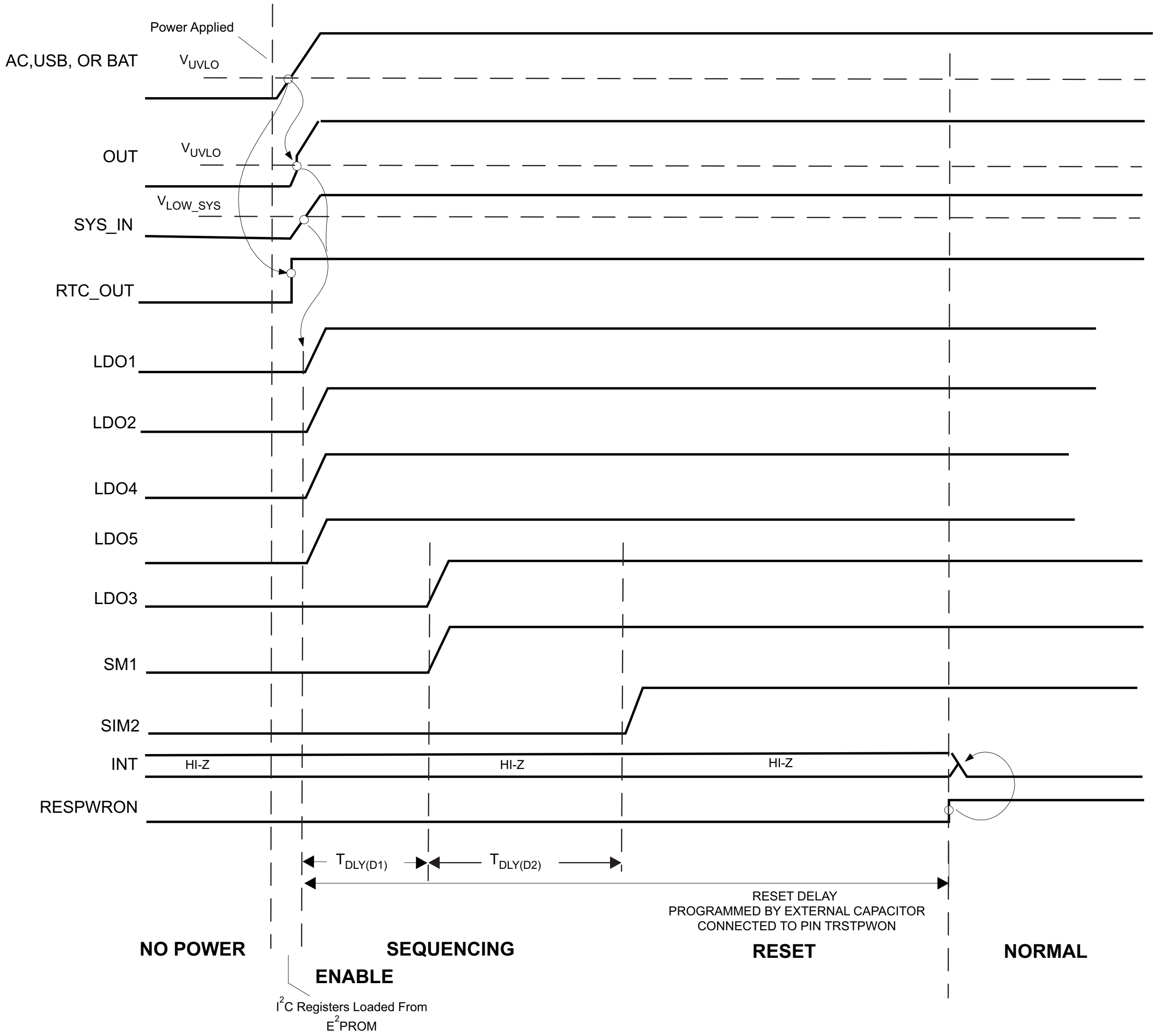


Figure 29. TPS65820 Supply Sequencing Timing

RESET– When the reset state starts the $\overline{\text{RESPWRON}}$ output is LO. The user can program the reset timer value selecting the value of the external capacitor connected to pin TRSTPWON, as shown below:

$T_{(RESET)} = K_{RESET} \times C_{TRSTPWON}$; where K_{RESET} is the reset timer constant (1 ms/nF typ)

The TPS65820 $\overline{\text{RESPWRON}}$ pin should be used to reset the external host. During the external host reset ($\overline{\text{RESPWRON}}$ = LO) the I2C SDA and SCL pins are not used to access TPS65820 internal registers. If a non-standard configuration is used to reset the system the SDA and SCL lines should not be used to communicate with the TPS65820 until $\overline{\text{RESPWRON}}$ = HI. The TPS65820 I2C engine will be kept in reset as long as $\overline{\text{RESPWRON}}$ = LO, avoiding false detection of start/stop conditions when the SDA and SCL pull-up resistors are initially powered.

The power good comparators are masked during the reset mode. The reset mode ends when the reset timer expires, and the TPS65820 goes into the power good check mode.

At the end of the reset mode an Interrupt request is sent to the Host ($\overline{\text{INT}}$: HI → LO) .

POWER GOOD CHECK– In the power good check mode the power good comparators are enabled, providing status on the integrated supplies output voltages. An output voltage will be considered as out of regulation and generate a fault condition if the output voltage is below 90% of the target output voltage regulation value. If a power good fault is detected the SLEEP mode is set, if a power good fault is not detected the NORMAL mode is set.

The individual supply power good status can be masked via an I2C register PGOODFAULT_MASK. Supplies that have their power good fault status masked will not generate a power good fault . However, the status bit for the supply indicates that the output voltage is out of regulation.

The power good mask register bits default to masked upon power up.

NORMAL MODE– If a power good fault is not present at the end of the power good check mode the NORMAL mode starts. In this mode of operation the I2C registers define the TPS65820 operation, and the host has full control on operation modes, parameter settings, etc. The normal state operation ends if a thermal fault, system low voltage fault (V(SYS_IN) < V_{LOW_SYS}) or power good fault is detected. A thermal fault or system low voltage fault sets the SLEEP mode operation, a power good fault sets the NO POWER operation mode. From the normal mode the converters SM1 and SM2 can be set in the STANDBY mode, with reduced output voltages. In NORMAL mode either an I2C register bit (SOFT_RESET register bit SOFT_RST) or a hardware input ($\overline{\text{HOT\_RESET}}$ pin set to LO) can trigger a transition to the RESET state, enabling implementation of a host reset function. In NORMAL mode an I2C register bit (SOFT_RESET register bit SLEEP_MODE) can trigger a transition to SLEEP mode.

SLEEP MODE– The SLEEP mode is set when a thermal fault or system low voltage fault is detected, under NORMAL operation mode set. This operation mode is also set when a power good fault is detected during the power good check state or via the I2C bit SLEEP_MODE. In the SLEEP mode the $\overline{\text{RESPWRON}}$ output is set to LO, and the I2C registers keep the same contents as in the state preceding SLEEP mode, with the exception of the following control bits, which are reset to the default power-up values:

1. LDO1,2,3,4,5 and RTC_OUT are enabled, SIM LDO is disabled: EN_LDO register set to default values
2. LDO0 disabled, all GPIO’s with no control function assigned: GPIO12, GPIO3 registers set to default values
3. White LED driver is set to OFF: SM3_SET register has all bits set to LO
4. RGB drivers are set to OFF: RGB_FLASH, RGB_RED, RGB_GREEN, RGB_BLUE registers are set to default values
5. PWM , PWM_LED drivers OFF: PWM, LED_PWM registers are set to default values
6. ADC engine reset to power up default: ADC_SET, ADC_DELAY, ADC_WAIT registers are set to default values

In SLEEP mode the power path and main internal blocks are still active, but the internal integrated supply sequencing is disabled. As a result of that , during SLEEP mode ALL integrated supplies (ALL LDO's, ALL Buck Converters) will be disabled, with exception of the RTC_LDO. The RTC_LDO will be ON during sleep mode if the RTC_EN bit (register EN_LDO) is set to HI. The RTC_LDO will be OFF during sleep mode if the RTC_EN bit (register EN_LDO) is set to LO.

At the end of the SLEEP mode the sequencer block will use the I2C control register values (which were reset to the default power-up values) to sequence the integrated power supplies. The SLEEP mode ends when one of the three following events happens:

1. *If SLEEP was set by thermal fault:* The SLEEP mode will end only when all external input supplies and battery pack are removed and an UVLO condition is detected by the TPS65820, setting the NO POWER mode.
2. *If SLEEP was set by a system low voltage detection , or I2C bit SLEEP_MODE , only with battery present:* Input power must be connected, setting the TPS65820 in the ENABLE mode. If no input power is inserted the battery will discharge until the TPS65820 detects an UVLO condition and enters the NO POWER mode.
3.) *If sleep was set by a system low voltage detection, power good fault or SLEEP_MODE, with battery and input power present:* all external input supplies connected to AC and USB pins must be removed, and then at least one of them reconnected to the system. The input power cycling will trigger a transition from SLEEP mode to the ENABLE mode.

PROCESSOR STANDBY STATE– This state is set using a I2C register or a GPIO configured as SM1/SM2 standby control. In standby mode operation the SM1 and SM2 voltages are set to value distinct than the normal mode output voltage, and SM1/SM2 are set to PFM mode. The standby output voltage is defined in I2C registers SM1_STANDBY and SM2_STANDBY.

TPS65820 OPERATING MODE CONTROLS

HARDWARE RESET: A dedicated control pin, $\overline{\text{HOT\_RESET}}$, enables implementation of a hardware reset function. The system reset pin $\overline{\text{RESPWRON}}$ will be set to LO when $\overline{\text{HOT\_RESET}}$ = LO for a period longer than the internal deglitch (5mSec typ). The RESET mode is started when the $\overline{\text{HOT\_RESET}}$ pin transitions from LO to HI, as shown in the state diagram.

SOFTWARE RESET: The external host can set the TPS65820 in RESET mode using the I2C register SOFT_RESET, bit B0 (SOFT_RST).

SOFTWARE SLEEP: The external host can set the TPS65820 in SLEEP mode using the I2C register SOFT_RESET, bit B6 (SLEEP_MODE).

A hardware or software reset does not affect the contents of the I2C registers.

SEQUENCING AND OPERATING MODES – I2C REGISTERS

The I2C registers that control sequencing-related functions are shown below. The HEX address for each register is shown by the register name, together with the R or W functionality for the register bits. Shaded values indicate default initial power-up values.

SOFT_RESET, ADDRESS=08, ALL BITS R/W, BITS B7/B6/B1/B0 APPLY TO SEQUENCING.

	B7	B6	B5	B4	B3	B2	B1	B0
Bit name	STBY MODE	SLEEP MODE	NOT USED	NOT USED	SM3_LF_OSc	NOT USED	nRAMLOAD	SOFT RST
Function	SET SM1 AND SM2 IN STANDBY MODE	SET TPS65820 IN SLEEP MODE	NOT USED	NOT USED	*NOT RELATED TO SEQUENCING SEE SM3 SECTION*	NOT USED	RAM RESET FLAG	SOFTWARE RESET CONTROL
When 0	NOT ACTIVE	NOT ACTIVE	NOT USED	NOT USED		NOT USED	RAM DEFAULTS LOADED	NOT ACTIVE
When 1	When 1 SET SM1 AND SM2 IN STANDBY	SET SLEEP MODE (reset to LO internally)	NOT USED	NOT USED		NOT USED	RAM DEFAULTS NOT LOADED	SET RESET MODE (reset to LO internally)

Some host algorithms need to identify when the power-up defaults are loaded in the RAM, in order to start routines that initialize specific RAM registers. If that functionality is required the nRAMLOAD bit should be set to HI by the host when entering hte NORMAL operation mode. The nRAMLOAD bit will be reset to LO by the TPS65820 when the power-up defaults are loaded in the I2C registers (V(OUT)<V_{UVLO} OR PGOOD fault detected), enabling the host algorithm to detect that the RAM registers need to be initialized.

The integrated supplies status is available in a dedicated register, shown below . The host can select which integrated supply outputs will trigger a power good fault condition using the PGOODFAULT_MASK register.

When a non-masked power good status register bit toggles state the sequence controller will generate a transition in the TPS65820 state machine, indicated as a PGOOD FAULT in TPS65820 state diagram.

The power-good status register and mask register are shown below:

SYSTEM STATUS MONITORED BY SEQUENCING CONTROLLER								
	B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
PGOOD, ADDRESS=02, ALL BITS READ ONLY - POWER UP DEFAULTS SHOW SYSTEM STATUS WHEN EXITING POWER DOWN								
Bit name	PGOOD SM1	PGOOD SM2	PGOOD SM3	PGOOD LDO1	PGOOD LDO2	PGOOD LDO3	PGOOD LDO4	PGOOD LDO5
Function	SM1 OUTPUT STATUS	SM2 OUTPUT STATUS	SM3 OVP STATUS	LDO1 OUTPUT STATUS	LDO2 OUTPUT STATUS	LDO3 OUTPUT STATUS	LDO4 OUTPUT STATUS	LDO5 OUTPUT STATUS
When 0	OK	OK	OK	OK	OK	OK	OK	OK
When 1	FAULT	FAULT	FAULT	FAULT	FAULT	FAULT	FAULT	FAULT
PGOODFAULT_MASK, ADDRESS=07, ALL BITS R/W								
Bit name	MASK_PSM1	MASK_PSM2	MASK_PSM3	MASK_PLDO1	MASK_PLDO2	MASK_PLDO3	MASK_PLDO4	MASK_PLDO5
Function	MASK PGOOD FAULT BY SM1	MASK PGOOD FAULT BY SM2	MASK PGOOD FAULT BY SM3	MASK PGOOD FAULT BY LDO1	MASK PGOOD FAULT BY LDO2	MASK PGOOD FAULT BY LDO3	MASK PGOOD FAULT BY LDO4	MASK PGOOD FAULT BY LDO5
When 0	UNMASKED	UNMASKED	UNMASKED	UNMASKED	UNMASKED	UNMASKED	UNMASKED	UNMASKED
When 1	MASKED	MASKED	MASKED	MASKED	MASKED	MASKED	MASKED	MASKED

INTERRUPT CONTROLLER

The TPS65820 has internal block and overall system status information stored in I2C status registers. The following subsystems and system parameters are monitored :

- External power supply status: AC or USB supply detected, AC or USB connected to system, AC/USB OVP
- Charger status: on/off/suspend, fast charge/pre-charge, termination detected, DPPM on, thermal loop ON
- Battery pack status: temperature, discharge on/off
- TPS65820 Thermal shutdown
- ADC status: conversion status, input out of range, ANLG1 high impedance detection
- Integrated supplies status: output out of regulation (power good fault)

The GPIO1 and GPIO2 pins can be configured as inputs, generating an interrupt request to the host ($\overline{\text{INT}}$:HI→LO) at the GPIO rising or falling edge. The host can use internal the INT_MASK I2C registers to define which of the monitored status variables will trigger an interrupt. When a non-masked system status bit toggles state the interrupt controller will issue an interrupt , following the steps below:

1. system status bits that caused the interruption are set to HI in registers INT_ACK1 and INT_ACK2
2. An interrupt is sent to the host ($\overline{\text{INT}}$:HI→LO)

Once an interrupt is sent to the host $\overline{\text{INT}}$ will be kept in the LO state and the INT_ACK registers contents are latched, holding the system status that generated the currently issued interrupt request. When an interrupt request is active ($\overline{\text{INT}}$ = LO) additional changes in non-masked status registers and control signals are ignored, and the INT_ACK registers are not updated.

The host must execute a write operation resetting the INT_ACK register bit that generated the interrupt in order to set $\overline{\text{INT}}$ = HI and enable new updates to the INT_ACK registers. If the host stops in the middle of a WRITE or READ operation the $\overline{\text{INT}}$ pin will stay at the LO level. The TPS65820 has no reset timeout; it is assumed that the host will not leave $\overline{\text{INT}}$ = LO and the status registers unread for a long time.

The non-masked I2C register bits and internal control signals will generate a new interrupt only after $\overline{\text{INT}}$ is set to HI. The non-masked power good fault register bits will generate a power good fault when any of the non-masked bits detects that the monitored output voltage is out of regulation, independently of the $\overline{\text{INT}}$ pin level.

SYSTEM STATUS — I2C REGISTERS

The I2C registers that have system status data are shown below. The HEX address for each register is shown by the register name, together with the R or W functionality for the register bits. Those registers are valid, after an initial power up, when the TPS65820 enters the normal operation mode.

SYSTEM STATUS MONITORED BY INTERRUPT CONTROLLER								
	B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
PGOOD, ADDRESS=02, ALL BITS READ ONLY - POWER UP DEFAULTS SHOW SYSTEM STATUS WHEN EXITING POWER DOWN								
Bit name	PGOOD SM1	PGOOD SM2	PGOOD SM3	PGOOD LDO1	PGOOD LDO2	PGOOD LDO3	PGOOD LDO4	PGOOD LDO5
Function	SM1 OUTPUT STATUS	SM2 OUTPUT STATUS	SM3 OVP STATUS	LDO1 OUTPUT STATUS	LDO2 OUTPUT STATUS	LDO3 OUTPUT STATUS	LDO4 OUTPUT STATUS	LDO5 OUTPUT STATUS
When 0	OK	OK	OK	OK	OK	OK	OK	OK
When 1	FAULT	FAULT	FAULT	FAULT	FAULT	FAULT	FAULT	FAULT
CHG_STAT, ADDRESS=A, ALL BITS READ ONLY – POWER UP DEFAULTS SHOW SYSTEM STATUS WHEN EXITING POWER DOWN								
Bit name	BAT_STAT(1)	INPUT _PWR	THDPPM_ON	ACPG	USBPG	STAT1	STAT2	INP_OV
Function	BATTERY DISCH STATUS	SELECTED INPUT POWER STATUS	THERMAL FAULT AND DPPM MODE	AC INPUT POWER STATUS	USB INPUT POWER STATUS	CHARGE STATUS		AC OR USB INPUT OVP DETECTION
When 0	NOT DISCHARGING	AC INPUT SELECTED	BOTH OFF	AC NOT DETECTED	USB NOT DETECTED	00=FAULT/OFF/SUSPEND, 01=DONE, 10=FAST CHG ON, 11= PRE-CHARGE		NO OVP
When 1	When 1 DISCHARGING	USB INPUT SELECTED	DPPM ON OR THERMAL ON	AC DETECTED	USB DETECTED			OVP DETECTED
ADC STATUS								
REGISTER ADC_READING_HI, B7: CONVERSION COMPLETE ; INTERNAL STATUS BITS (NO I2C REGISTER BIT AVAILABLE: INPUT OUT OF RANGE (HI OR LO), ANLG1 PIN IMPEDANCE TO AGND2 EXCEEDS 1 mΩ								
OTHER SYSTEM STATUS: THERMAL FAULT DETECTED								

(1) BAT_STAT pin does not generate an interrupt, in order to avoid oscillatory behavior when battery supplement mode is set.

INTERRUPT CONTROLLER – I²C REGISTERS

The I2C registers that control an interrupt generation (INT: HI→LO) are shown below. The HEX address for each register is shown by the register name, together with the R or W functionality for the register bits. Shaded values indicate default initial power-up values.

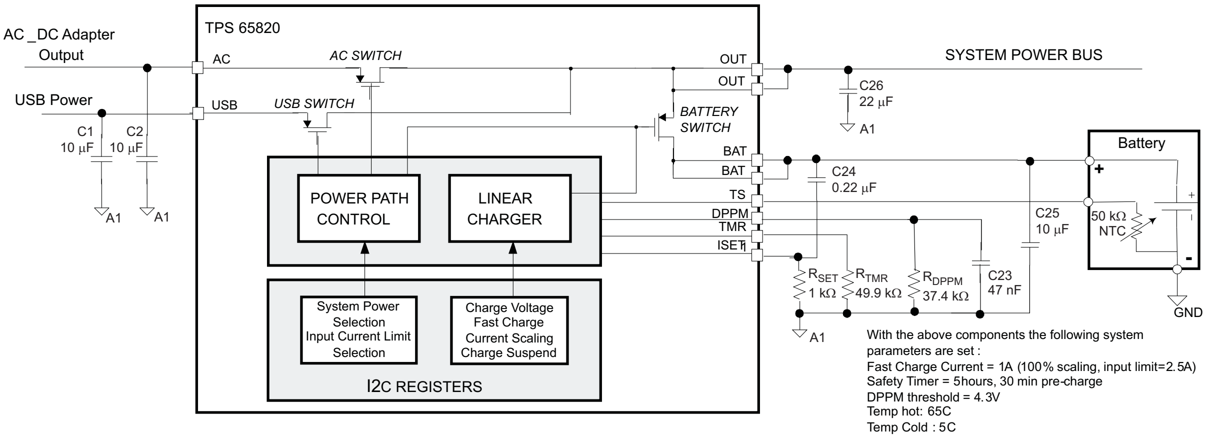
INTERRUPT AND POWER GOOD FAULT MANAGEMENT REGISTERS								
	B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
INTMASK1, ADDRESS=03, ALL BITS R/W								
Bit name	MASK_ISM1	MASK_ISM2	MASK_ISM3	MASK_ILDO1	MASK_ILDO2	MASK_ILDO3	MASK_ILDO4	MASK_ILDO5
Function	MASK INT by SM1 PGOOD FAULT	MASK INT by SM2 PGOOD FAULT	MASK INT by SM3 PGOOD FAULT	MASK INT by LDO1 PGOOD FAULT	MASK INT by LDO2 PGOOD FAULT	Mask INT by LDO3 PGOOD FAULT	MASK INT by LDO4 PGOOD FAULT	MASK INT by LDO5 PGOOD FAULT
When 0	UNMASKED	UNMASKED	UNMASKED	UNMASKED	UNMASKED	UNMASKED	UNMASKED	UNMASKED
When 1	MASKED	MASKED	MASKED	MASKED	MASKED	MASKED	MASKED	MASKED
INTMASK2, ADDRESS=04, ALL BITS R/W								
Bit name	MASK_IADC	MASK_IANLG1	MASK_IGPIO2	MASK_IGPIO1	MASK_ITHSHUT	MASK_ICHGST	MASK_IADC_HI	MASK_IADC_LO
Function	MASKS INT BY ADC END OF CONVERSION	MASKS INT BY ANLG1 HIGH IMPEDANCE	MASKS INT BY GPIO2 EDGE TRANSITION	MASKS INT BY GPIO1 EDGE TRANSITION	MASKS INT BY THERMAL FAULT	MASK INT BY CHG_STAT REGISTER BITS	MASK INT BY ADC INPUT ABOVE HI LIMIT	MASK INT BY ADC INPUT BELOW LO LIMIT
When 0	UNMASKED	UNMASKED	UNMASKED	UNMASKED	UNMASKED	UNMASKED	UNMASKED	UNMASKED
When 1	MASKED	MASKED	MASKED	MASKED	MASKED	MASKED	MASKED	MASKED
INT_ACK1, ADDRESS=05, ALL BITS R/W								
Bit name	ACK_SM1	ACK_SM2	ACK_SM3	ACK_LDO1	ACK_LDO2	ACK_LDO3	ACK_LDO4	ACK_LDO5
Function	SM1 INT REQUEST	SM2 INT REQUEST	SM3 INT REQUEST	LDO1 INT REQUEST	LDO2 INT REQUEST	LDO3 INT REQUEST	LDO4 INT REQUEST	LDO5 INT REQUEST
When 0	CLEAR FLAG	CLEAR FLAG	CLEAR FLAG	CLEAR FLAG	CLEAR FLAG	CLEAR FLAG	CLEAR FLAG	CLEAR FLAG
When 1	SM1 PGOOD FAULT GENERATED INT	SM2 PGOOD FAULT GENERATED INT	SM3 OVP FAULT GENERATED INT	LDO1 PGOOD FAULT GENERATED INT	LDO2 PGOOD FAULT GENERATED INT	LDO3 PGOOD FAULT GENERATED INT	LDO4 PGOOD FAULT GENERATED INT	LDO5 PGOOD FAULT GENERATED INT
INT_ACK2, ADDRESS=06, ALL BITS READ ONLY								
Bit name	ACK_ADC	ACK_ANLG1	ACK_GPIO2	ACK_GPIO1	ACK_THSHUT	ACK_CHGSTAT	ACK_ADC_HI	ACK_ADC_LO
Function	ADC INT REQUEST 1	ANLG1 COMPARATOR INT REQUEST	GPIO2 INT REQUEST	GPIO1 INT REQUEST	THERMAL FAULT INT REQUEST	CHARGER INT REQUEST	ADC INT REQUEST 2	ADC INT REQUEST 3
When 0	CLEAR FLAG	CLEAR FLAG	CLEAR FLAG	CLEAR FLAG	CLEAR FLAG	CLEAR FLAG	CLEAR FLAG	CLEAR FLAG
When 1	ADC DONE GENERATED INT REQUEST	ANLG1 HIGH IMPEDANCE DETECTION GENERATED INT REQUEST	GPIO2 EDGE GENERATED INT REQUEST	GPIO1 EDGE GENERATED INT REQUEST	THERMAL FAULT GENERATED INT REQUEST	CHARGER STATUS CHANGE GENERATED INT REQUEST	ADC INPUT ABOVE HI LIMIT GENERATED INT REQUEST	ADC INPUT BELOW LO LIMIT GENERATED INT REQUEST
PGOODFAULT_MASK, ADDRESS=07, ALL BITS R/W								
Bit name	PGOOD SM1	PGOOD SM2	PGOOD SM3	PGOOD LDO1	PGOOD LDO2	PGOOD LDO3	PGOOD LDO4	PGOOD LDO5
Function	MASK PGOOD FAULT BY SM1	MASK PGOOD FAULT BY SM2	MASK PGOOD FAULT BY SM3	MASK PGOOD FAULT BY LDO1	MASK PGOOD FAULT BY LDO2	MASK PGOOD FAULT BY LDO3	MASK PGOOD FAULT BY LDO4	MASK PGOOD FAULT BY LDO5
When 0	UNMASKED	UNMASKED	UNMASKED	UNMASKED	UNMASKED	UNMASKED	UNMASKED	UNMASKED
When 1	MASKED	MASKED	MASKED	MASKED	MASKED	MASKED	MASKED	MASKED

FUNCTIONALITY GUIDE — SYSTEM POWER AND CHARGE MANAGEMENT

CHARGE MANAGEMENT								
Fast Charge[1]		**Precharge Current**	**Termination**		**Charge Voltage**	**Precharge Voltage**	**SafetyTimer Timeout**	**Power Up Default**
Charge Current Value	**Charge Current Scaling**		**Current**	**Current Scaling**				
$I_{O(BAT)}$, Programmable, 1.5A max	25%, 50%, 75%, 100% of $I_{O(BAT)}$	10% of $I_{O(BAT)}$	I(TERM), 10% of $I_{O(BAT)}$	25%, 50%, 75%, 100% of $I_{(TERM)}$ value	4.2 V or 4.36 V	3.0 V	Programmable	Charger ON
Set via external resistor	Set via I2C	Fixed ratio	Fixed ratio	Set via I2C	Set via I2C	Fixed	Set via external resistor	

(1) The input current limit (see system power management below) regulates the input current , effectively limiting the charge current if the input current limit is lower than the fast charge current value programmed.

POWER PATH MANAGEMENT				
INPUT CURRENT LIMIT		**INPUT CONNECTED TO OUT PIN**		**POWER UP DEFAULT**
AC PIN	**USB PIN**	**INPUT POWER TO SYSTEM**	**BATTERY TO SYSTEM**	
2.5 A typ	100 mA max or 500 mA max or 2.5 A typ	#1 – AC #2 – USB #3 – Battery (when AC pin power and USB pin power are not detected)	Battery connected to system, independently of battery voltage	Input Power to System, USB mode selected, 100 mA max
Internal fixed current limit	Set via I2C	Automatic internal algorithm	Set via I2C, overrides internal algorithm	



With the above components the following system parameters are set :
Fast Charge Current = 1A (100% scaling, input limit=2.5A)
Safety Timer = 5hours, 30 min pre-charge
DPPM threshold = 4.3V
Temp hot: 65C
Temp Cold : 5C

Figure 30. Required External Components, Recommended Values, External Connections

POWER PATH AND CHARGE MANAGEMENT

Overview

The TPS65820 has an integrated charger with power path integrated MOSFETs. This topology, shown in the simplified block diagram below, enables using an external input power to run the system and charge the battery simultaneously. The power path has dual inputs that can be used to select either an external AC_DC adapter (AC pin) or an USB port power (USB pin) to power the end equipment main power rail (OUT pin, also referred to as the system power bus) and charge the battery pack (connected to BAT pin).

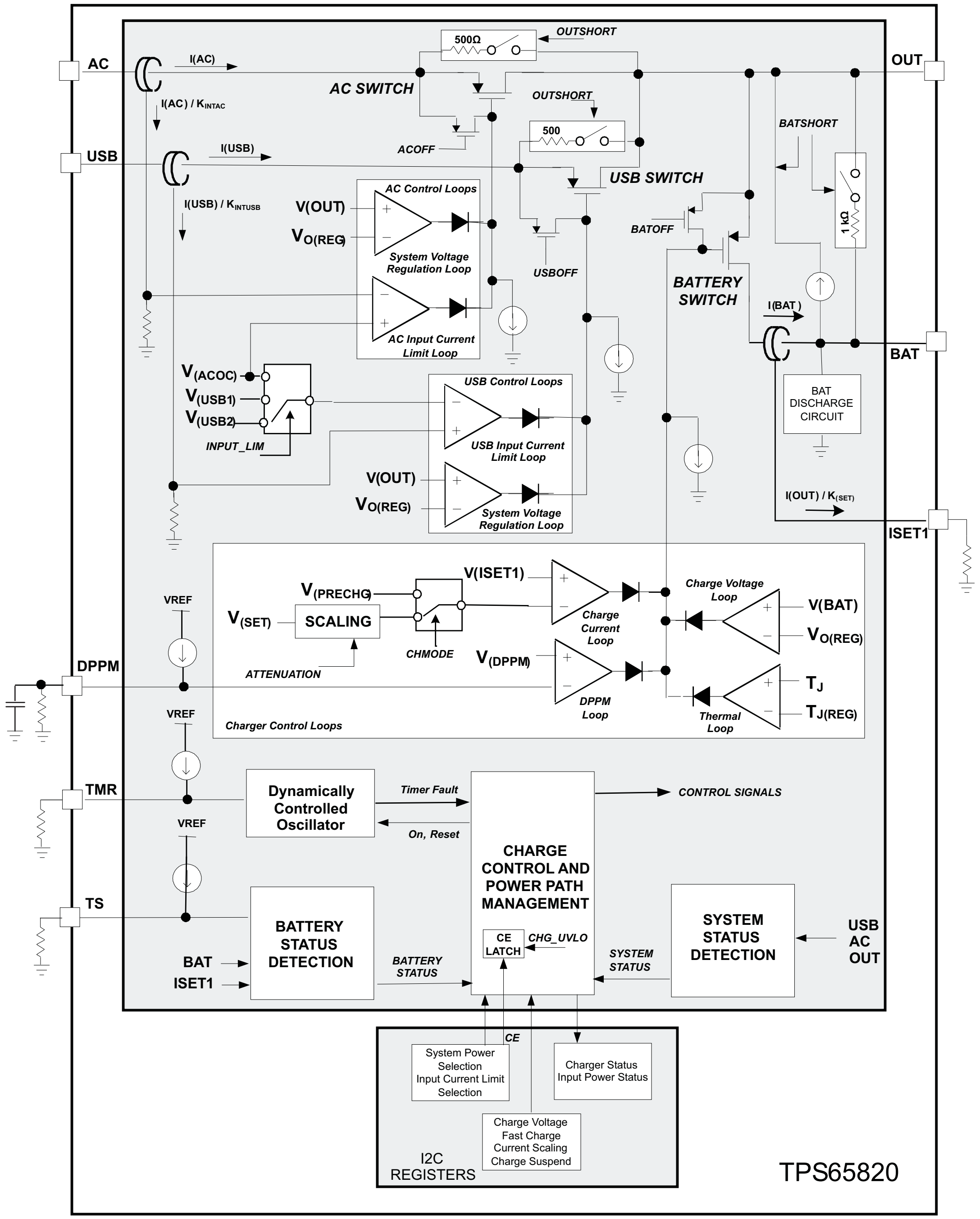


Figure 31. TPS65820 Charger and Power Path Section Simplified Block Diagram

The power path has three integrated power MOSFETs: the battery to system MOSFET (battery switch), the AC input to system MOSFET (AC switch) and the USB input to system MOSFET (USB switch). Each of those power MOSFETs can be operated either as an ON/OFF switch or as a linear pass element under distinct operating conditions, as defined by the control circuits that set the power MOSFET gate voltage.

The TPS65820 will regulate the voltage at the OUT pin to 4.6 V, when one of the external supplies connected to pins AC or USB is powering the OUT pin. The selected input (AC or USB pin) current is limited to a value defined by I2C register settings. The input current limit function assures compatibility with USB standard requirements, and also implements a protection function by limiting the maximum current supplied by an external AC_DC adapter or USB port power terminal.

The AC power MOSFET and USB power MOSFET operating modes are set by integrated control loops. Each of the power MOSFETs is controlled by two loops: one system voltage regulation loop and one input current limiting loop. The integrated loops modulate the AC or USB power MOSFETs drain to source resistance to regulate either the OUT pin voltage or to limit the input current. If no input power is present (AC and USB input power not detected) the AC and USB power MOSFETs are turned OFF, and the battery MOSFET is turned ON, connecting the BAT pin to the OUT pin .

The battery switch is turned ON when the AC or USB input power is detected and the charger function is enabled , charging the battery pack. During charge the battery MOSFET switch operation mode is defined by the charger control loops. The battery MOSFET switch drain to source resistance will be modulated by the charge current loop and charge voltage loop in order to implement the battery charging algorithm. In addition ot that multiple safety functions are activated (thermal shutdown, safety timers, short circuit recovery) , and additional functions (thermal loop and DPPM loop) optimize the charging process.

POWER PATH MANAGEMENT FUNCTION

Detecting the System Status

The power path and charge management block operate independently of the other TPS65820 circuits. Internal circuits check battery parameters (pack temperature, battery voltage, charge current) and system parameters (AC and USB voltage, battery voltage detection), setting the power path MOSFETs operating modes automatically. The TPS65820 has integrated comparators that monitor the battery voltage, AC pin voltage, USB pin voltage and the OUT pin voltage. The data generated by those comparators is used by the power path control logic to define which of the integrated power path switches will be active. A simplified block diagram for the system status detection is shown below.

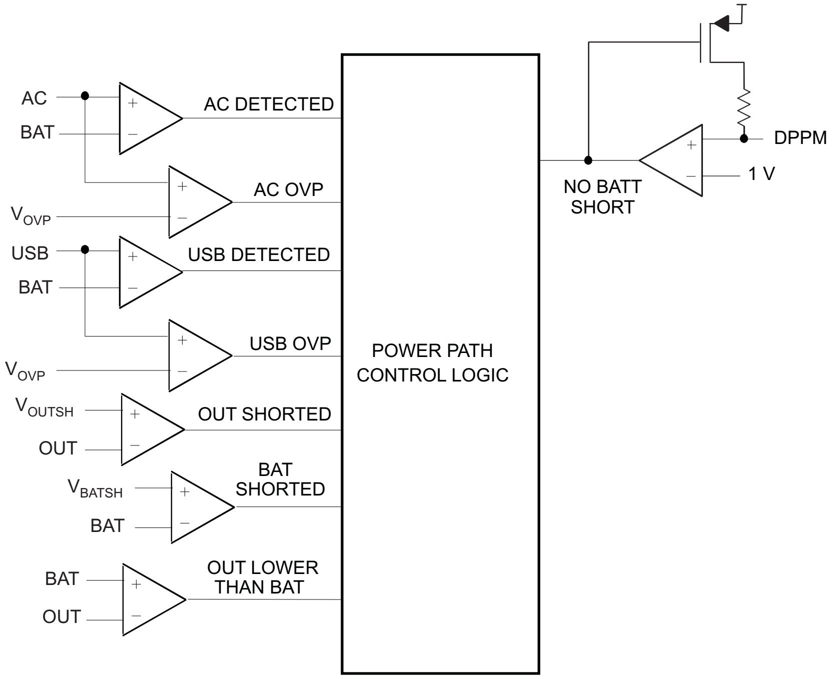


Figure 32. TPS65820 Systems Status Detection, Charger and Power Path Section

Table 4 lists the system power detection conditions. $V_{IN(DT)}$, V_{OUTSH}, V_{BATSH}, V_{OVP} are TPS65820 internal references, refer to the electrical characteristics for additional details.

Table 4. System Status Detection, Charger and Power Path Section

AC input voltage detected	V(AC) – V(BAT) > $V_{IN(DT)}$
USB input voltage detected	V(USB) – V(BAT) > $V_{IN(DT)}$
AC over-voltage detected	V(AC) > V_{OVP}
USB over-voltage detected	V(USB) > V_{OVP}
AC PIN TO OUT pin OR USB TO OUT PIN short detected	V(OUT) < $V_{INOUTSH}$
BAT pin to OUT pin short detected	V(BAT) - V(OUT) > $V_{BATOUTSH}$
Battery supplement mode need detected	V(BAT) – V(OUT) > V_{SUP}
Blank BAT to OUT short circuit detection	V(DPPM) < 1V

Power Path Logic: Priority Algorithm

The system power bus supply is automatically selected by the power path control logic, following an internal algorithm. The power path function detects an external input power connection when the input voltage exceeds the battery pack voltage. It also detects a supplement mode need (battery switch must be turned ON) when the system voltage (OUT pin) is below the battery voltage. A connected and non-selected external supply or the battery is automatically switched to the system bus, following the priority algorithm, when the external supply currently selected is disconnected from the system.

The input power priority is hard-wired internally, with the AC input having the higher priority, followed by the USB input (2nd) and the battery pack (3rd) . Using the I2C CHG_CONFIG register control bit CE the user can override the power path algorithm, connecting the battery to the system power bus. Care must be taken when using the battery to system connection option, as the system power bus **will not** be connected back to the AC or USB inputs (even if those are detected) when the battery is removed. Table 5 describes the priority algorithm.

Table 5. Power Path Control Logic Priority Algorithm

CE BIT (I2C CHG_CONFIG Register)	EXTERNAL SUPPLY DETECTED		SWITCH MODE			SYSTEM POWER SOURCE
	AC	**USB**	**AC**	**USB**	**Battery**	
HI	YES	NO	ON	OFF	ON if Supplement mode is required, OFF otherwise	AC
	NO	YES	OFF	ON		USB
	YES	YES	ON	OFF		AC
	NO	NO	OFF	OFF		BATTERY
LO	XX	XX	OFF	OFF	ON	BATTERY

The power path status is stored in register CHG_STAT.

Input Current Limit

The USB input current is limited to the maximum value programmed by the host, using the I2C interface. If the system current requirements exceed the input current limit the output voltage will collapse, the charge current will be reduced and finally the supplement mode will be set. The input current limit value is set with the I2C charge control register bits PSEL and ISET2, and it will be applied to the USB input ONLY. The AC input current limit is fixed to the internal short circuit limit value.

Table 6. Charge Current Scaling via I^{2}C

PSEL (I2C)	ISET2 (I2C)	INPUT CURRENT LIMIT	
		USB	**AC**
LO	LO	100 mA	2.75 A
LO	HI	500 mA	2.75 A
HI	LO	2.75 A	2.75 A
HI	HI	2.75 A	2.75 A

System Voltage Regulation

The system voltage is regulated to a fixed voltage when one of the input power supplies is connected to the system. The system voltage regulation is implemented by a control loop that modulates the selected switch Rds(on).

The typical system regulation voltage is 4.6 V.

Input Over-Voltage Detection

The AC and USB input voltages are monitored by voltage comparators that identify an over-voltage condition. If an over-voltage condition is detected a status register bit is set, indicating a potential fault condition.

When an over-voltage condition is detected the AC or USB switches state is not modified. If any of those switches was ON it will be kept in the ON state. During over-voltage conditions the system voltage will still be regulated, and no major safety issues are observed when not modifying the input switch state.

If the input over-voltage condition results in excessive power dissipation the thermal shutdown circuit will be activated, the AC and USB switches are turned OFF and the BAT switch is turned ON.

Output Short Circuit Detection

If the OUT pin voltage falls below an internal threshold $V_{INOUTSH}$ the AC and USB switches are turned off and internal pull-up resistors are connected from AC pin to OUT pin and USB pin to OUT pin. When the short circuit is removed those resistors enable the OUT pin voltage to rise above the $V_{INOUTSH}$ threshold, returning the system to normal operation.

Battery Short Circuit Detection

If the OUT pin voltage falls below the BAT pin voltage by more than an internal threshold $V_{BATOUTSH}$ the battery switch is turned off and internal pull-up resistor is connected between the OUT pin and the BAT pin. This resistor enables detection of the short removal, returning the system to normal operation.

Boot-Up Algorithm

During the initial TPS65820 power-up the contents of the ISET2, CE and SUSPEND bits on the control register are ignored for a time period t_{BOOT} . During that time the charger is enabled, and the selected input current limit is set internally to 100 mA max. At the end of t_{BOOT} period the control register settings are implemented.

No Battery Detection Circuit

The ANLG1 pin may be used to detect the connection of an external resistor that is embedded in a battery pack and is used as a pack ID function. The ANLG1 pin has an internal current source connected between OUT and ANLG1, which will be automatically enabled when the TPS65820 is not in SLEEP mode. The current levels for ANLG1 pin can be programmed via I2C register ADC_WAIT, bits BATID_n, as shown below:

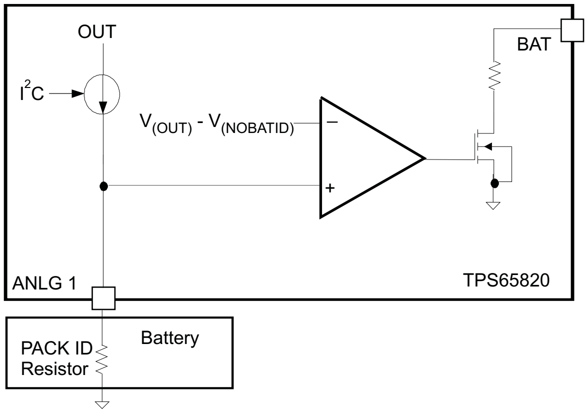


Figure 33. Battery Removal Detection, ANLG1 Pin

An internal comparator with a fixed deglitch time, $t_{DGL(NOBAT)}$ monitors the ANLG1 pin voltage, if V(ANLG1) > V(OUT) – $V_{NOBATID}$ a battery removed condition is detected and an internal discharge switch is activated, connecting an internal resistor from BAT pin to AGND1. Note that ANLG1 can also be used as an analog input for the ADC converter, in this case the voltage at pin ANLG1 must never exceed the V(OUT) - $V_{NOBATID}$ threshold to avoid undesired battery discharge.

Using the Input Power to Run the System and Charge the Battery Pack

The external supply connected to AC or USB pins must be capable of supplying the system power and the charger current. If the external supply power is not sufficient to run the system and charge the battery pack the TPS65820 executes a two-stage algorithm that prevents a low voltage condition at the system power bus:

1. The charge current is reduced, until the total (charger + system current) is at a level that can be supplied by the external input supply. This function is implemented by a dedicated charger control loop (see DPPM section in charger functional description for additional details).
2. The battery switch is turned ON if the charge current is reduced to zero and the input current is not enough to run the system. In this mode of operation both the battery and the external input power supply the system power (supplement operation mode).

The supplement operation mode is automatically set by the TPS65820 when the input power is switched to the OUT pin, and the OUT pin voltage falls below the battery voltage.

BATTERY CHARGE MANAGEMENT FUNCTION

Operating Modes

The TPS65820 supports charging of single-cell Li-Ion or Li-Pol battery packs. The charge process is executed in three phases: pre-charge (or pre-conditioning), constant current and constant voltage.

The charge parameters are selectable via I2C interface and using external components. The charge process will start when an external input power is connected to the system, the charger is enabled by the I2C register CHG_CONFIG bits CE=HI and CHGON=HI, and the battery voltage is below the recharge threshold, V(BAT) < $V_{(RCH)}$. When the charge cycle starts a safety timer is activated. The safety timer timeout value is set by an external resistor connected to TMR pin.

When the charger is enabled two control loops modulate the battery switch drain to source impedance to limit the BAT pin current to the programmed charge current value (charge current loop) or to regulate the BAT pin voltage to the programmed charge voltage value (charge voltage loop). If V(BAT) < 3 V (typ) the BAT pin current is internally set to 10% of the programmed charge current value. A typical charge profile is shown below, for an operation condition that does not cause the IC junction temperature to exceed 125°C (typ).

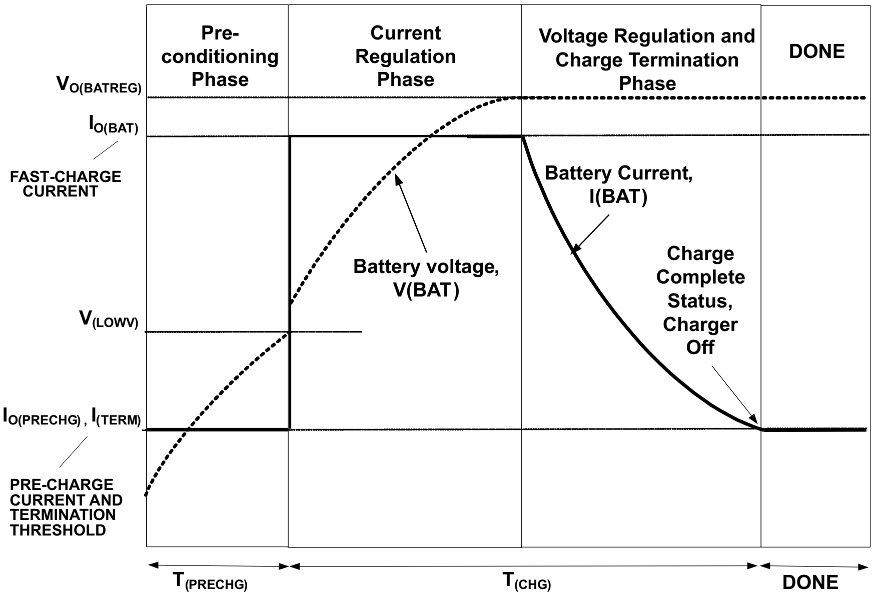
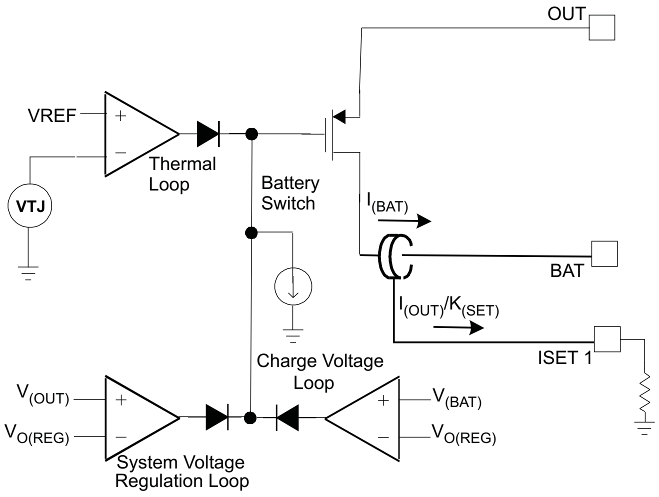


Figure 34. Typical Charge Cycle, Thermal Loop not Active

If the operating conditions cause the IC junction temperature to exceed 125°C the charge cycle is modified, with the activation of the integrated thermal control loop. The thermal control loop will be activated when an internal voltage reference, which is inversely proportional to the IC junction temperature, is lower than a fixed, temperature stable internal voltage. The thermal loop overrides the other charger control loops and reduces the charge current until the IC junction temperature returns to 125°C, effectively regulating the IC junction temperature.



A modified charge cycle, with the thermal loop active, is shown here:

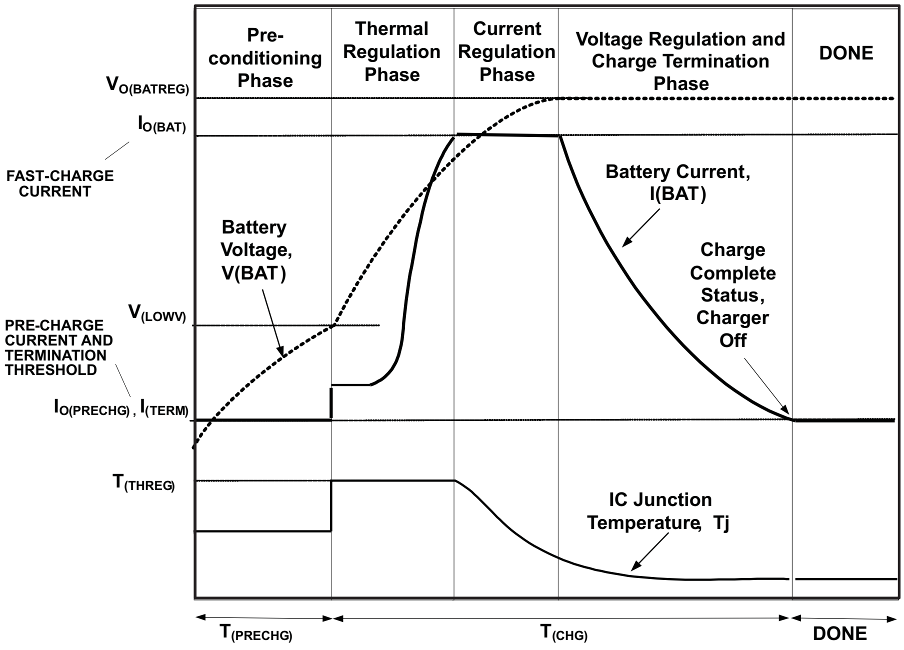


Figure 35. Typical Charge Cycle, Thermal Loop Active

Battery Pre-Conditioning

The TPS65820 applies a pre-charge current $I_{o(PRECHG)}$ to the battery if the battery voltage is below the $V_{(LOWV)}$ threshold, pre-conditioning deeply discharged cells. The charge current loop regulates the ISET1 pin voltage to an internal reference value, V_{PRECHG}. The resistor connected between the ISET1 and AGND pins, R_{SET}, determines the precharge rate.

The pre-charge rate programmed by R_{SET} is always applied to a deeply discharged battery pack, independently of the input power selection (AC or USB). The pre-charge current can be calculated as follows:

$$I_{O(PRECHG)} = \frac{V_{PRECHG} \times K_{SET}}{R_{SET}} \qquad (2)$$

where:

K_{SET} is the charge current scaling factor and V_{PRECHG} is the pre-charge set voltage.

CONSTANT CURRENT CHARGING

The constant charge current mode (fast charge) is set when the battery voltage is higher than the pre-charge voltage threshold. The charge current loop regulates the ISET1 pin voltage to an internal reference value, V_{SET} . The fast charge current regulation point is defined by the external resistor connected to the ISET1 pin , R_{SET} , as shown in the following:

$$I_{O(BAT)} = \frac{V_{SET} \times K_{SET}}{R_{SET}} \qquad (3)$$

where:

V_{SET} (2.5 V typ) is the voltage at ISET1 pin during charge current regulation and K_{SET} = Charge Current Scaling Factor.

The reference voltage V_{SET} can be reduced via I2C register CHG_CONFIG bits ISET1_1 and ISET1_0. V_{SET} can be selected as a percentage (75%, 50% or 25%) of the original 2.5 V typ, non-attenuated V_{SET} value, effectively scaling down the charge current.

The ISET1 resistor will always set the maximum charge current, if the AC input is selected. When the USB input is selected the maximum charge current will be defined by the USB input current limit and the programmed charge current. If the USB input current limit is lower than the $I_{O(OUT)}$ value the battery switch will be set in the dropout region and the charge current will be defined by the input current limit value and system load, as shown in the following curves:

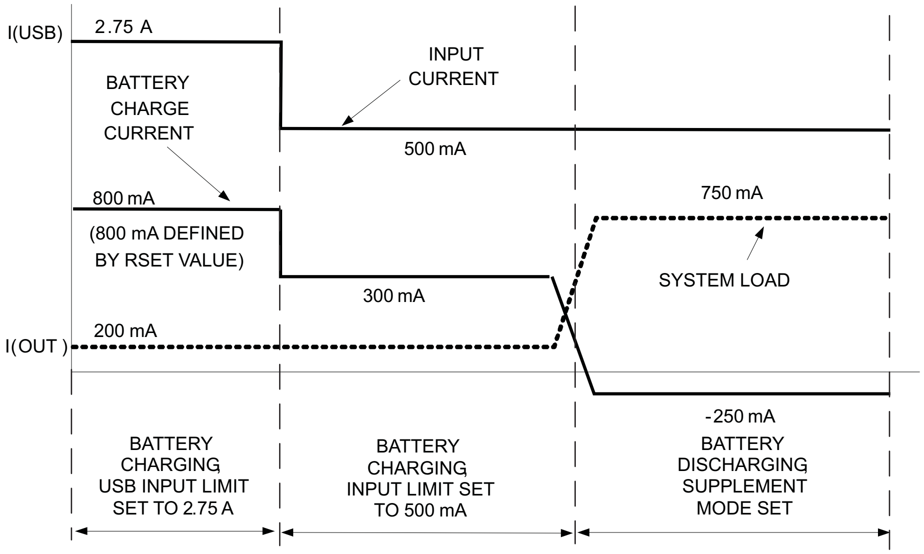


Figure 36. Input Current Limit Impact on Effective Charge Current

CHARGE TERMINATION AND RECHARGE

The TPS65820 monitors the charging current during the voltage regulation phase. Charge is terminated when the charge current is lower than an internal threshold, set to 10% (typ) of the fast charge current rate. The termination point applies to both AC and USB charging, and it can be calculated as follows:

$$I_{TERM} = \frac{V_{TERM} \times K_{SET}}{R_{SET}} \tag{4}$$

where

V_{TERM} is the termination detection voltage reference.

The voltage at ISET1 pin is monitored to detect termination, and termination is detected when V(SET1) < V_{TERM} (0.25 V typ). The voltage reference V_{TERM} is internally set to 10% of the V_{SET} reference voltage, and it will be modified if the reference voltage V_{SET} is scaled via I2C register CHG_CONFIG bits ISET1_1 and ISET1_0. V_{TERM} is reduced by the same percentage used to scale down V_{SET} .

The table below shows charge current and termination thresholds for a 1-A charge current set (1-kΩ resistor connected to ISET1 pin), with the selected input current limit set to a value higher than the programmed charge current. The termination current is scaled for all charge current modes (AC or USB), as it is always set by the ISET1 pin external resistor value.

Table 7. Charge Current and Termination Threshold Selection Example

Charge Control Register Bits		Charge Current, (% of typical value programmed by ISET1 resistor)	Vset (V)	Vterm (mV)	Charge Current (A)	Termination Current (mA)
ISET1_1	ISET1_0					
0	0	25%	0.6	60	0.24	20
0	1	50%	1.25	115	0.5	40
1	0	75%	1.9	160	0.78	60
1	1	100%	2.5	250	1	100

Once termination is detected, a new charge cycle starts if the voltage on the BAT pin falls below the $V_{(RCH)}$ threshold. A new charge start is also triggered if the charger is enabled/disabled/enabled via I2C (CHG_CONFIG register bits CE or CHGON), or if both AC and USB input power are removed and then at least one of them is re-inserted.

The termination is disabled when the thermal loop OR DPPM loop are active, and during supplement mode. The charge termination will also be disabled when the I2C control bit TERM_OFF is set to HI, in the CHG_CONFIG register. A new charge cycle will be started , if the control bit TERM_OFF is set to HI after termination was detected.

BATTERY VOLTAGE REGULATION, CHARGE VOLTAGE

The voltage regulation feedback is Implemented by sensing the BAT pin voltage, which is connected to the positive side of the battery pack. The TPS65820 monitors the battery-pack voltage between the BAT and AGND1 pins, when the battery voltage rises to the $V_{O(REG)}$ threshold the voltage regulation phase begins and the charging current tapers down.

The charging voltage can be selected as 4.2 V or 4.365 V (typ). The default power-up voltage is 4.2 V. As a safety measure the 4.365 V charge voltage is programmed only if two distinct bits are set via I2C: VCHG=HI in the CHG_CONFIG , and CHG_VLTG=LO in the GPIO3 register.

TEMPERATURE QUALIFICATION

The TPS65820 continuously monitors battery temperature by measuring the voltage between the TS and AGND1 pins. An internal current source provides the bias for a negative-temperature coefficient thermistor (NTC), and the TS pin voltage is compared to the window set by internal thresholds V_{LTF} and V_{HTF} to determine if charging is allowed. A voltage outside the V_{LTF} to V_{HTF} window is considered a temperature fault, and charge is suspended. Charge resumes when the temperature returns to the valid window range.

With a 50 kΩ (at 25°C) thermistor the valid temperature window will be set between 0°C to 45°C. The temperature window can be enlarged by adding external resistors to the TS pin application circuit.

DYNAMIC POWER PATH MANAGEMENT

Under normal operating conditions the OUT pin voltage will be regulated, when the AC or USB pin are powering the OUT pin and the battery pack is being charged. If the total (system + charge current) exceeds the available input current the system voltage will drop below the regulation value.

The dynamic power path management function monitors the system output voltage. A condition where the external input supply rating has been exceeded or the input current limit has been reached is detected when the OUT pin voltage drops below an user-defined threshold, V_{DPPM}:

$$V_{DPPM} = R_{DPPM} \times K_{DPPM} \times I_{DPPM} \tag{5}$$

where:

R_{DPPM} = external resistor connected to DPPM pin
K_{DPPM} = DPPM scaling factor
I_{DPPM} = DPPM pin internal current source

To correct this situation the DPPM loop reduces the charge current , regulating the OUT pin voltage to the user-defined V_{DPPM} threshold . The DPPM loop effectively identifies the maximum current that can be delivered by the selected input and dynamically adjusts the charge current to guarantee that the end equipment is always powered. In order to minimize OUT voltage ripple during DPPM operation the V_{DPPM} threshold should be set just below the system regulation voltage.

If the charge current is reduced to zero by the DPPM and the input current is still lower than the OUT pin load the output voltage will fall below the DPPM threshold, decreasing until the battery supplement mode is set [V(OUT) = V(BAT) – $V_{SUP(DT)}$].

CHARGER OFF MODE

The TPS65820 charger circuitry enters the low-power OFF mode if both AC and USB power are not detected . This feature prevents draining the battery during the absence of input supply.

PRE-CHARGE SAFETY TIMER

The TPS65820 activates an internal safety timer during the battery pre-conditioning phase. The pre-charge safety timer time-out value is set by the external resistor connected to TMR pin, RTMR, and the timeout constants K_{PRE} and K_{TMR} :

$T_{PRECHG} = K_{PRE} \times R_{TMR} \times K_{TMR}$

The K_{PRE} constant typical value is 0.1, setting the pre-charge timer value to 10% of the charge safety timer value.

When the charger is in suspend mode, set via I^2C register CHG_CONFIG bit CHGON or set by a pack temperature fault, the pre-charge safety timer is put on hold (i.e., charge safety timer is not reset). Normal operation resumes when the charger exits the suspend mode . If V(BAT) does not reach the internal voltage threshold V_{PRECHG} within the pre-charge timer period a fault condition is detected and the charger is turned off.

If the TMR pin is left floating and internal resistor , 50KΩ typ, is used to generate the timebase used to set the pre-charge timeout value. The typical pre-charge timeout value can be then calculated as :

$T_{PRECHG} = K_{PRE} \times 50K \times K_{TMR}$

CHARGE SAFETY TIMER

As a safety mechanism the TPS65820 has a user-programmable timer that measures the total fast charge time. This timer (charge safety timer) is started at the end of the pre-conditioning period. The safety charge timeout value is set by the value of an external resistor connected to the TMR pin (R_{TMR}). The charge safety timer time-out value is calculated as follows:

$T_{CHG} = K_{TMR} \times R_{TMR}$

When the charger is in suspend mode, set via I^2C register CHG_CONFIG bit CHGON or set by a pack temperature fault, the charge safety timer is put on hold (i.e., charge safety timer is not reset). Normal operation resumes when the charger exits the suspend mode. If charge termination is not reached within the timer period a fault condition is detected, and the charger is turned off.

The charge safety timer is held in reset if the TMR pin is left floating or if the control bit TERM_OFF,in the CHG_EN I2C register, is set to HI . Under this mode of operation an internal resistor , 50 KΩ typ, sets the internal charger and power path deglitch and delay times, as well as the pre-charge safety timer timeout value.

TIMER FAULT RECOVERY

The TPS65820 provides a recovery method to deal with timer fault conditions. The following summarizes this method:

- Condition 1: Charge voltage above recharge threshold , V_{RCH} , and timeout fault occurs.

Recovery method: The IC waits for the battery voltage to fall below the recharge threshold. This could happen as a result of a load on the battery, self-discharge or battery removal. Once the battery falls below the recharge threshold, the IC clears the fault and starts a new charge cycle.

- Condition 2: Charge voltage below recharge threshold ,$V_{(RCH)}$, and timeout fault occurs.

Recovery method: Under this scenario, the IC connects an internal pull-up resistor from OUT pin to Bat pin. This pull-up resistor is used to detect a battery removal condition and remains on as long as the battery voltage stays below the recharge threshold. If the battery voltage goes above the recharge threshold, the IC disables the pull-up resistor connection and executes the recovery method described for condition 1.

All timers will be reset and all timer fault conditions are cleared when a new charge cycle is started either via I2C (toggling CHG_CONFIG bits CE, CHGON) or by cycling the input power . All timers are reset and all timer fault conditions are cleared when the TPS65820 enters the UVLO mode.

DYNAMIC TIMER FUNCTION

The charge and pre-charge safety timers are programmed by the user to detect a fault condition if the charge cycle duration exceeds the total time expected under normal conditions. The expected total charge time is usually calculated based on the fast charge current rate.

When the thermal loop or the DPPM loops are activated the charge current is reduced, and a false safety timer fault can be observed if this mode of operation is active for a long periods. To avoid this undesirable fault condition the TPS65820 activates the dynamic timer function when the DPPM and thermal loops are active. The dynamic timer function slows down the safety timers clock, effectively adding an extra time to the programmed timeout value as follows:

1. If the battery voltage is below the battery depleted threshold: the pre-charge timer value is modified while the thermal loop or the DPPM loop are active
2. If the battery voltage is above the pre-charge threshold: the safety timer value is modified if the DPPM or the thermal loop are active AND the battery voltage is below the recharge threshold.

The TPS65820 dynamic timer function circuit monitors the voltage at pin ISET1 during pre-charge and fast charge. When the charger is regulating the charge current the voltage at pin ISET1 will be regulated by the control loops to either V_{SET} or V_{PRECHG}. If the thermal loop or DPPM loops are active the voltage at pin ISET1 will be lower than V_{SET} or V_{PRECHG} , and the dynamic timer control circuit changes the safety timers clock period based on the V_{SET}/V(ISET1) ratio (fast charge) or V_{PRECHG}/V(ISET1) ratio (pre-charge).

The maximum *clock period* is internally limited to twice the value of the programmed clock period , which is defined by the resistor connected to TMR pin , as shown in the following figure:

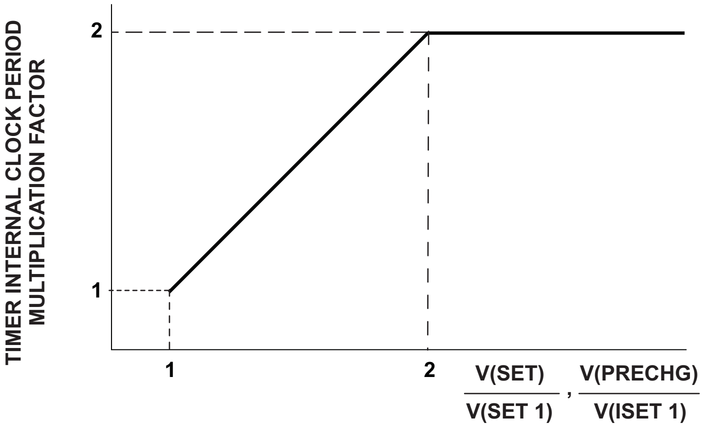


Figure 37. Safety Timer Internal Clock Slowdown

The effective charge safety timer value can then be expressed as follows:

Effective pre-charge timeout = $t_{(PRECHG)} + t_{(PCHGADD)}$

Effective charge safety timeout = $t_{(CHG)} + t_{(CHGADD)}$

Where the *added* timeout values, $t_{(PCHGADD)}$, $t_{(CHGADD),}$ will be equal to the sum of all time periods when either the thermal loop or DPPM loop were active. The *maximum added* timeout value will be internally limited to 2 x $t_{(CHG)}$ or 2 x $t_{(PRECHG)}$

CHARGE AND SYSTEM POWER MANAGEMENT — I2C REGISTERS

The I2C registers that control charger and power path related functions are shown below. The HEX address for each register is shown by the register name, together with the R or W functionality for the register bits. Shaded values indicate default initial power-up values. Note that the CHG_STAT register contents are valid only when either AC or USB power are applied to the TPS65820. The output of linear regulator LDO_PM can be used as an indicator of external input power detection; if LDO_PM is in regulation the CHG_STAT register contents are valid.

CHG_CONFIG, ADDRESS=9, ALL BITS R/W								
	B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Bit name	VCHG	CHGON	TERM_OFF	ISET1_1	ISET1_0	ISET2	PSEL	CE(1)
Function	CHARGE VOLTAGE SELECTION	CHARGE ENABLE	TERMINATION ENABLE CONTROL	CHARGE CURRENT SCALING FACTOR		USB CURRENT LIMIT	SELECTED INPUT CURRENT LIMIT	SYSTEM POWER SELECTION
When 0	4.36 V	CHARGE SUSPENDED	TERMINATION ENABLED	00= 0.25 10=0.75 01= 0.5 **11= 1** Note: Relative to Charge Current Programmed by external ISET pin resistor.		100 mA	USE USB CURRENT LIMIT	BATTERY TO SYSTEM
When 1	4.20 V	CHARGE ON	TERMINATION DISABLED			500 mA	INPUT CURRENT LIMIT SET TO MAXIMUM	INPUT POWER TO SYSTEM(1)

(1) The CE bit state is latched inside the charger control logic (CE latch) during an OUT pin UVLO event , prior to resetting the charge control register bit CE to its power up default value. The charger CE latch will control the charger and power path state as long as the TPS65820 is in UVLO mode and an external supply is connected to the charger block. The CE latch will be reset to its power-up value (CE=LO) only when the input power is removed from the charger block. The CE latch is disabled and the CE charge control register bit sets the charger and power path MOSFETs state when the TPS65820 exits the UVLO mode. This feature avoids a host software *loop* when the host algorithm requires a depleted (or absent) battery to be connected to the system bus while input power is present.

GPIO3, ADDRESS= 1C, ALL BITS R/W. NOTE: ONLY BIT B4 CONTROLS CHARGER-RELATED FUNCTIONALITY								
	B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Bit name	GPIO3i/O	GPIO3_LEVEL	LDO0_ENABLE	CHARGE _VLTG	NOT USED	GPIO2 _INTSRC	GPIO1 _INTSRC	GPIO2 _SM2
Function	*SEE GPIO SECTION*	*SEE GPIO SECTION*	*SEE GPIO SECTION*	CHARGE VOLTAGE SELECTION SAFETY BIT	NOT USED	*SEE GPIO SECTION*	*SEE GPIO SECTION*	*SEE GPIO SECTION*
When 0				4.2 V				
When 1				4.36 V				

CHG_STAT, ADDRESS=A, ALL BITS READ ONLY– POWER UP DEFAULTS SHOW SYSTEM STATUS WHEN EXITING POWER DOWN								
	B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Bit name	BAT_STAT(1)(2)	INPUT _PWR	THDPPM_ON	ACPG	USBPG	STAT1	STAT2	INP_OV
Function	BATTERY SUPPLEMENT MODE STATUS	SELECTED INPUT POWER STATUS	THERMAL LOOP AND DPPM STATUS	AC INPUT POWER STATUS	USB INPUT POWER STATUS	CHARGE STATUS		AC OR USB INPUT OVP DETECTION
When 0	SUPPLEMENT MODE OFF	AC INPUT SELECTED	BOTH OFF	AC NOT DETECTED	USB NOT DETECTED	00 = PRE-CHARGE ON 01=CHARGE DONE 10=FAST CHARGE ON 11= CHARGE SUSPEND, TIMER FAULT, CHARGER OFF		NO OVP
When 1	SUPPLEMENT MODE ON	USB INPUT SELECTED	DPPM ON OR THERMAL ON	AC DETECTED	USB DETECTED			OVP DETECTED

(1) The battery supplement is entered when $V_{(BAT)} – V_{(OUT)} > 60$ mV (typ), and it ends when $V_{(BAT)} – V_{(OUT)} < 20$ mV. When the system power bus current exceeds the input current limit or the external supply current capability the supplement mode will be set. An oscillatory behavior for BAT_STAT bit can happen if the battery switch dropout voltage is less than 20 mV (typ) when in supplement mode.

(2) The BAT_STAT is always masked internally, and does not generate interrupts

FUNCTIONALITY GUIDE — LINEAR REGULATORS

SELECTABLE OUTPUT VOLTAGE LDO

Supply	ON/OFF Control	Output Discharge Switch	OUTPUT VOLTAGE (V), set via I2C		IO Max (mA)	Acc %	Power Up Default
			# of Steps	Available Values (V)			
LDO1	Yes, set via I2C	Yes, enabled via I2C	8	1.25/1.5/1.8/2.5/2.85/3/3.2/3.3	150	3	ON, 2.85 V
LDO2	Yes, set via I2C	Yes, enabled via I2C	8	1.25/1.5/1.8/2.5/2.85/3/3.2/3.3	150	3	ON, 3.3 V
SIM	Yes, set via I2C	no	2	1.8 / 3.0	8	2	OFF, 1.8 V
RTC_OUT	Yes, set via I2C	no	2	2.6/3.1	8	5	ON, 2.6V

PROGRAMMABLE OUTPUT VOLTAGE LDO

Supply	ON/OFF Control	Output Discharge Switch	OUTPUT VOLTAGE (V), set via I2C			IO Max (mA)	Acc %	Power Up Default
			Range	# of Steps	Min Step			
LDO3	yes, set via I2C	Yes, enabled via I2C	1.224–4.46	128	25 mV	100	3	ON, 1.25 V
LDO4	yes, set via I2C	Yes, enabled via I2C	1.224–4.46	128	25 mV	100	3	ON, 2.75 V
LDO5	yes, set via I2C	Yes, enabled via I2C	1.224–4.46	128	25 mV	100	3	ON, 2.81 V

FIXED OUTPUT VOLTAGE LDO’S

Supply	ON/OFF Control	OUTPUT VOLTAGE (V)	IO Max (mA)	Acc %	Power Up Default
LDC0	Yes, via I2C	3.3, fixed	150	3	OFF
LDO_PM	NO, enabled internally	3.3, fixed	20	5	ON if AC or USB power detected

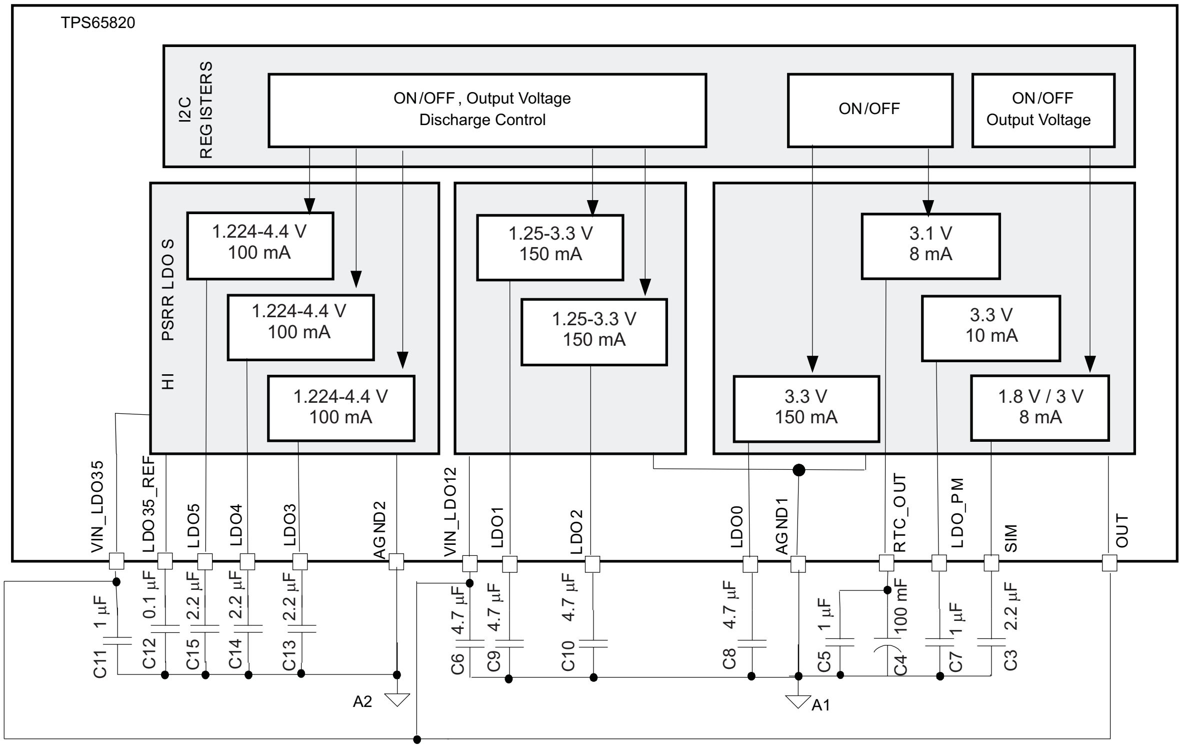


Figure 38. Required External Components, Recommended Values, External Connections

LINEAR REGULATORS — FUNCTIONAL DESCRIPTION

The TPS65820 offers nine Integrated Linear Regulators, designed to be stable over the operating load range with use of external ceramic capacitors, as long as the recommended filter capacitor values (see application diagram and pinout description) are used. The output voltage can be programmed via I^{2}C (LDO0-2, LDO3-5) or have a fixed output voltage.

Simplified Block Diagram

A simplified block diagram for the LDOs is shown in Figure 39.

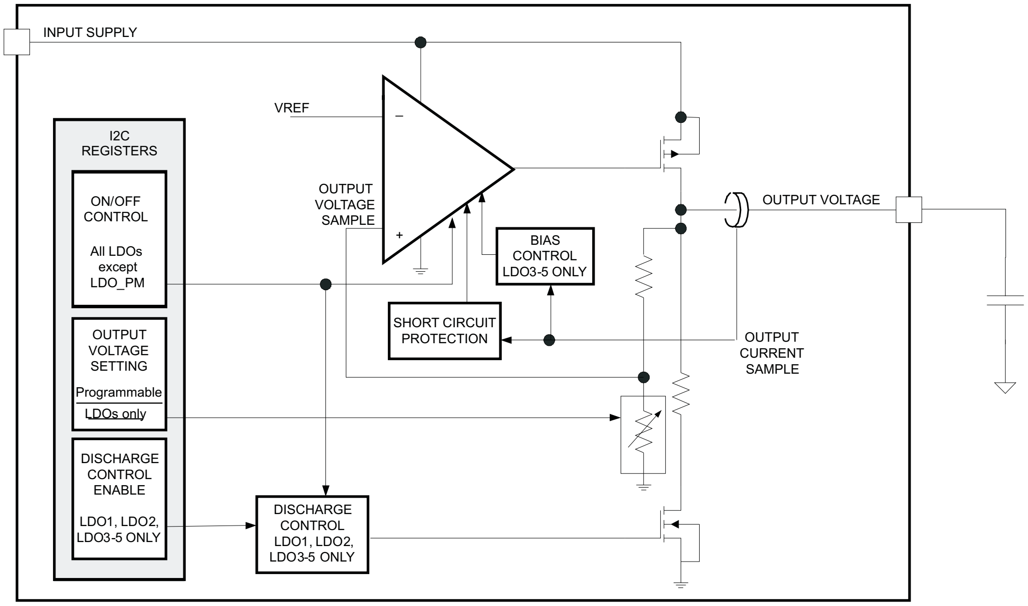


Figure 39. Simplified Block Diagram

Connecting the LDO Input Supply

Both LDO1-2 and LDO3-5 have uncommitted input power supply pins (VIN_LDO12, VIN_LDO35) , which should be externally connected to the OUT pin. Optionally the LDO0-2 and LDO3-5 input supplies can be connected to the output of the available buck converters SM1 or SM2, as long as the resulting overall power-up sequence meets the system requirements.

The RTC_OUT, SIM, LDO0 and LDO_PM linear regulators are internally connected to the OUT pin.

ON/OFF Control

All the LDO’s, with exception of LDO_PM LDO, have a ON/OFF control which can be set via I2C commands, facilitating host management of the distinct system power rails . The LDO_PM LDO On/OFF control is internally hard-wired, and it will be set to ON when either the AC or USB input power is detected.

Output Discharge Switch

LDO1, LDO2 AND LDO3-5 have integrated switches that discharge each output to ground when the LDO is set to OFF by an I2C command. The output discharge switch function can be disabled by using I2C register control bits. The discharge switches are enabled after the initial power-up

Special Functions

The RTC_OUT, SIM (Subscriber line interface module) and LDO_PM linear regulators are designed to support lower load currents. The SIM and RTC_LDO have low leakage in OFF mode, with the input pin voltage above or below the output pin voltage. The LDO_PM can be used for USB enumeration, or a status indication of input power connection.

Output Voltage Monitoring

Internal power good comparators monitor the LDO outputs and detect when the output voltage is below 90% of the programmed value. This information is used by the TPS65820 to generate interrupts or to trigger distinct operating modes, depending on specific I2C register settings. See interrupt and sequencing controller section for additional details.

LINEAR REGULATORS — I^{2}C REGISTERS

The I2C registers that control LDO-related functions are shown below. The HEX address for each register is shown by the register name, together with the R or W functionality for the register bits. Shaded values indicate default initial power-up values.

	B7	B6	B5	B4	B3	B2	B1	B0
EN_LDO: ADRESS=B, ALL BITS R/W								
Bit name	LDO1_EN	LDO2_EN	LDO3_EN	LDO4_EN	LDO5_EN	SIM_SET	SIM EN1	RTC_EN
Function	LDO1…5 ON/OFF CONTROL					SIM LDO output voltage	SIM/RTC ON/OFF CONTROL	
When 0	OFF	OFF	OFF	OFF	OFF	3.0 V	OFF	OFF
When 1	ON	ON	ON	ON	ON	1.80 V	ON	ON
LDO12: ADRESS=C, ALL BITS R/W								
Bit name	LDO1_DISCH	LDO1_2 SET	LDO1_1 SET	LDO1_0 SET	LDO2_DISCH	LDO2_2 SET	LDO2_1 SET	LDO2_0 SET
Function	LDO1 output discharge switch enable	LDO1 OUTPUT VOLTAGE SETTING			LDO2 Output discharge switch enable	LDO2 OUTPUT VOLTAGE SETTING		
When 0	OFF	000=1.25 V 001=1.5 V **Default=2.85V** 010=1.8 V 011=2.5 V **100=2.85 V** 110=3 V 110=3.2 V 111=3.3			OFF	000=1.25 V 001=1.5 V **Default=3.3V** 010=1.8 V 011=2.5 V 100=2.85 V 110=3.0 V 110=3.2 V **111=3.3 V**		
When 1	ON				ON			
LDO3, ADDRESS=16, ALL BITS R/W								
Bit name	LDO3_DISCH	LDO3_6 SET	LDO3_5 SET	LDO3_4 SET	LDO3_3 SET	LDO3_2 SET	LDO3_1 SET	LDO3_0 SET
Function	LDO3 Output discharge switch enable	LDO3 OUTPUT VOLTAGE SETTING						
When 0	OFF	SeeTable 8 for LDO3-5 output voltage setting, **Power up default=1.25 V**						
When 1	ON							
LDO4, ADRESS=E, ALL BITS R/W								
Bit name	LDO4_DISCH	LDO4_6 SET	LDO4_5 SET	LDO4_4 SET	LDO4_3 SET	LDO4_2 SET	LDO4_1 SET	LDO4_0 SET
Function	LDO4 Output discharge switch enable	LDO4 OUTPUT VOLTAGE SETTING						
When 0	OFF	See Table 8 for LDO3-5 output voltage setting, **Power up default=2.75 V**						
When 1	ON							
LDO5, ADRESS=F, ALL BITS R/W								
Bit name	LDO5_DISCH	LDO5_6 SET	LDO5_5 SET	LDO5_4 SET	LDO5_3 SET	LDO5_2 SET	LDO5_1 SET	LDO5_0 SET
Function	LDO5 Output discharge switch enable	LDO5 OUTPUT VOLTAGE SETTING						
When 0	OFF	See Table 8 for LDO3-5 output voltage setting, **Power up default=2.81 V**						
When 1	ON							
GPIO3, ADDRESS= B7, ALL BITS R/W. NOTE: ONLY BIT B5 CONTROLS LDO-RELATED FUNCTIONALITY								
Bit name	GPIO3i/O	GPIO3 LEVEL	LDO0 ENABLE	CHARGE _VLTG	RTC_SET	GPIO2 _INTSRC	GPIO1 _INTSRC	GPIO2 _SM2
Function	*SEE GPIO SECTION*	*SEE GPIO SECTION*	LDO0 ON/OFF CONTROL	*SEE CHARGER SECTION*	RTC_LDO OUTPUT VOLTAGE	*SEE GPIO SECTION*	*SEE GPIO SECTION*	*SEE GPIO SECTION*
When 0			LDO0 OFF		2.6V			
When 1			LDO0 ON		3.1V			

Table 8. LDO35 SET

Dec	B6-B0	Vset	Dec	B6-B0	Vset	Dec	B6-B0	Vset	Dec	B6-B0	Vset
0	0000000	1.224	32	0100000	2.040	31	0011111	2.015	64	0000040	2.856
1	0000001	1.250	33	0000021	2.066	32	0100000	2.040	65	0000041	2.882
2	0000010	1.275	34	0000022	2.091	66	1000010	2.907	98	1100010	3.723
3	0000011	1.301	35	0000023	2.117	67	1000011	2.933	99	1100011	3.749
4	0000100	1.326	36	0000024	2.142	68	1000100	2.958	100	1100100	3.774
5	0000101	1.352	37	0000025	2.168	69	1000101	2.984	101	1100101	3.800
6	0000110	1.377	38	0000026	2.193	70	1000110	3.009	102	1100110	3.825
7	0000111	1.403	39	0000027	2.219	71	1000111	3.035	103	1100111	3.851
8	0001000	1.428	40	0000028	2.244	72	1001000	3.060	104	1101000	3.876
9	0001001	1.454	41	0000029	2.270	73	1001001	3.086	105	1101001	3.902
10	0001010	1.479	42	000002A	2.295	74	1001010	3.111	106	1101010	3.927
11	0001011	1.505	43	000002B	2.321	75	1001011	3.137	107	1101011	3.953
12	0001100	1.530	44	000002C	2.346	76	1001100	3.162	108	1101100	3.978
13	0001101	1.556	45	000002D	2.372	77	1001101	3.188	109	1101101	4.004
14	0001110	1.581	46	000002E	2.397	78	1001110	3.213	110	1101110	4.029
15	0001111	1.607	47	000002F	2.423	79	1001111	3.239	111	1101111	4.055
16	0010000	1.632	48	0000030	2.448	80	1010000	3.264	112	1110000	4.080
17	0010001	1.658	49	0000031	2.474	81	1010001	3.290	113	1110001	4.106
18	0010010	1.683	50	0000032	2.499	82	1010010	3.315	114	1110010	4.131
19	0010011	1.709	51	0000033	2.525	83	1010011	3.341	115	1110011	4.157
20	0010100	1.734	52	0000034	2.550	84	1010100	3.366	116	1110100	4.182
21	0010101	1.760	53	0000035	2.576	85	1010101	3.392	117	1110101	4.208
22	0010110	1.785	54	0000036	2.601	86	1010110	3.417	118	1110110	4.233
23	0010111	1.811	55	0000037	2.627	87	1010111	3.443	119	1110111	4.259
24	0011000	1.836	56	0000038	2.652	88	1011000	3.468	120	1111000	4.284
25	0011001	1.862	57	0000039	2.678	89	1011001	3.494	121	1111001	4.310
26	0011010	1.887	58	000003A	2.703	90	1011010	3.519	122	1111010	4.335
27	0011011	1.913	59	000003B	2.729	91	1011011	3.545	123	1111011	4.361
28	0011100	1.938	60	000003C	2.754	92	1011100	3.570	124	1111100	4.386
29	0011101	1.964	61	000003D	2.780	93	1011101	3.596	125	1111101	4.412
30	0011110	1.989	62	000003E	2.805	94	1011110	3.621	126	1111110	4.437
31	0011111	2.015	63	000003F	2.831	95	1011111	3.647	127	1111111	4.463

FUNCTIONALITY GUIDE — SWITCHED MODE STEP-DOWN CONVERTERS

BUCK CONVERTERS, I2C PROGRAMMABLE OUTPUT VOLTAGE												
Supply	**PFM Mode**	**Standby Mode**	**OUTPUT VOLTAGE (V), Set via I²C, Separate Settings for Normal or Standby Mode**				**IO Max (mA)**	**PWM Freq and Phase**	**SLEW RATE, mV/µS, Set via I²C**			**Power Up Default**
			Range	**# of Steps**	**Min Step**	**Acc (%)**			**Range**	**# of Steps**	**Min Step**	
SM1	PFM/PWM with automatic mode selection or PWM only.	Standby mode with distinct voltage available. Standby mode set via I2C or with GPIO pin	0.6-1.8	32	40 mV	3	600	1.5MHz, 0°	0, 0.24 to 15.36	8	0.24	ON, skip mode off, PWM only, 1.24 V(on/stby), 15.36mV/µS
SM2	Mode of operation set via I2C		1.0-3.4	32	80mV	3	600	1.5MHz, 0/90/180 270°, with respect to SM1, set via I2C	0, 0.48-30.72	8	0.48	ON, skip mode on, PWM/PFM, 1.8 V (on/stby), 180°, 30.72mV/µS

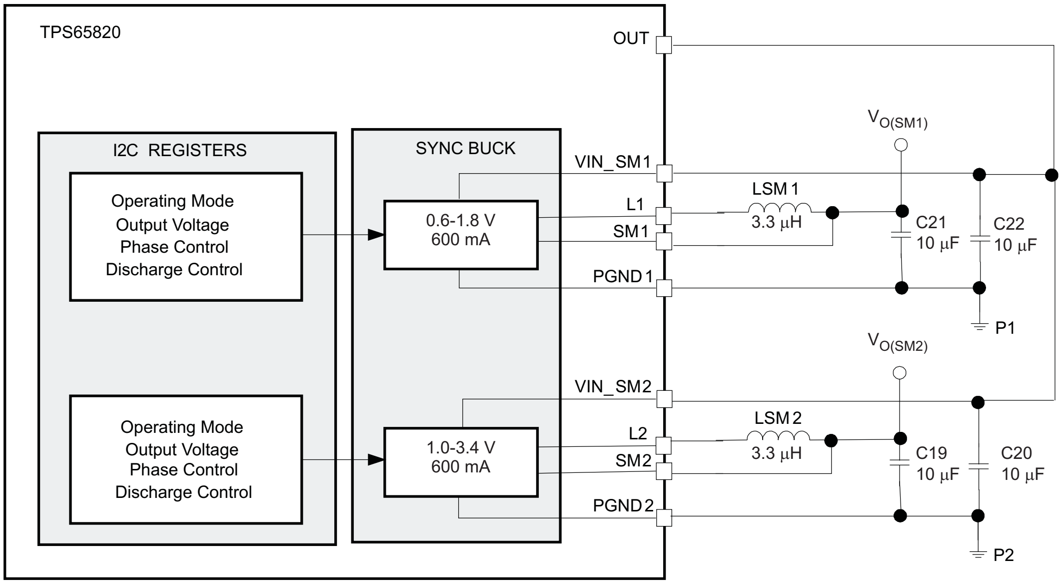


Figure 40. Required External Components, Recommended Values, External Connections

STEP-DOWN SWITCHED MODE CONVERTERS: SM1 and SM2

The TPS65820 has two highly efficient step down synchronous converters. The integration of the power stage switching MOSFETs reduces the external component count, and only the external output inductor and filter capacitor are required. The integrated power stage supports 100% duty cycle operation. Multiple operation modes are available, enabling optimization of the overall system performance under distinct load conditions.

The converters have two modes of operation: a 1.5 MHz fixed frequency pulse width modulation (PWM) mode at moderate to heavy loads, and a pulse frequency modulation (PFM) mode at light loads. The converter output voltage is programmable via I^{2}C registers SM1_SET1 and SM2_SET1.

When the SM1/SM2 converters are disabled an integrated switch automatically discharges the converter output capacitor. The discharge switch function can be disabled by setting the control bits DISCHSM1 and DISCHSM2 to LO, in I^{2}C registers SM1_SET2 and SM2_SET2.

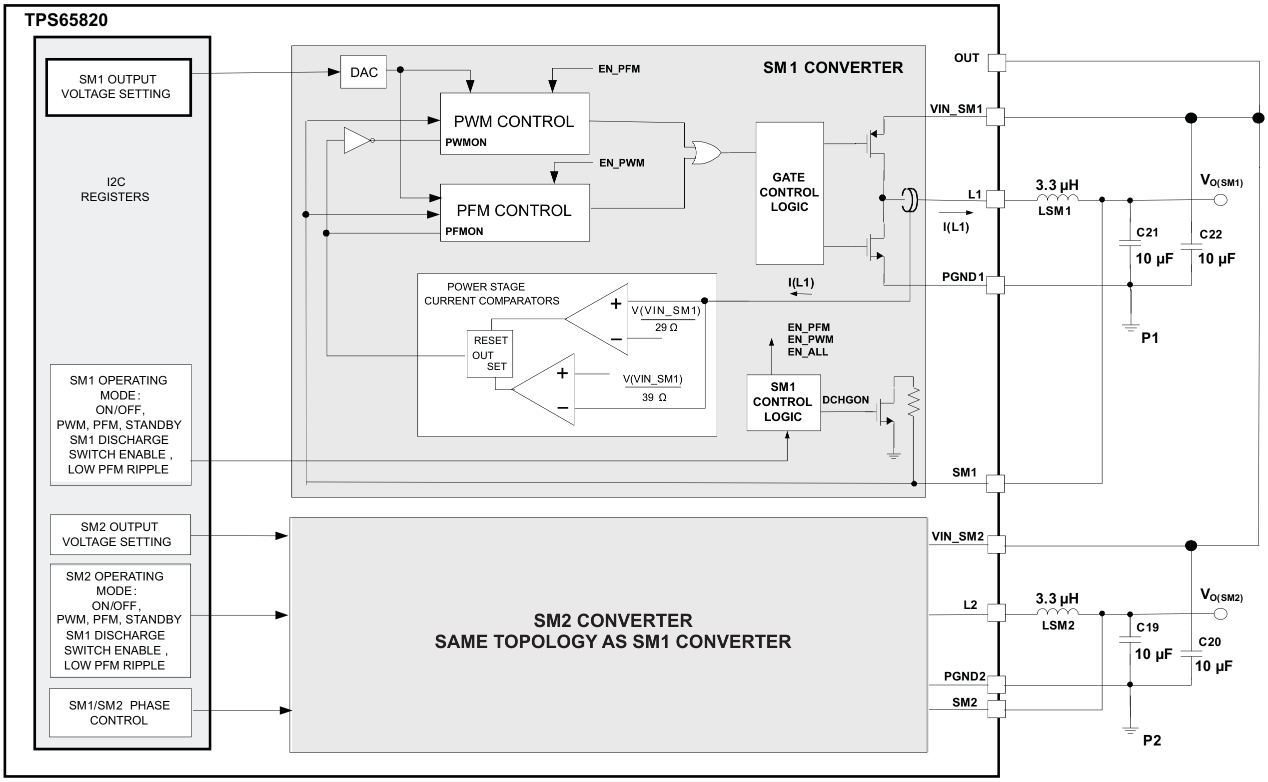


Figure 41. SM1/SM2 Converter

The TPS65820 SM1 and SM2 buck converters can be set to operate only in PWM mode or to switch automatically between PFM and PWM modes. The average load current is monitored, and the PFM mode is set if the average load current is below the threshold IPFM(ENTER). When in PFM mode the load current is also monitored, and the PWM mode is set when the load current exceeds the threshold $I_{PFM(LEAVE)}$. The thresholds for automatic PFM/PWM switching are calculated as shown in Equation 6 for the SM1 converter, the same thresholds apply to the SM2 converter by replacing VIN_SM1 by VIN_SM2 :

$$I_{PFM(LEAVE)} = \frac{V(VIN\_SM3)}{29\ \Omega}, \qquad I_{PFM(ENTER)} = \frac{V(VIN\_SM3)}{39\ \Omega} \tag{6}$$

The automatic switching mode is enabled via the control bits PFM_SM1 and PFM_SM2 on I2C registers SM1_SET1 and SM2_SET1.

Output Voltage Slew Rate

I2C registers enable setting the output voltage slew rate, when transitioning from one programmed voltage to a new programmed voltage value. These events can be triggered by a new output voltage selection or by switching from a low power mode (standby) to a normal operating mode. During a transition the output voltage will be stepped from the currently programmed voltage to the new target voltage. The slew rate from the initial voltage to the final voltage can be selected using I^{2}C registers, SM1_SET2 and SM2_SET2, ranging from 0.24 mv/µs to 15.36 mV/µs for the SM1 converter and 0.48 to 30.72 mV/µS for the SM2 converter. If the slew rate is set to OFF the output voltage will go from the current value to the programmed value in a single step.

During the transition to standby mode the Power Good comparators are disabled.

Soft Start

SM1 and SM2 have an internal soft start circuit that limits the inrush current during start-up. An initial delay (170 µsec typ) from the converter enabled command to the converter effectively being operational is required, to assure that the internal circuits of the converter are properly biased. At the end of that initial delay the soft start is initiated, and the internal compensation capacitor is charged with a low value current source. The soft start time is typically 750 µs, with the output voltage ramping from 5% to 95% of the final target value.

Dropout Opration at 100% Duty Cycle

The TPS65820 buck converters offer a low input to output voltage difference while still maintaining operation when the duty cycle is set to 100%. In this mode of operation the P-channel switch is constantly turned on, enabling operation with a low input voltage. The dropout operation will start if :

$$V(VIN\_SM1) \leq V(SM1) + I(L1)\left(R_{DSON(PSM1)} + R_L\right) \tag{7}$$

Where:

I(L1) = Output current plus inductor ripple current.

R_L = DC resistance of the inductor

Equation 7 can be also used for the SM2 converter, replacing SM1 by SM2 and L1 by L2.

Output Voltage Monitoring

The output voltage of converters SM1 and SM2 is monitored by internal comparators, and an output low voltage condition is detected when the output voltage is below 90% of the programmed value. The power good status for SM1 and SM2 is accessible via I2C, see interrupt controller section for more details.

The power good comparators for SM1 and SM2 are disabled during the transition to standby mode operation. They are enabled when the transition to standby mode is complete.

Stand-By Mode

Using the I^2C SM1 and SM2 can be set in stand-by mode. In STANDBY mode the PFM operation mode is set and the output voltage is defined by I^2C registers SM1_STANDBYand SM2_STANDBY, and it can be set to a value different than the normal mode output regulation voltage. The standby mode can also be set by the GPIO pins, if those are configured as control pins that define the SM1/SM2 operating mode.

PWM Operation

During PWM operation the converters use a fast response voltage mode controller scheme with input voltage feed-forward, enabling the use of small ceramic input and output capacitors. At the beginning of each clock cycle the P-channel MOSFET switch is turned on, and the oscillator starts the voltage ramp. The inductor current will ramp-up until the ramp voltage reaches the error amplifier output voltage, when the comparator trips and the p-channel MOSFET switch is turned off. Internal adaptative break-before-make circuits turn on the integrated n-channel MOSFET switch after an internal, fixed dead-time delay, and the inductor current ramps down, until the next cycle is started. When the next cycle starts the ramp voltage is reset to its low value and the p-channel MOSFET switch is turned on again.

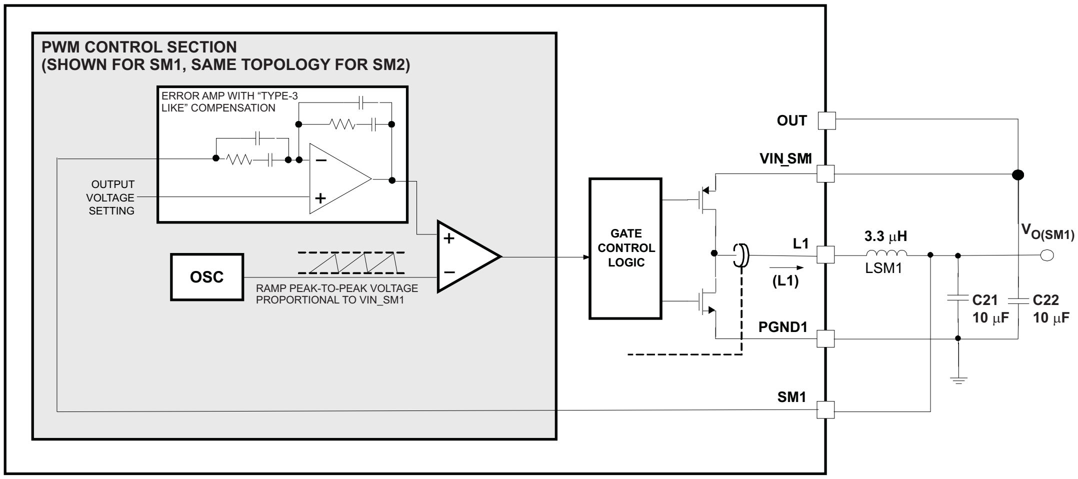


Figure 42. PWM Operation

The integrated power MOSFETs current is monitored at all times and the power MOSFET is turned off if its internal short circuit current limit is reached.

Phase Control in PWM Mode

The SM1 and SM2 converters operate synchronized to each other when both are in PWM mode, with converter SM1 as the master. I2C control register bits S1S2PHASE in register SM1_SET2 enables delaying the SM2 PWM clock with respect to SM1 PWM clock, selecting a phase shift from 0 to 270 degrees. The out-of-phase operation reduces the average current at the input node, enabling use of smaller input filter capacitors when both converters are connected to the same input supply.

PFM Mode Operation

Using the I^{2}C interface the SM1 and SM2 converters can have the automatic power saving PFM mode enabled. When the PFM mode is set the switching frequency is reduced and the internal bias currents are decreased, optimizing the converter efficiency under light load conditions.

In PFM mode the output voltage is monitored by a voltage comparator, which regulates the output voltage to the programmed value $V_{O(SM1)}$. If the output voltage is below $V_{O(SM1)}$ the PFM control circuit turns on the power stage, applying a burst of pulses to increase the output voltage. When the output voltage exceeds the target regulation voltage $V_{O(SM1)}$ the power stage is disabled, and the output voltage will drop until it is below the regulation voltage target, when the power stage is enabled again

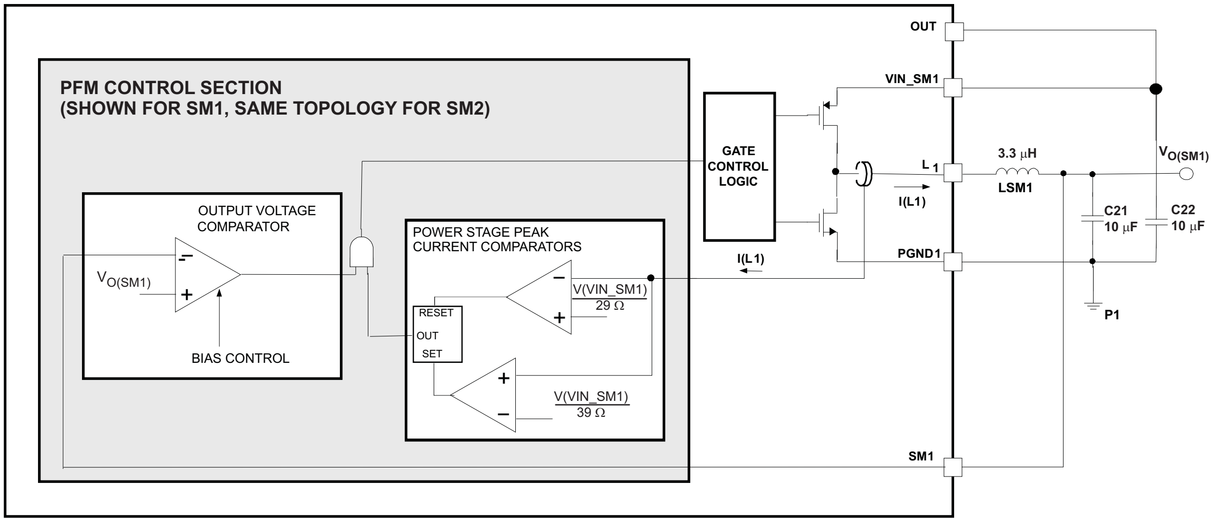


Figure 43. PFM Mode Operation

During burst operation two current comparators control the power stage integrated MOSFETs. These comparators monitor the instantaneous inductor current and compare it to the internal thresholds $I_{PFM(ENTER)}$ and $I_{PFM(LEAVE)}$, turning the p-channel switch on if the inductor current is less than $I_{PFM(LEAVE)}$ and turning it off if the inductor current exceeds $I_{PFM(ENTER)}$. The n-channel switch will be turned on when the p-channel MOSFET is off.

The PFM output voltage comparator quiescent current may be reduced using the I2C register bits PFM_RPL1 and PFM_RPL2 in registers SM1_SET and SM2_SET. The voltage comparator quiescent current is reduced if PFM_RPL1 and PFM_RPL2 bits are set to LO, and the comparator response time (t_{COMP}, see Figure 44) increases. A reduction in quiescent current increases the converter efficiency at light loads, at the expense of a larger output voltage ripple when in PFM mode.

The ripple is minimized if PFM_RPL1 and PFM_RPL2 bits are set to HI, at the expense of reduced efficiency under light loads. The operation under low and high ripple settings is described in Figure 44.

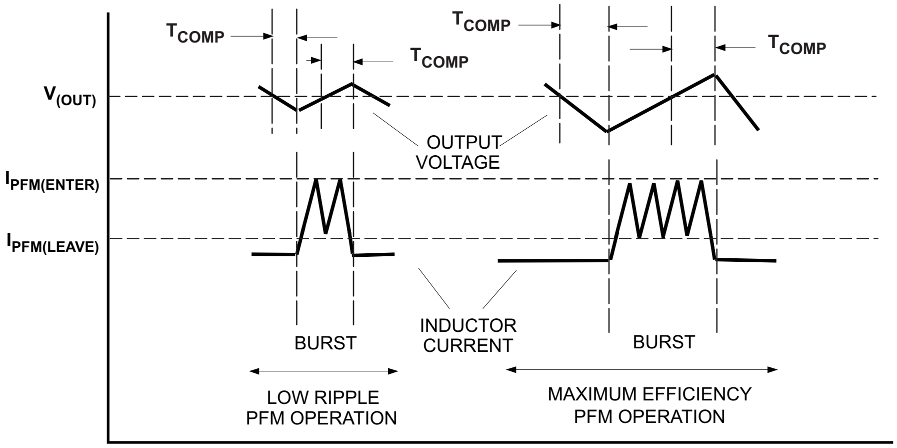


Figure 44. PFM mode operation waveforms

When a burst of pulses is generated the PFM current comparators will control the power stage MOSFETs to limit the inductor current to a value between the thresholds $I_{PFM(LEAVE)}$ and $I_{PFM(ENTER)}$. The number of pulses in a burst cycle will be proportional to the load current, and the average current will be always below $I_{PFM(LEAVE)}$ once PFM operation is set. The typical burst operation in PFM mode is shown in Figure 45.

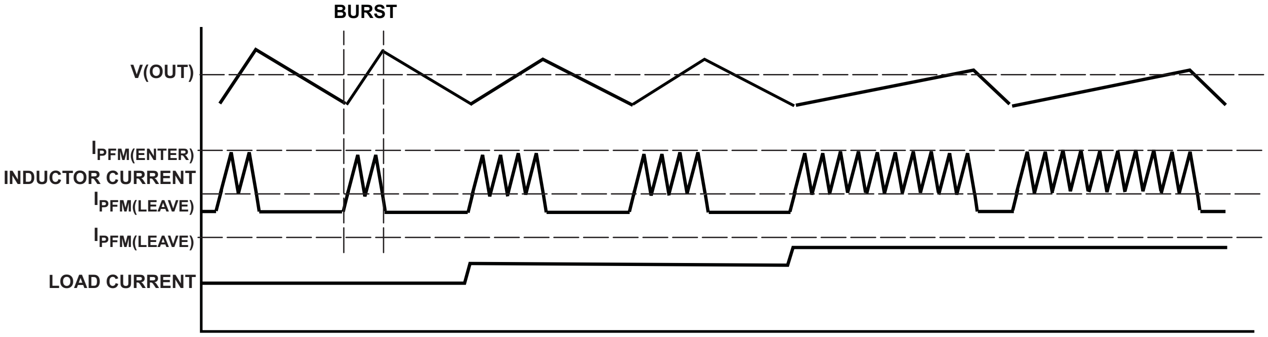


Figure 45. Typical Burst Operation in PFM Mode

The PFM operation is disabled and PWM operation set if one of the following events happen during PFM operation:

1. The total burst operation time exceeds 10 µs, typ.
2. The output voltage falls below 2% of the target regulation voltage.

The PFM mode can be disabled through the serial interface to force the individual converters to stay in fixed frequency PWM mode.

SWITCHED MODE STEP-DOWN CONVERTERS — I^2C REGISTERS

The I^2C registers that control buck converter-related functions are shown below. The HEX address for each register is shown by the register name, together with the R or W functionality for the register bits. Shaded values indicate default initial power-up values.

	B7	B6	B5	B4	B3	B2	B1	B0
SM1_SET1, ADDRESS=10, ALL BITS R/W								
Bit name	SM1 EN	PFM_RPL1	PFM_SM1	SetV4_SM1	SetV3_SM1	SetV2_SM1	SetV1_SM1	SetV0_SM1
Function	SM1 ON/OFF CONTROL	SM1 PFM FUNCTION OPERATION	SM1 PFM MODE ON/OFF CTRL	SM1 OUTPUT VOLTAGE REGULATION VALUE, STANDBY MODE NOT SET				
When 0	OFF	MAXIMIZE EFFICIENCY	PWM/PFM	See Table 9 for SM1, SM2 voltage setting, **Power up default=1.24 V**				
When 1	ON	MINIMIZE OUTPUT RIPPLE	Only PWM					
SM1_SET2, ADDRESS=11, ALL BITS R/W								
Bit name	NOT USED	STANDBY_SM 1	DISCHSM1	S1S2PHASE_1	S1S2PHASE_0	SLEWSM1_2	SLEWSM1_1	SLEWSM1_0
Function	NOT USED	SM1 STANDBY MODE ON	SM1 output discharge switch enable	SM2 PWM CLOCK DELAY, WITH RESPECT TO SM1 PWM CLOCK		SM1 OUTPUT SLEW RATE SETTING		
When 0	NOT USED	OFF	OFF	00 = 0 **10 = 180** 01 = 90 11 = 270 Units: degrees **Default= 180**		000 = 0.24 010 = 0.96 100 = 5.84 **110 = 15.36** 001 = 0.48 011 = 1.92 101 = 7.68 111 = IMMEDIATE Unit: mV/µSec **Default= 15.36**		
When 1	NOT USED	ON	ON					
SM1_STANDBY, ADDRESS=12, B4-B0 R/W, B7-B5 READ ONLY								
Bit name	NOT USED	NOT USED	NOT USED	SetV4_SM1SL	SetV3_SM1SL	SetV2_SM1SL	SetV1_SM1SL	SetV0_SM1SL
Function	NOT USED	NOT USED	NOT USED	SM1 OUTPUT VOLTAGE REGULATION VALUE, STANDBY MODE SET				
When 0	NOT USED	NOT USED	NOT USED	See Table 9 for SM1, SM2 voltage setting, **Power up default=1.24 V**				
When 1	NOT USED	NOT USED	NOT USED					
SM2_SET1, ADDRESS=13, ALL REGISTER BITS R/W								
Bit name	SM2 EN	PFM_RPL2	PFM_SM2	SetV4_SM2	SetV3_SM2	SetV2_SM2	SetV1_SM2	SetV0_SM2
Function	SM2 ON/OFF CONTROL	SM2 PFM FUNCTION OPERATION	SM2 PFM MODE ON/OFF CTRL	SM2 OUTPUT VOLTAGE REGULATION VALUE, STANDBY MODE NOT SET				
When 0	OFF	MAXIMIZE EFFICIENCY	PWM/PFM	See Table 9 for SM1, SM2 voltage setting,**Power up default=1.80 V**				
When 1	ON	MINIMIZE OUTPUT RIPPLE	ONLY PWM					
SM2_SET2, ADDRESS=14, ALL REGISTER BITS R/W								
Bit name	NOT USED	STANDBY_SM 2	DISCHSM2	NOT USED	NOT USED	SLEWSM2_2	SLEWSM2_1	SLEWSM2_0
Function	NOT USED	SM1 STANDBY MODE ON	SM1 output discharge switch enable	NOT USED	NOT USED	SM2 OUTPUT SLEW RATE SETTING		
When 0	NOT USED	OFF	OFF	NOT USED	NOT USED	000 = 0.48 010 = 1.92 100 = 7.68 **110 = 30.72** 001 = 0.096 011 = 3.84 101 = 15.36 111 = IMMEDIATE Unit: mV/µSec **Default= 30.72**		
When 1	NOT USED	ON	ON	NOT USED	NOT USED			
SM2_STANDBY, ADDRESS=15, ALL REGISTER BITS R/W								
Bit name	NOT USED	NOT USED	NOT USED	SetV4_SM2SL	SetV3_SM2SL	SetV2_SM2SL	SetV1_SM2SL	SetV0_SM2SL
Function	NOT USED	NOT USED	NOT USED	SM1 OUTPUT VOLTAGE REGULATION VALUE, STANDBY MODE SET				
When 0	NOT USED	NOT USED	NOT USED	See Table 9 for SM1, SM2 voltage setting, **Power up default=1.8 V**				
When 1	NOT USED	NOT USED	NOT USED					

Table 9. Set Voltages for SM1 and SM2 (including STAND-BY)

SetV4_ SM	SetV3_ SM	SetV2_ SM	SetV1_ SM	SetV0_ SM	Vset SM1	Vset SM2	SetV4_ SM	SetV3_ SM	SetV2_ SM	SetV1_ SM	SetV0_ SM	Vset SM1	Vset SM2
0	0	0	0	0	0.6	1	1	0	0	0	0	1.24	2.28
0	0	0	0	1	0.64	1.08	1	0	0	0	1	1.28	2.36
0	0	0	1	0	0.68	1.16	1	0	0	1	0	1.32	2.44
0	0	0	1	1	0.72	1.24	1	0	0	1	1	1.36	2.52
0	0	1	0	0	0.76	1.32	1	0	1	0	0	1.4	2.6
0	0	1	0	1	0.8	1.4	1	0	1	0	1	1.44	2.68
0	0	1	1	0	0.84	1.48	1	0	1	1	0	1.48	2.76
0	0	1	1	1	0.88	1.56	1	0	1	1	1	1.52	2.84
0	1	0	0	0	0.92	1.64	1	1	0	0	0	1.56	2.92
0	1	0	0	1	0.96	1.72	1	1	0	0	1	1.6	3
0	1	0	1	0	1	1.8	1	1	0	1	0	1.64	3.08
0	1	0	1	1	1.04	1.88	1	1	0	1	1	1.68	3.16
0	1	1	0	0	1.08	1.96	1	1	1	0	0	1.72	3.24
0	1	1	0	1	1.12	2.04	1	1	1	0	1	1.76	3.32
0	1	1	1	0	1.16	2.12	1	1	1	1	0	1.8	3.4
0	1	1	1	1	1.2	2.2	1	1	1	1	1	0.6	1.0

SM1,SM2 PHASE			SMX_SLEW RATE, SMX=SM1 OR SM2				
S1S2_PHASE1	**S1S2_PHASE0**	**PHASE**	**SLEWX_2**	**SLEWX_1**	**SLEWX_0**	**SM1 mV/µs**	**SM2 mV/µs**
0	0	0	0	0	0	0.24	0.48
0	1	90°	0	0	1	0.48	0.96
1	0	180°	0	1	0	0.96	1.92
1	1	270°	0	1	1	1.92	3.84
			1	0	0	5.84	7.68
			1	0	1	7.68	15.36
			1	1	0	15.36	30.72
			1	1	1	Immediate	

FUNCTIONALITY GUIDE – ANALOG TO DIGITAL CONVERTER

10 BIT SUCCESSIVE APPROXIMATION ADC								
ADC Input Channels		**Trigger Mode**	**Conversion Count**	**Converter Mode**	**Trigger Delay**		**Wait Time, Multiple Conversions**	**Power Up Default**
Internal	**External**				**Range**	**Min Step**		
Charge Current, Thermistor temperature, IC junction temperature, RTC_OUT voltage, OUT voltage, Battery voltage	ANLG1 and ANLG2 voltages	GPIB, I^2C driven, Repeat	1, 4, 8, 16, 32, 64, 128, 256	Single, Average, Find max value, Find min value	0-750 µs, 16 steps	50 µs	µs: 20, 40, 60, 80, 160, 240, 320, 640 ms: 1.28, 1.92, 2.56, 5.12, 10.24, 15.36, 20.48	ADC off
Fixed internally	Selectable via I^2C	Selectable via I^2C	Selectable via I^2C	Selectable via I2C	Selectable via I^2C	Selectable via I^2C	Selectable via I^2C	

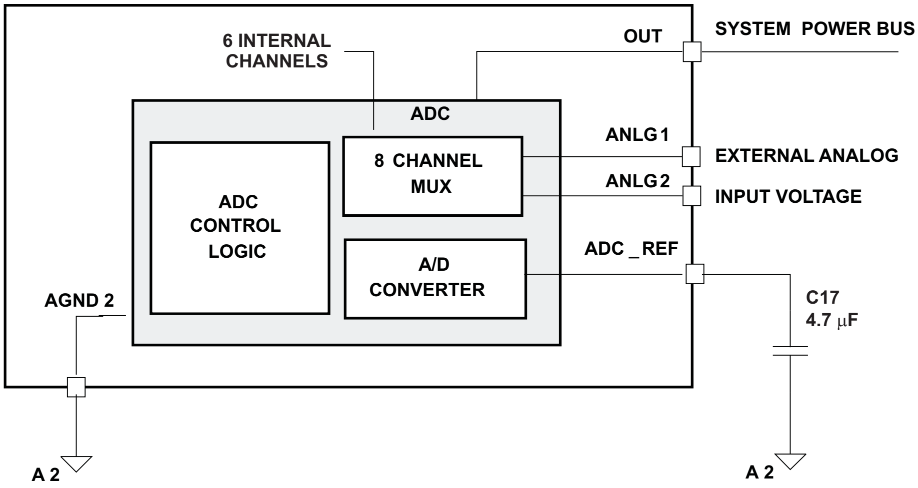


Figure 46. Required External Components, Recommended Values, External Connections

ANALOG TO DIGITAL CONVERTER

Overview

The TPS65820 has a 10 bit integrated successive approximation A/D, capable of running A/D conversions on eight distinct channels in a variety of modes. Two of the eight channels are connected to uncommitted pins ANLG1 and ANLG2, and can be used to convert external voltages. The other six channels monitor system parameters which are critical to the overall system monitoring. The channel selection is set via I^2C.

A dedicated set of I^2C registers enables configuration of the ADC to perform a conversion cycle with either a single conversion or a multiple conversions. The ALU generates a data set containing maximum value detection, minimum value detection and average value calculation for each conversion cycle. Each cycle can be performed a single time or multiple times.

Input Channels

The following channels are available for selection via the I2C register ADC_SET bits CHSEL_SET bits:

Table 10. ADC input channel overview

Channel	Connection	Parameter Sampled	Voltage Range Under Normal Operating Conditions	Special Features	Full Scale Reading (Internal reference selected)	LSB value
CH1	ANLG1 pin	User defined	User defined	Internal pull-up current source programmable via I2C : 0/ 10/50/60 µA	2.535 V	Full scale reading ÷ 1023
CH2	ANLG2 pin				2.535 V	
CH3	ISET1 pin	Voltage proportional to charge current	0 V (charger off) to 2.525 V (fast charge)	—	2.535 V	
CH4	TS pin	Voltage proportional to pack temperature	0 V (short) to 4.7v (no thermistor)	Internal 20 µA pull-up current source (ON only when AC/USB are present)	2.535 V	
CH5	Internal junction temperature	Voltage proportional to IC junction temperature	1.85 V at T_J = 25°C, –6.5 mV/°C slope typ	—	2.535 V	
CH6	RTC_OUT pin	Internal LDO output voltage	0 V to 3.3 V	—	4.7 V	
CH7	OUT pin	System Power bus voltage	0 V to 4.4 V	—	4.7 V	
CH8	BAT pin	Battery pack positive terminal voltage	0 V to 4.4 V	—	4.7 V	

FUNCTIONAL OVERVIEW

The TPS65820 ADC can be subdivided in four sections:

1. **Input selection:** The input selection section has two major blocks, the input bias control and an 8 channel MUX. The input bias control provides the bias currents that are applied to pins ANLG1 and ANLG2 and pin TS. The TS pin bias current is fixed (20 µA typ) , and the bias currents for pins ANLG1 and ANLG2 are set on I2C register ADC_WAIT.

   The TS and ANLG1 pin current sources are automatically enabled when the input power is detected, providing the required setup to measure a pack thermistor temperature (TS pin) or a battery ID resistor (ANLG1 pin). ANLG1 and ANLG2 can be used to measure external resistive loads or analog voltages. The bias current sources are always connected to the OUT pin internally.

   The internal MUX connects one of the monitored analog inputs to the ADC engine, following the selection defined on register ADC_SET.

2. **ADC engine:** The ADC engine uses an internal or external voltage reference, as defined by the ADC_REF bit on the ADC_SET control register. If the internal reference is selected ADC_REF is connected to an internal LDO that regulates the ADC_REF pin voltage to generate the ADC supply and internal voltage reference. The internal LDO maximum output current is 6 mA typical, and a conversion should be started only after the external capacitor is fully charged.

   If an external reference is used it should be connected to the ADC_REF pin. When an external reference is selected the internal LDO connected to ADC_REF is disabled. Care must be taken when selecting an external reference as the ADC reference voltage , as it affects the ADC LSB absolute value.

3. **Trigger control and synchronization :** The ADC engine starts a conversion of the selected input when the trigger control circuit sends a start command. The trigger control circuit starts the ADC conversion and transfers the ADC output data to the arithmetic logic unit (ALU) at the end of the conversion. It also synchronizes the data transfer from the ALU to the I2C ADC_READING register at the end of a conversion cycle, and generates the ADC status information sent to the ADC registers.

   An ADC engine conversion is triggered by the TPS65820 trigger control circuit using either an internal trigger or an external trigger. The internal trigger is automatically generated by the TPS65820 at the end of each ADC engine conversion, following the timing parameters set on I2C registers ADC_SET, ADC_DELAY and ADC_WAIT.

   The GPIO3 pin can be used as an external trigger if the bit ADC_TRG_GPIO3 is set HI , in the I2C register ADC_DELAY. In the external trigger mode a new conversion is started after the GPIO3 pin has an edge transition, following the timing parameters set on I2C registers ADC_SET, ADC_DELAY and ADC_WAIT.

4. **Arithmetic Logic Unit (ALU):** The ALU performs mathematical operations on the ADC output data as defined by the I2C ADC_READING registers. It executes average calculations or minimum /maximum detection. The result of the calculations is stored in a 11 bit accumulator register (1 bit allocated for carry-over). The accumulator value is transferred to the I2C data register at the end of a conversion cycle.

A simplified block diagram for the ADC is shown in Figure 47.

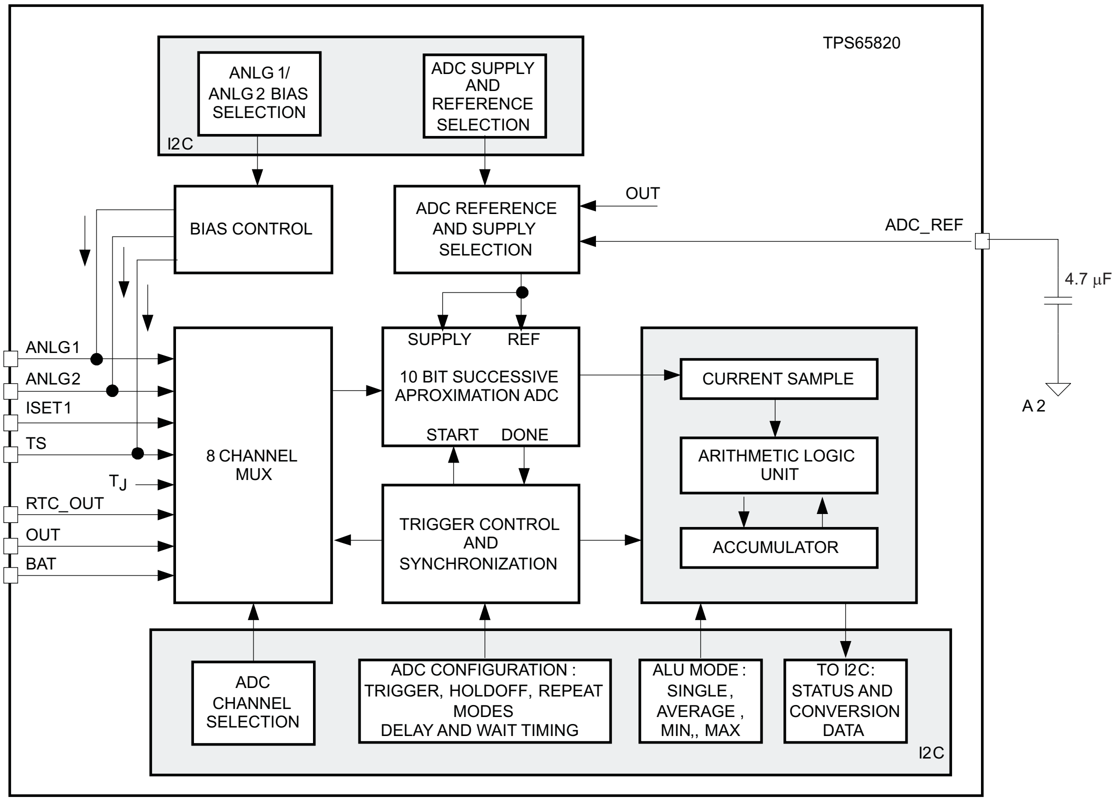


Figure 47. ADC Simplified Block Diagram

ADC Conversion Cycle

A conversion cycle includes all the steps required to successfully sample the selected input signal and transfer the converted data to the I2C, generating an interrupt request to the host (pin : HI→LO) . The number of individual conversions (samples) in a conversion cycle is defined by the I2C ADC_SET register bits READ_MODE settings, and can range from a single sample to 256 samples. The conversion cycle settings for the ALU is defined by register ADC_READING and it can be set to average, maximum value detection, minimum value detection or no processing (ADC engine output loaded in the accumulator directly).

The conversion cycle starts with the first sampling and ends when:

- The required ALU operations are performed on the final sample, and
- The ALU accumulator data is transferred to the I2C ADC_READING register, and
- The register bit ADC_STATUS in the ADC_READING register is set to LO.

A conversion cycle is always started by the external host when the ADC_EN bit in the ADC_SET register is toggled from LO to HI by a I2C write operation. Resetting the ADC_EN bit to LO before the current conversion cycle ends ($\overline{\text{INT}}$: LO → HI, ADC_STATUS bit set to LO) is not recommended, as the ADC will keep its current configuration until the current conversion cycle ends.

At the end of a conversion cycle the output data is stored at registers in the ALU block. The ADC_STATUS bit is set to LO (DONE) and an interrupt is generated ($\overline{\text{INT}}$ pin : HI→LO) if the ADC_STATUS bit is unmasked, at the interrupt masking registers INT_MASK. It should be noted that the minimum, maximum and average values are ALWAYS calculated by the ALU for each conversion cycle.

The value loaded in the I^2C registers ADC READING_HI and ADC READING_LO at the end of a conversion cycle is defined by control bits ADC_READ0 and ADC_READ1 in register ADC READING_HI. The average, minimum, maximum and last sample values for a conversion cycle can be read if the external host executes an I^2C write operation, changing the values of bits ADC_READ0 and ADC_READ1, followed by an I^2C read operation on registers ADC READING_HI and ADC READING_LO. The minimum, maximum, average and last values will have the same value if a conversion cycle with only one sample is executed .

The ADC_READ0 and ADC_READ1 bits *can not be modified* during the execution of a conversion cycle. A new conversion cycle should be started *only after* the current conversion cycle is completed, by toggling the ADC_EN bit from HI to LO and HI again.

External Trigger Operation

The trigger control circuit can be programmed to use an external signal to start a conversion. The TPS65820 GPIO3 input is configurable as an ADC trigger, with ADC conversion starting on either a rising edge or falling edge. When using an external trigger the trigger delay , trigger wait time delay and trigger holdoff mode can be programmed using I2C registers.

The procedure to start an externally-triggered conversion cycle has the following steps:

1. Verify that the current conversion cycle has ended (ADC_STATUS=LO, I^2C register ADC_READING_HI)
2. Set ADC_EN=LO
3. Configure ADC sampling mode, ALU mode , trigger parameters, etc.
4. Set ADC_EN=HI

After step 4 the ADC is armed, waiting for an external trigger detection to start a conversion cycle. Similarly to the non-triggered mode, the ADC configuration *should not be modified until the current conversion cycle ends*. Note that in the external trigger mode the current cycle does not end if the converter is armed and an external trigger is not detected.

Detecting an External Trigger Event

An external trigger event is detected when the GPIO3 input has an edge that matches the edge detection programmed in the EDGE bit, at the I^2C register ADC_DELAY. The internal ADC trigger can be delayed with respect to the external trigger signal edge. The delay time value is set by the ADC_DELAY register bits DELAY_n, and can range from 0 µs (no delay) to 750 µsec. A conversion will be started only if the external trigger remains at its active level when the delay time expires, as shown in Figure 48. In a positive-edge detection the active trigger level is HI; in a negative-edge detection the active trigger level is LO.

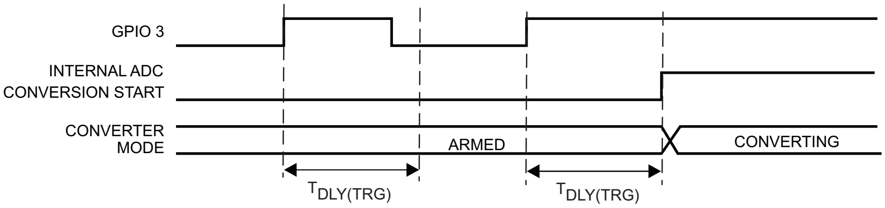


Figure 48. ADC Conversion Triggerd by GPIO3 Positive Edge Triggered Active Level Hi

Executing Multiple Sample Cycles With an External Trigger

When executing conversion cycles that require multiple samples it may be desirable to synchronize the input signal conversion using either an external trigger that has a periodic repetition rate or an external asynchronous trigger that indicates when the external input signal being converted is valid. The TPS65820 has additional operating modes and timing parameters that can be programmed using the I2C to configure multiple sample conversion cycles.

In multiple sample cycles the host can select the wait time between samples using the bits WAITn in the ADC_WAIT register to set the wait time between samples. The wait time is measured between the end of a conversion and the start of a new conversion.

With the default power-up settings (HOLDOFF=LO, ADC_DELAY register) the TPS65820 will execute a multiple sample conversion cycle if the first sample is taken when the trigger is at its active level. Subsequent samples will be converted at the end of the wait time, even if the trigger returns to the non-active level. The external trigger level edge is ignored until the current conversion cycle ends.

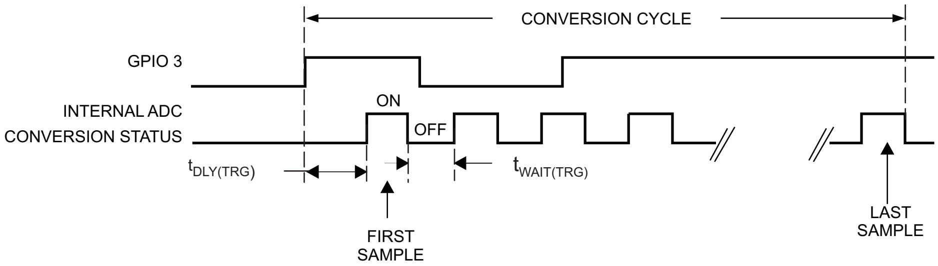


Figure 49. ADC Conversion Triggerd by GPIO3 Positive Edge Triggered Active Level Hi; Holdoff = LC

If the sample conversion needs to be synchronized with an external trigger, during multiple sample conversion cycles, the control bit HOLDOFF should be set to HI. When the holdoff mode is active the internal trigger will start a sample conversion only if the external trigger was detected and is at its active level at the end of the wait time, as shown in Figure 50.

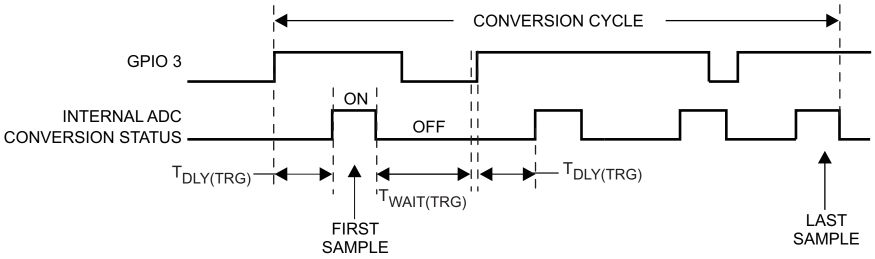


Figure 50. ADC Conversion Triggerd by GPIO3 Positive Edge Triggered Active Level Hi; Holdoff = Hi 4 Sample Cycle

When the multiple sample cycles are executed the host must configure the maximum and minimum limits for the ADC output using registers DLOLIM1, DLOLIM2, DHILIM1 and DHILIM2. A conversion cycle will end if any individual conversion result exceeds the maximum limit value or is below the minimum limit value. When an out of limit conversion is detected an interrupt is sent to the host, and the ADC_STATUS bit on register ADC READING_HI is set to DONE .

Continuous Conversion Operation (Repeat Mode)

The TPS65820 ADC can be set to operate in a continuous conversion mode, with back-to-back conversion cycles executed. The REPEAT mode is targeted at applications where an input is continuously monitored for a period of time, and the host must be informed if the monitored input is out of the range set by I^2C registers DLOLIM1, DLOLIM2, DHILIM1 and DHILIM2 . In REPEAT mode each conversion is started when the ADC trigger (internal or external) is detected, and a new conversion cycle is started when the current conversion cycle ends. All the trigger and sampling modes available for normal conversion cycles are available in repeat mode. Executing I2C read operations to get the ADC readings for average, minimum, maximum and last sample values is possible in REPEAT mode. However, this is not a recommended operation , as the REPEAT mode does not generate a DONE status flag making it difficult to synchronize the ADC data reading to the end of a conversion cycle.

The recommended use of the REPEAT mode is :

1. Configure the ADC conversion cycle : trigger mode, sample mode, select input signal, etc.
2. Configure the HI and LO limits for the ADC readings
3. Set the ADC_DELAY register bit REPEAT to HI
4. Toggle ADC_DELAY register bit ADC_EN bit from LO to HI

5. Monitor the INT pin. An interrupt triggered by ADC_STATUS=LO indicates that the selected input signal is out of range

To exit the continuous mode the host must follow the steps below, if external trigger mode was set :

1. Exit external trigger mode
2. Set REPEAT bit to LO, effectively terminating the repeat mode. This will generate an additional conversion, at the end of this conversion the ADC will be ready for a new configuration
3. Set ADC_EN to LO, after on-going conversion ends

   To exit the continuous mode the host must follow the steps below, if internal trigger mode was set :

1. Set REPEAT bit to LO, effectively terminating the repeat mode.
2. Set ADC_EN to LO, after on-going conversion ends

ADC Input Signal Range Setting

The registers DHILIMn and DLOLIMn can be used by the host to set maximum and minimum limits for the DAC engine output. At the end of each conversion the ADC output is checked for the maximum and minimum limits, and a status flag is set if the converted data exceeds the high limit or is under the low limit. In multiple sample operation the converted data range is checked when all programmed samples have been converted.

The host can mask or unmask interrupts caused by the ADC range status bits using the INT_MASKn registers.

ADC State Machine

The ADC state machine with all the trigger and operation modes is shown in Figure 51.

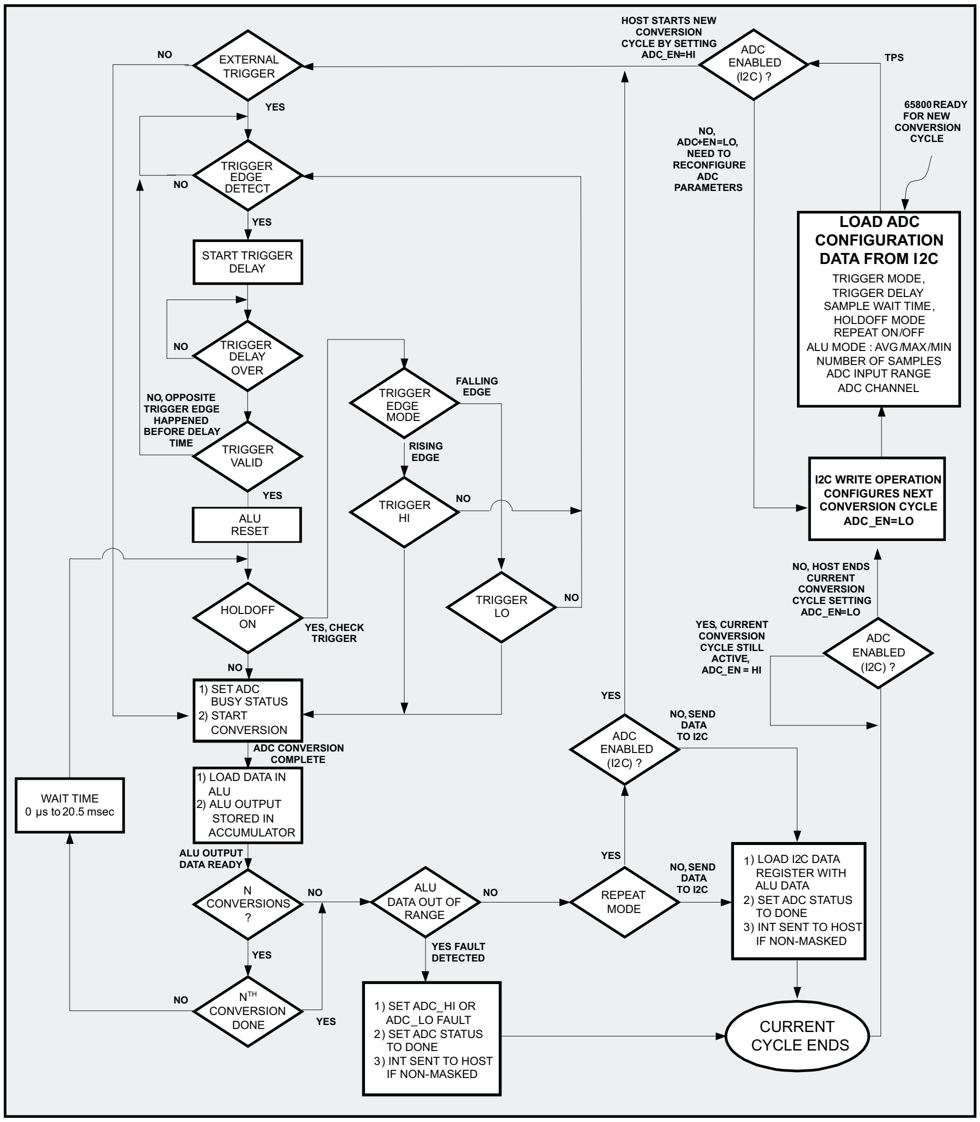


Figure 51. Trigger and Operation Modes for the ADC State Machine

BATTERY DETECTION CIRCUIT

The ANLG1 pin has an internal current source connected between OUT and ANLG1, which will be automatically turned on when the OUT pin voltage exceeds the minimum system voltage set by the SYS_IN pin external resistive divider. The current levels for ANLG1 pin can be programmed via I2C register ADC_WAIT, bits BATID_n. An integrated switch discharges the BAT pin to AGND1 when V(ANLG1)> V(OUT) – $V_{(NOBATID)}$, enabling implementation of a battery removal function if an external pack resistor ID is connected between ANLG1 and ground.

The ANLG1 pin may be used to monitor other parameters than a pack ID resistor. When ANLG1 pin is used as a generic ADC analog input V(ANLG1) should never exceed V(OUT) – $V_{(NOBATID)}$, to avoid undesired battery discharge caused by activation of the battery pin discharge circuit.

ADC – I^{2}C REGISTERS

The I^{2}C registers that control ADC-related functions are shown below. The HEX address for each register is shown by the register name, together with the R or W functionality for the register bits. Default, initial power-up values are shown in bold. In the timing equations, replace Bn with 1 for HI state, and 0 for LO state.

	B7	B6	B5	B4	B3	B2	B1	B0
ADC_SET, ADDRESS=1E, ALL BITS R/W								
Bit Name	ADC_ENABLE	ADC_REF_EN	CHSEL2_SET	CHSEL1_SET	CHSEL0_SET	READ_MODE2	READ_MODE1	READ_MODE0
Function	ADC ON/OFF CONTROL	ADC REFERENCE SELECTION	ADC CHANNEL SELECTION			ADC SAMPLING SETTINGS		
When 0	OFF	Internal	**000=ANLG1** 010= V(ISET1) 100= Tj 110= V(OUT) 001=ANLG2 011=V(TS) 101 = V(RTC_OUT) 111=V(BAT) **Default= ANLG1**			**000=1** 010= 8 100= 32 110= 128 001=4 011=16 101 = 64 111=256 **Default= 1**		
When 1	ON	External						
ADC READING,_HI, ADDRESS=1F, BITS B3/B4 R/W, ALL OTHER BITS READ ONLY								
Bit Name	ADC_STATUS	NOT USED	NOT USED	ADC_READ1	ADC_READ0	D10	D9_MSB	D8
Function	CURRENT CONVERSION STATUS	NOT USED	NOT USED	ALU OUTPUT DATA SELECTION		ADC AVERAGE CARRYOVER BIT	ADC CONVERSION OUTPUT BITS	
When 0	DONE	NOT USED	NOT USED	**00=LAST** 10 = MAXIMUM 01=AVERAGE 11 = MINIMUM **Default= LAST**			VALID ONLY AFTER ADC CONVERSION ENDS SEE ADC_READING_LO	
When 1	BUSY	NOT USED	NOT USED					
ADC READING_LO, ADDRESS=20, READ ONLY								
Bit Name	D7	D6	D5	D4	D3	D2	D1	D0_LSB
Function	ADC CONVERSION OUTPUT BITS , VALID ONLY AFTER ADC CONVERSION ENDS							
Value	VALUE=[B10*512 + B9*256 + B8*128 + B7*64 + B6*32 + B5*16 + B4*8 + B3*4 + B2*2 + B1] * [VRNG(CHn) / 1023] ; Unit=Volts, **The LSB bit value is proportional to the ADC reference voltage - See $V_{RNG(CHn)}$ in electrical parameters**							
DHILIM2, ADDRESS=22, ALL BITS R/W								
Bit Name	DHILIM7	DHILIM6	DHILIM5	DHILIM4	DHILIM3	DHILIM2	DHILIM1	DHILIM0_LSB
Function	ADC CONVERTER MAXIMUM INPUT VOLTAGE LIMIT SETTING							
Value	VALUE=[B10*512 + B9*256 + B8*128 + B7*64 + B6*32 + B5*16 + B4*8 + B3*4 + B2*2 + B1] * [$V_{RNG(CHn)}$ / 1023] ; Unit=Volts, **The LSB bit value is proportional to the ADC reference voltage - See $V_{RNG(CHn)}$ in electrical parameters**							
DHILIM1, ADDRESS=22, ALL BITS R/W					**DLOLIM1, ADDRESS=23, ALL BITS R/W**			
Bit Name	NOT USED	DHILIM10	DHILIM9	DHILIM8	NOT USED	DLOLIM10	DLOLIM9	DLOLIM8
Function	NOT USED	ADC CONVERTER MAXIMUM INPUT VLTG LIMIT SETTING			NOT USED	ADC CONVERTER MIN INPUT VLTG LIMIT SETTING		
Value	NOT USED	SEE REGISTER DHILIM2			NOT USED	SEE REGISTER DHILIM1		
DLOLIM2, ADDRESS=24, ALL BITS R/W								
Bit Name	DLOLIM7	DLOLIM6	DLOLIM5	DLOLIM4	DLOLIM3	DLOLIM2	DLOLIM1	DLOLIM0_LSB
Function	ADC CONVERTER MINIMUM INPUT VOLTAGE LIMIT SETTING							
Value	VALUE=[B10*512 + B9*256 + B8*128 + B7*64 + B6*32 + B5*16 + B4*8 + B3*4 + B2*2 + B1] * [$V_{RNG(CHn)}$ / 1023] ; Unit=Volts, **The LSB bit value is proportional to the ADC reference voltage - See $V_{RNG(CHn)}$ in electrical parameters**							
ADC_DELAY, ADDRESS=25,ALL BITS R/W								
Bit Name	ADC_TRG_GPIO3	EDGE _GPIO3	HOLDOFF	REPEAT	Delay_3	Delay_2	Delay_1	Delay_0
Function	USE GPIO3 AS ADC TRIGGER	GPIO3 TRIGGER MODE	ADC HOLDOFF ON/OFF CONTROL	REPEAT MODE ON/OFF	ADC EXTERNAL TRIGGER DELAY SETTING			
When 0	OFF	Falling Edge	OFF	OFF	$T_{DLY(TRIG)}$= B4*400 + B3 * 200 + B2*100 + B1* 50 , Units=µSec **Default=0µSec**			
When 1	ON	Rising Edge	ON	ON				
ADC_WAIT, ADDRESS=26, ALL BITS R/W								
Bit Name	ADC_cH2I_D1	ADC_cH2I_D0	BATIDI_D1	BATIDI_D0	WAIT_D3	WAIT_D2	WAIT_D1	WAIT_LSB
Function	ANLG2 PULL-UP CURRENT SOURCE VALUE		ANLG1 PULL-UP CURRENT SOURCE VALUE		ADC SAMPLE WAIT TIME, MULTIPLE SAMPLES MODE			
When 0	11:60 µA, 10:50 µA, 01:10 µA,**00: 0** **Default= 00**		11:60 µA, 10:50 µA, 01:10 µA, **00: WEAK PULL UP** **Default : 00**		**0000=0** 0100=0.08 1000=0.64 1100=5.12 0001= 0.02 0101=0.16 1001=1.28 1101=10.24 0010=0.04 0110=0.24 1010=1.92 1110=15.36 0011=0.06 0111=0.32 1011=2.56 1111=20.48 Units=µSec **Default=0**			
When 1								

FUNCTIONALITY GUIDE — LED AND PERIPHERAL DRIVERS

WHITE LED CONSTANT CURRENT DRIVER

Driver	PWM		Output Voltage	LED Current			Eff (%)	Power Up Default
	Duty Cycle Range	# of Steps		Io(Typ)	Max	Acc (%)		
SM3	Off (0%), 0.4% -99.6% Set via i2c	256	5 V–25 V	Set by external resistor	25 mA	25	80	Off (0%)

OPEN DRAIN PWM DRIVERS

Driver	PWM Freq (kHz)	PWM Duty Cycle			Io(max) mA	Power Up Default
		Range	# of Steps	Min Step		
PWM	0.5/1/1.5/2/3/ 4.5/7.8/15.6 Set via I^2C	Off (0%), 6.25% to 100 Set via I^2C	8	6.25%	150	Off(0%)
LED_PWM	15.625 or 23.4 , set via I^2C	Off(0%), 0.4% to 99.6% Set via I^2C	256	0.4%	150	Off (0%)

RGB OPEN DRAIN LED DRIVER

Driver	Flash Period (same for RGB)			Flash On time (same for RGB)			Brightness (Individual R/G/B Control)			Io mA	Power Up Default
	Range	# of Steps	Min Step	Range	# of Steps	Min Step	Duty (%)	# of Steps	Min Steps		
RED, GREEN, BLUE	No flash, or 1–8 sec Set via i2c	16	0.5 sec	0.1–0.6 sec Set via i2c	8	0.1 sec	Off (0%), 3.125 to 96.87 Set via i2c	32	3.125%	0/4/8/12	Flash Off, 0 mA, 0% brightness duty cycle

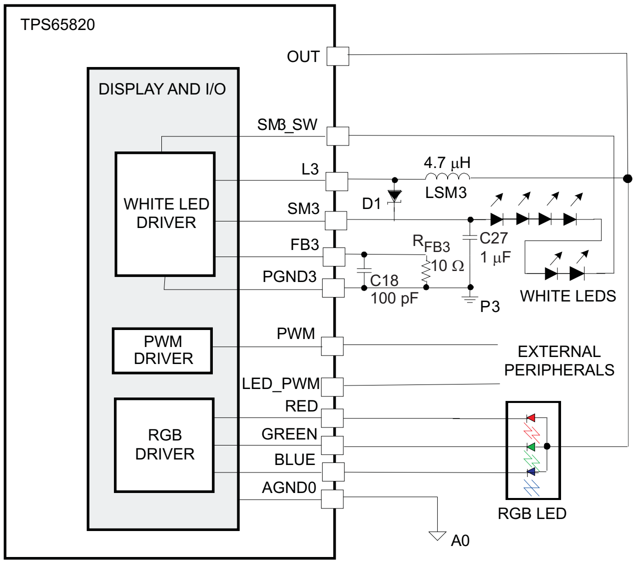


Figure 52. Required External Components, Recommended Values, External Connections

WHITE LED CONSTANT CURRENT DRIVER

The TPS65820 has an integrated boost converter (SM3) that is optimized to drive white LEDs connected in a series configuration. Up to six series white LEDs can be driven, with programmable current and duty cycle adjustable via a dedicated I^2C register.

The SM3 boost converter (SM3) has a 30-V, 500-mA, low-side integrated power stage switch that drives the external inductor. Another integrated 30-V, 25-mA switch (LED switch) is used to modulate the brightness of the external white LEDs . A simplified block diagram is shown in Figure 53

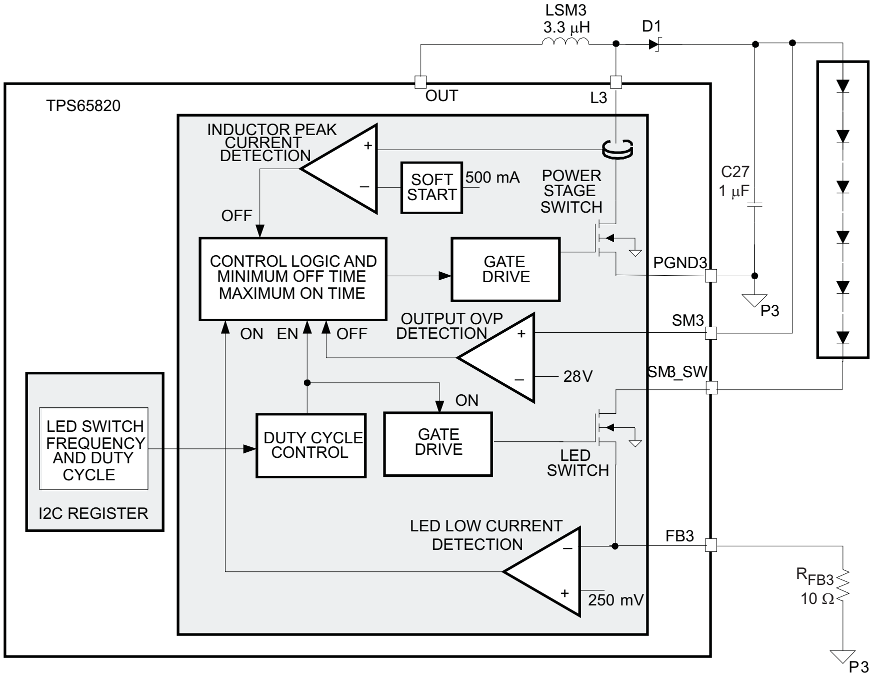


Figure 53. Simplified Block Diagram

The SM3 converter operates like a standard boost converter. The LED current is defined by the value of the external resistor R_{FB3}, connected from pin FB3 to AGND1. The integrated power stage switch control monitors the LED switch current (FB3) and the integrated power stage switch current, implementing a topology that effectively regulates the LED current independently of the input voltage and number of LEDs connected. The high voltage rating of the integrated switches enables driving up to six white LEDs, connected in a series configuration.

The internal LED switch, in series with the external LEDs, disconnects the LEDs from ground during shutdown. In addition, the LED switch is driven by a PWM signal that sets the duty cycle , enabling adjustment to the average LED current by modifying the settings of the I^2C register SM3_SET. With this control method, the LED brightness depends on the LED switch duty cycle only, and is independent of the PWM control signal.

The duty cycle control used in the SM3 converter LED switch is implemented by generating a burst of high frequency pulses, with a pattern that is repeated periodically. For a duty cycle of 50%, all of the high frequency pulses have a 50% duty cycle. The duty cycle control sets individual pulses to 100% duty cycle when increasing the LED_PWM output duty cycle; for decreasing LED_PWM output duty cycles, individual pulses are set to 0% duty cycle. An example of distinct duty cycles is shown in Figure 54, the sum of the individual pulses on/off time over the repetition period are equivalent to the duty cycle obtained with traditional single-pulse duty cycle circuits.

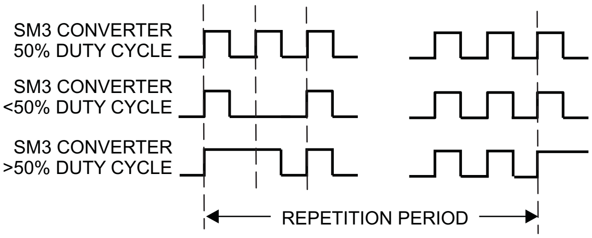


Figure 54. Example of Distinct Duty Cycles

The repetition period can be set using the register SOFT_RESET control bit SM3_LF_OSC to either 183 Hz (HI) or 122 Hz (LO). Each repetition period has a total of 256 pulses, enabling a resolution of 0.4% when programming the duty cycle.

SM3 Control Logic Overview

The SM3 boost converter operates in a pulse frequency modulation (PFM) scheme with constant peak current control. This control scheme maintains high efficiency over the entire load current range and enables the use of small external components, as the switching frequency can reach up to 1 MHz depending on the load conditions. The LED current ripple is defined by the external inductor size.

The converter monitors the sense voltage at pin FB3, and turns on the integrated power stage switch when $V_{(FB3)}$ is below the 250-mV (typ) internal reference voltage and the LED Switch is ON, starting a new cycle. The integrated power switch turns off when the inductor current reaches the internal 500-mA (typ) peak current limit, or if the switch is on for a period longer than the maximum on-time of 6 µs (typ). The integrated power switch also turns off when the LED switch is set to OFF. As the integrated power switch is turned off, the external Schottky diode is forward biased, delivering the stored inductor energy to the output. The main switch remains off until the FB3 pin voltage is below the internal 250-mV reference voltage and the LED switch is turned ON , when it is turned on again.

This PFM peak current control scheme sets the converter in discontinuous conduction mode (DCM), and the switching frequency depends on the inductor, input/output voltage and LED current. Lower LED currents reduce the switching frequency, with high efficiency over the entire LED current range. This regulation scheme is inherently stable, allowing a wide range for the selection of the inductor and output capacitor.

Peak Current Control (Boost Converter)

The SM3 integrated power stage switch is turned on until the inductor current reaches the DC current limit $I_{MAX(L3)}$ (500 mA , typ) . Due to internal delays, typically around 100 ns, the actual current exceeds the DC current limit threshold by a small amount. The typical peak current limit can be calculated as shown in Equation 8

$$I_{P(typ)} = I_{MAX(L3)} + \frac{V(OUT)}{L} \times 100\ \text{ns},\ \text{or}:\ I_{P(typ)} = 500\ \text{mA} + \frac{V(OUT)}{L} \times 100\ \text{ns} \tag{8}$$

The current overshoot is directly proportional to the input voltage, and inversely proportional to the inductor value.

Softstart

All inductive step-up converters exhibit high in-rush current during start-up. If no special precautions are taken, voltage drops can be observed at the input supply rail during start-up, with unpredictable results in the overall system operation.

The SM3 boost converter limits the inrush current during start-up by increasing the current limit in three steps:

1. 125 mA (typ),
2. 250 mA (typ) and
3. 500 mA (typ)

The two initial steps (125 mA and 250 mA) are active for 256 power stage switching cycles.

Enabling the SM3 Converter

The SM3_SET I^2C register controls the SM3 LED switch duty cycle. If the register is set to all zeros SM3 is set to OFF mode. When the host writes a value other than 00 in SM3_SET the SM3 converter is enabled, entering the soft start phase and then normal operation. The SM3 converter can operate with duty cycles varying from 0.4% to 99.6%, with LED switch frequencies of 100 Hz or 180 Hz. The LED switch operating frequency is set by bit SM3_LF, in the SOFT_RESET register.

Overvoltage Protection

The output voltage of the boost converter is sensed at pin SM3, and the integrated power stage switch is turned OFF when V(SM3) exceeds the internal over-voltage threshold V_{OVP3}. The converter returns to normal operation when V(SM3) < $V_{OVP3} – V_{HYS(OVP3)}$.

Under Voltage Lockout Operation

When the TPS65820 enters the UVLO mode, the SM3 converter is set to OFF mode with the power stage MOSFET switch and the LED switch open (off).

Thermal Shutdown Operation

When the TPS65820 enters the thermal shutdown mode, the SM3 converter is set to OFF mode with the power stage MOSFET switch and the LED switch open (off).

PWM DRIVERS

PWM Pin Driver

The TPS65820 offers one low-frequency, open-drain PWM driver, capable of driving up to 150 mA. The PWM frequency and duty cycle are defined by the PWM I^2C register settings. The PWM parameters are set in I^2C register PWM. Available frequency values range from 500 Hz to 15 kHz, with 8 frequency values and 16 duty cycle options (6.25% each).

LED_PWM Pin Driver

The TPS65820 has another PWM driver output (pin LED_PWM), which is optimized to drive a backlight LED. The LED_PWM driver controls the external LED current intensity using a pulse-width control method, with duty cycle being set by the I^2C register LED_PWM.

The pulse width method implemented generates a burst of high frequency pulses, with a pattern that is repeated periodically. For a duty cycle of 50%, all of the high -frequency pulses have a 50% duty cycle. The duty cycle control sets individual pulses to 100% duty cycle when increasing the LED_PWM output duty cycle; for decreasing LED_PWM output duty cycles individual pulses are set to 0% duty cycle. An example of distinct duty cycles is shown in Figure 55; the sum of the individual pulses on/off time over the repetition period is equivalent to the duty cycle obtained with traditional single-pulse duty cycle circuits.

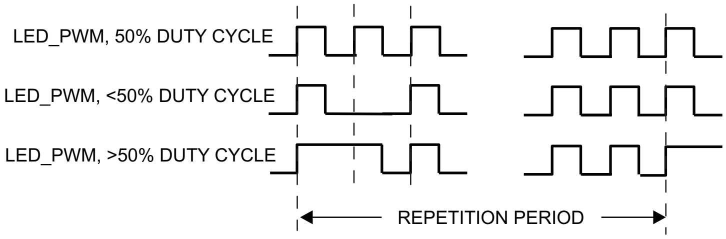


Figure 55. Example of Distinct Duty Cycles

The repetition period can be set using the register SOFT_RESET control bit SM3_LF_OSC to either 183 Hz (HI) or 122 Hz (LO). Each repetition period has a total of 256 pulses, enabling a resoltuion of 0.4% when programming the duty cycle. The LED_SET register enables control of the duty cycle via I^2C, with duty cycle ranging from 0.4% to 99.6%. Setting the LED_SET register to all zeros forces the LED_PWM pin to 0% duty cycle (OFF).

RGB Driver

The TPS65820 has a dedicated driver for an RGB external LED. Three outputs are available (pins RED, GREEN, BLUE), with common settings for operation mode (flash on/off, flash period, flash on time), LED current and phase delay between outputs. The TPS65820 RGB driver continually flashes the external LEDs connected to the RED, GREEN and BLUE pins using the flash operation parameters defined in register RGB_FLASH.

The currents for the external LEDs can be programmed via I^{2}C, and external resistors are not required to limit the LED current. However, they can be added to set the LED current if the available I^{2}C values are not compatible with the current application, as shown in the circuit below:

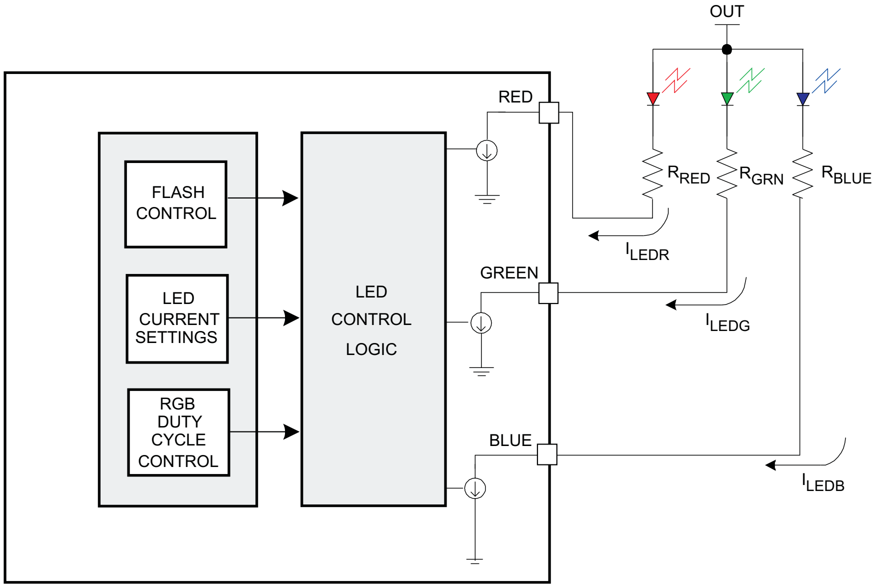


Figure 56. Limiting the external LED current

The flashing-mode parameters defined in register RGB_FLASH enable setting the flashing period from 1 to 8 seconds in 0.5-sec steps, or to continuous operation. Flashing operation is enabled by setting the FLASH_EN bit in register RGB_FLASH to HI.

Each driver has an individual duty cycle control. The duty cycle modulation method used is similar to the PWM_LED duty cycle control, with high frequency pulses being generated when the driver (RED, GREEN, or BLUE pins) is ON. The repetition period for the RGB drivers has a total of 32 pulses, enabling a 3.125% resolution when programming the individual RED, GREEN and BLUE drivers duty cycles. The duty cycles for each driver can be set individually using control bits on registers RGB_RED, RGB_GREEN and RGB_BLUE.

The RGB drivers can be programmed to sink 4, 8, or 12 mA, with no external current limiting resistor.

White LED, PWM Drivers — I^2C Registers

The I^2C registers that control LED AND PWM driver related functions are shown below. The HEX address for each register is shown by the register name, together with the R or W functionality for the register bits. Shaded values indicate default initial power-up values. In the equations replace Bn with 1 for HI state, and 0 for LO state.

	B7	B6	B5	B4	B3	B2	B1	B0
SM3_SET, ADDRESS=16, ALL BITS R/W								
Bit Name	SM3_I7 set	SM3_I6 set	SM3_I5 set	SM3_I4 set	SM3_I3 set	SM3_I2 set	SM3_I1 set	SM3_I0 set
Function	SM3 DUTY CYCLE CONTROL							
Value	See Table 11 for SM3 duty cycle settings , **default=0 (OFF)**							
RGB_FLASH, ADDRESS= 17, ALL BITS R/W								
Bit Name	FLASH_EN	FLASH_ON2	FLASH_ON1	FLASH_ON0	FLASH_PER3	FLASH_PER2	FLASH_PER1	FLASH_PER0
Function	FLASH MODE ON/OFF CTRL	FLASH MODE ON TIME			FLASH MODE PERIOD			
When 0	OFF	See Table 12 for RGB ON TIME settings, **default=0.1**			See Table 12 for RGB FLASH settings, **default=1**			
When 1	ON							
RGB_RED, ADDRESS=18, ALL BITS R/W								
Bit Name	RGB_ISET1	RGB_ISET0	PHASE	PWMR_D4	PWMR_D3	PWMR_D2	PWMR_D1	PWMR_D0
Function	RGB LED CURRENT SETTINGS		PHASE CONTROL	REG DRIVER DUTY CYCLE CONTROL				
When 0	**00= 0** 10= 8 mA 01= 4 mA 11=12 mA		GREEN out of Φ with RED & BLUE	See Table 12 for RGB_RED DUTY settings, **default=0**				
When 1			BLUE out of Φ with RED & GREEN					
RGB_GREEN, ADDRESS=19, ALL BITS R/W								
Bit Name	NOT USED	NOT USED	NOT USED	PWMG_D4	PWMG_D3	PWMG_D2	PWMG_D1	PWMG_D0
Function	NOT USED	NOT USED	NOT USED	GREEN DRIVER DUTY CYCLE CONTROL				
Value	NOT USED	NOT USED	NOT USED	See Table 12 for RGB_GREEN DUTY settings, **default=0**				
RGB_BLUE, ADDRESS=1A, ALL BITS R/W								
Bit Name	NOT USED	NOT USED	NOT USED	PWMB_D4	PWMB_D3	PWMB_D2	PWMB_D1	PWMB_D0
Function	NOT USED	NOT USED	NOT USED	BLUE DRIVER DUTY CYCLE CONTROL				
Value	NOT USED	NOT USED	NOT USED	See Table 12 for RGB_BLUE DUTY settings, **default=0**				
PWM, ADDRESS=1D, ALL BITS R/W								
Bit Name	PWM_EN	PWM1_F2	PWM_F1	PWM_F0	PWM_D3	PWM_D2	PWM_D1	PWM_D0
Function	PWM ON/OFF CONTROL	PWM DRIVER FREQUENCY SETTINGS			PWM DRIVER DUTY CYCLE SETTINGS			
When 0	Disabled	**000=15.6K** 011= 3K 110 = 1K 001=7.8K 100= 2K 111 = 500 010= 4.5K 101=1.5K **Default=15.6K**			See Table 13 for PWM DUTY settings, **default=0.0625**			
When 1	Enabled							
LED_PWM, ADDRESS=27, ALL BITS R/W								
Bit Name	LPWM_7 set	LPWM_6 set	LPWM_5 set	LPWM_4 set	LPWM_3 set	LPWM_2 set	LPWM_1 set	LPWM_0 set
Function	LED_PWM DRIVER DUTY CYCLE CONTROL							
Value	See Table 11 for LED_PWM DUTY settings, **default=0 (OFF)**							

Table 11. SM3 and LED_PWM Duty Cycle Settings

Dec	B7-B0	Dcpu	Dec	B7-B0	Dcpu	Dec	B7-B0	Dcpu	Dec	B7-B0	Dcpu	Dec	B7-B0	Dcpu
0	00000000	–	52	00110100	0.203	104	01101000	0.406	156	10011100	0.609	208	11010000	0.813
1	00000001	0.004	53	00110101	0.207	105	01101001	0.410	157	10011101	0.613	209	11010001	0.816
2	00000010	0.008	54	00110110	0.211	106	01101010	0.414	158	10011110	0.617	210	11010010	0.820
3	00000011	0.012	55	00110111	0.215	107	01101011	0.418	159	10011111	0.621	211	11010011	0.824
4	00000100	0.016	56	00111000	0.219	108	01101100	0.422	160	10100000	0.625	212	11010100	0.828
5	00000101	0.020	57	00111001	0.223	109	01101101	0.426	161	10100001	0.629	213	11010101	0.832
6	00000110	0.023	58	00111010	0.227	110	01101110	0.430	162	10100010	0.633	214	11010110	0.836
7	00000111	0.027	59	00111011	0.230	111	01101111	0.434	163	10100011	0.637	215	11010111	0.840
8	00001000	0.031	60	00111100	0.234	112	01110000	0.438	164	10100100	0.641	216	11011000	0.844
9	00001001	0.035	61	00111101	0.238	113	01110001	0.441	165	10100101	0.645	217	11011001	0.848
10	00001010	0.039	62	00111110	0.242	114	01110010	0.445	166	10100110	0.648	218	11011010	0.852
11	00001011	0.043	63	00111111	0.246	115	01110011	0.449	167	10100111	0.652	219	11011011	0.855
12	00001100	0.047	64	01000000	0.250	116	01110100	0.453	168	10101000	0.656	220	11011100	0.859
13	00001101	0.051	65	01000001	0.254	117	01110101	0.457	169	10101001	0.660	221	11011101	0.863
14	00001110	0.055	66	01000010	0.258	118	01110110	0.461	170	10101010	0.664	222	11011110	0.867
15	00001111	0.059	67	01000011	0.262	119	01110111	0.465	171	10101011	0.668	223	11011111	0.871
16	00010000	0.063	68	01000100	0.266	120	01111000	0.469	172	10101100	0.672	224	11100000	0.875
17	00010001	0.066	69	01000101	0.270	121	01111001	0.473	173	10101101	0.676	225	11100001	0.879
18	00010010	0.070	70	01000110	0.273	122	01111010	0.477	174	10101110	0.680	226	11100010	0.883
19	00010011	0.074	71	01000111	0.277	123	01111011	0.480	175	10101111	0.684	227	11100011	0.887
20	00010100	0.078	72	01001000	0.281	124	01111100	0.484	176	10110000	0.688	228	11100100	0.891
21	00010101	0.082	73	01001001	0.285	125	01111101	0.488	177	10110001	0.691	229	11100101	0.895
22	00010110	0.086	74	01001010	0.289	126	01111110	0.492	178	10110010	0.695	230	11100110	0.898
23	00010111	0.090	75	01001011	0.293	127	01111111	0.496	179	10110011	0.699	231	11100111	0.902
24	00011000	0.094	76	01001100	0.297	128	10000000	0.500	180	10110100	0.703	232	11101000	0.906
25	00011001	0.098	77	01001101	0.301	129	10000001	0.504	181	10110101	0.707	233	11101001	0.910
26	00011010	0.102	78	01001110	0.305	130	10000010	0.508	182	10110110	0.711	234	11101010	0.914
27	00011011	0.105	79	01001111	0.309	131	10000011	0.512	183	10110111	0.715	235	11101011	0.918
28	00011100	0.109	80	01010000	0.313	132	10000100	0.516	184	10111000	0.719	236	11101100	0.922
29	00011101	0.113	81	01010001	0.316	133	10000101	0.520	185	10111001	0.723	237	11101101	0.926
30	00011110	0.117	82	01010010	0.320	134	10000110	0.523	186	10111010	0.727	238	11101110	0.930
31	00011111	0.121	83	01010011	0.324	135	10000111	0.527	187	10111011	0.730	239	11101111	0.934
32	00100000	0.125	84	01010100	0.328	136	10001000	0.531	188	10111100	0.734	240	11110000	0.938
33	00100001	0.129	85	01010101	0.332	137	10001001	0.535	189	10111101	0.738	241	11110001	0.941
34	00100010	0.133	86	01010110	0.336	138	10001010	0.539	190	10111110	0.742	242	11110010	0.945
35	00100011	0.137	87	01010111	0.340	139	10001011	0.543	191	10111111	0.746	243	11110011	0.949
36	00100100	0.141	88	01011000	0.344	140	10001100	0.547	192	11000000	0.750	244	11110100	0.953
37	00100101	0.145	89	01011001	0.348	141	10001101	0.551	193	11000001	0.754	245	11110101	0.957
38	00100110	0.148	90	01011010	0.352	142	10001110	0.555	194	11000010	0.758	246	11110110	0.961
39	00100111	0.152	91	01011011	0.355	143	10001111	0.559	195	11000011	0.762	247	11110111	0.965
40	00101000	0.156	92	01011100	0.359	144	10010000	0.563	196	11000100	0.766	248	11111000	0.969
41	00101001	0.160	93	01011101	0.363	145	10010001	0.566	197	11000101	0.770	249	11111001	0.973
42	00101010	0.164	94	01011110	0.367	146	10010010	0.570	198	11000110	0.773	250	11111010	0.977
43	00101011	0.168	95	01011111	0.371	147	10010011	0.574	199	11000111	0.777	251	11111011	0.980
44	00101100	0.172	96	01100000	0.375	148	10010100	0.578	200	11001000	0.781	252	11111100	0.984
45	00101101	0.176	97	01100001	0.379	149	10010101	0.582	201	11001001	0.785	253	11111101	0.988
46	00101110	0.180	98	01100010	0.383	150	10010110	0.586	202	11001010	0.789	254	11111110	0.992
47	00101111	0.184	99	01100011	0.387	151	10010111	0.590	203	11001011	0.793	255	11111111	0.996
48	00110000	0.188	100	01100100	0.391	152	10011000	0.594	204	11001100	0.797			
49	00110001	0.191	101	01100101	0.395	153	10011001	0.598	205	11001101	0.801			
50	00110010	0.195	102	01100110	0.398	154	10011010	0.602	206	11001110	0.805			
51	00110011	0.199	103	01100111	0.402	155	10011011	0.605	207	11001111	0.809			

Table 12. RGB Duty Cycle Control Settings

RGB_D4	RGB_D3	RGB_D2	RGB_D1	RGB_D0	DC(%)	FLAS_P3	FLAS_P2	FLAS_P1	FLAS_P0	P(s)
0	0	0	0	0	0.00	0	0	0	0	1
0	0	0	0	1	3.23	0	0	0	1	1.5
0	0	0	1	0	6.45	0	0	1	0	2
0	0	0	1	1	9.68	0	0	1	1	2.5
0	0	1	0	0	12.90	0	1	0	0	3
0	0	1	0	1	16.13	0	1	0	1	3.5
0	0	1	1	0	19.35	0	1	1	0	4
0	0	1	1	1	22.58	0	1	1	1	4.5
0	1	0	0	0	25.80	1	0	0	0	5
0	1	0	0	1	29.03	1	0	0	1	5.5
0	1	0	1	0	32.25	1	0	1	0	6
0	1	0	1	1	35.48	1	0	1	1	6.5
0	1	1	0	0	38.70	1	1	0	0	7
0	1	1	0	1	41.93	1	1	0	1	7.5
0	1	1	1	0	45.15	1	1	1	0	8
0	1	1	1	1	48.38	1	1	1	1	CONTINUOUS
1	0	0	0	0	51.60		FLAS_ON2	FLAS_ON1	FLAS_ON0	ON_TIME (S)
1	0	0	0	1	54.83		0	0	0	0.1
1	0	0	1	0	58.05		0	0	1	0.15
1	0	0	1	1	61.23		0	1	0	0.2
1	0	1	0	0	64.50		0	1	1	0.25
1	0	1	0	1	67.73		1	0	0	0.3
1	0	1	1	0	70.95		1	0	1	0.4
1	0	1	1	1	74.18		1	1	0	0.5
1	1	0	0	0	77.40		1	1	1	0.6
1	1	0	0	1	80.63					
1	1	0	1	0	83.85					
1	1	0	1	1	87.08					
1	1	1	0	0	90.30					
1	1	1	0	1	93.53					
1	1	1	1	0	96.75					
1	1	1	1	1	99.98					

Table 13. PWM Frequency and Duty Cycle Settings

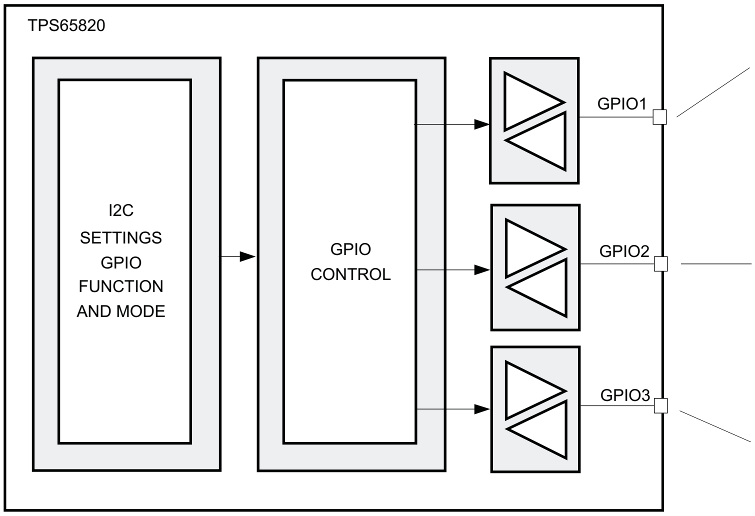
PWM FREQUENCY TABLE				PWM_D DUTY CYCLE				
PWM_F2	**PWM_F1**	**PWM_F0**	**F (Hz)**	**PWM2_D3**	**PWM2_D2**	**PWM2_D1**	**PWM2_D0**	**D_cycle (pu)**
0	0	0	15600	0	0	0	0	0.0625
0	0	1	7800	0	0	0	1	0.125
0	1	0	4500	0	0	1	0	0.1875
0	1	1	3000	0	0	1	1	0.25
1	0	0	2000	0	1	0	0	0.3125
1	0	1	1500	0	1	0	1	0.375
1	1	0	1000	0	1	1	0	0.4375
1	1	1	500	0	1	1	1	0.5
				1	0	0	0	0.5625
				1	0	0	1	0.625
				1	0	1	0	0.6875
				1	0	1	1	0.75
				1	1	0	0	0.8125
				1	1	0	1	0.875
				1	1	1	0	0.9375
				1	1	1	1	1

FUNCTIONALITY GUIDE – GENERAL PURPOSE INPUTS/OUTPUTS

GPIO3 FUNCTIONS			
CONFIGURED AS OUTPUT		**CONFIGURED AS INPUT**	**POWER-UP DEFAULT**
OUTPUT LEVEL	**Io(max) mA**	**A/D CONVERSION START TRIGGER**	
HI or LO at output set via I^2C	5	Falling or rising edge selected via I^2C	Input, no mode selected

GPIO2 FUNCTIONS				
CONFIGURED AS OUTPUT		**CONFIGURED AS INPUT**		**POWER-UP DEFAULT**
OUTPUT LEVEL	**Io(max) mA**	**HOST INTERRUPT REQUEST**	**SM2 ENABLE**	
HI or LO at output set via I2C	5	Set $\overline{\text{INT}}$ pin to LO via I2C when GPIO2 pin edge is detected. Rising or falling edge detection selected via I2C	GPIO2 level sets SM2 converter ON/OFF operation. GPIO2 pin level (HI or LO) for ON operation selected via I^2C	Input, no mode selected
		The host interrupt request and SM2 enable GPIO2 functions are mutually exclusive, and they should NOT be configured simultaneously		

GPIO1 FUNCTIONS					
CONFIGURED AS OUTPUT		**CONFIGURED AS INPUT**			**POWER-UP DEFAULT**
OUTPUT LEVEL	**Io(max) mA**	**HOST INTERRUPT REQUEST**	**SM1 ENABLE**	**SM1 AND SM2 STANDBY CONTROL**	
HI or LO at output set via I^2C	5	Set $\overline{\text{INT}}$ pin to LO via I^2C when GPIO1 pin edge is detected. Rising or falling edge detection set via I^2C	GPIO1 level sets SM1 converter ON/OFF operation. GPIO2 pin level (HI or LO) for ON operation set via I^2C	GPIO1 level sets SM2 and SM1 converters in standby mode. GPIO1 pin level (HI or LO) for standby mode set selected via I^2C	Input, no mode selected
		The host interrupt request, SM1 enable and SM1/SM2 standby control GPIO1 functions are mutually exclusive, and they should NOT be configured simultaneously.			



CONFIGURATION MODES:
1-OUTPUT
2-SM1/SM2 STANDBY CONTROL INPUT
3-SM1 ON/OFF CONTROL INPUT
4-INTERRUPT REQUEST CONTROL INPUT
GENERATES $\overline{\text{INT}}$ PIN HI→LO TRANSITION

CONFIGURATION MODES:
1-OUTPUT
2-SM2 ON/OFF CONTROL
3-INTERRUPT REQUEST CONTROL INPUT
4-GENERATES $\overline{\text{INT}}$ PIN HI→LO TRANSITION

CONFIGURATION MODES:
1-OUTPUT
2-ADC TRIGGER CONTROL
3-LDC0 ENABLE
4-CHARGE VOLTAGE SELECTION

Figure 57. Required External Components, Recommended Values, External Connections

General Purpose I/Os — GPIO 1, 2, 3

The TPS65820 integrates 3 general purpose open drain ports (GPIOs) that can be configured as selectable inputs or outputs. When configured as outputs the output level can be set to LO or HI via I^2C commands. When the GPIOs are configured as inputs the action to be taken when a transition or HI/LO level is detected at the GPIO pin is selectable via I^2C .

When configured as inputs the GPIOs can be set in the following modes:

1. Interrupt request: In this mode of operation a transition at the GPIO pin will generate an interrupt request at the interrupt controller. The GPIO interrupt request can be masked at the INT_MASK register. This operation mode is available for GPIO's 1 and 2.
2. SM1 and SM2 control: The GPIO's can be used to turn the converters SM1 and SM2 ON/OFF, as well as setting them in standby mode. This control mode is available for GPIO1 (SM1 on/off and SM1/SM2 standby) and GPIO2 (SM2 on/off control).
3. ADC trigger : GPIO3 can be configured as an external ADC trigger. The GPIO3 trigger configuration bit is located at the ADC register ADC_DELAY.

GPIOs Input Level Configuration

Using I^2C control bits the GPIOs can be configured as level detection inputs for SM1 and SM2 converter configuration. They also can be configured as edge detection inputs, to generate an interrupt request to the external host or to trigger an ADC conversion start .

When the GPIOs are configured as edge input detections for interrupt generation the edge transition will toggle the $\overline{\text{INT}}$ pin, as shown in Figure 58.

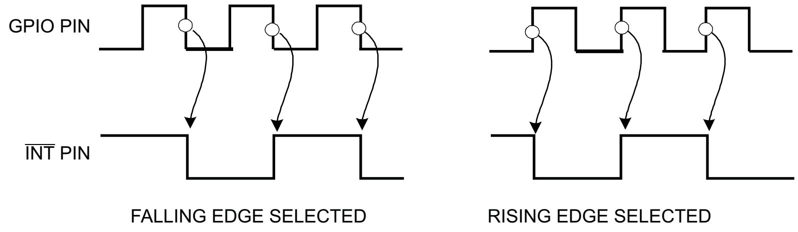


Figure 58. GPIO 1 or GPIO2 Configured as an Interrupt Request Input

Function Implementation: I^2C Commands Versus GPIO Commands

Some of the GPIO SM1/SM2 control functions overlap I^2C register control functions. Table 14 describes the TPS65820 action when the GPIO's command and I^2C registers commands are not compatible with each other.

Table 14. GPIO Commands and I^2C Registers Commands

SM1 AND SM2 ON/OFF I^2C COMMAND	GPIO COMMAND	SM1 OR SM2 MODE SET
CONVERTER DISABLED	DON'T CARE	DISABLED
CONVERTER ENABLED	CONVERTER ENABLED	ENABLED
DON'T CARE	CONVERTER DISABLED	DISABLED
SM1 AND SM2 STANDBY I^2C COMMAND	**GPIO COMMAND**	**SM1 OR SM2 MODE SET**
DO NOT SET STANDBY	DON'T CARE	NORMAL
SET STANDBY	SET STANDBY	STANDBY
DON'T CARE	DO NOT SET STANDBY	NORMAL

GPIO Configuration Table

Table 15 describes the I^2C register settings required to program the available GPIO modes.

Table 15. Recommended GPIO Configuration Procedure

GPIO MODE	I^2C REGISTERS	I2C REGISTER BIT SETTING	ADDITIONAL DETAILS
GPIO3 = OUTPUT	GPIO3	GPIO3I/O=HI **AND** GPIO3OUT=HI	GPIO3 PIN SET TO HIGH IMPEDANCE MODE
		GPIO3I/O=HI **AND** GPIO3OUT=LO	V(GPIO3) = V_{OL}
GPIO3 =INPUT ADC CONVERSION START TRIGGER	GPIO3 **AND** ADC_DELAY	GPIO3I/O=LO **AND** ADC_TRG_GPIO3=HI **AND** EDGE_GPIO3=HI	GPIO3 pin rising edge triggers ADC conversion
		GPIO3I/O=LO **AND** ADC_TRG_GPIO3=HI **AND** EDGE_GPIO3=LO	GPIO3 pin falling edge triggers ADC conversion
GPIO2 = OUTPUT	GPIO12	GPIO2I/O=HI **AND** GPIO2OUT=HI	GPIO3 PIN SET TO HIGH IMPEDANCE MODE
		GPIO2I/O=HI **AND** GPIO2OUT=LO	V(GPIO3) = V_{OL}
GPIO2=INPUT, HOST INTERRUPT REQUEST	GPIO12 **AND** GPIO3	GPIO2I/O=LO **AND** GPIO2INT=HI **AND** GPIO2LVL=HI **AND** GPIO2SM2=LO	$\overline{\text{INT}}$ pin HI→LO→HI at V(GPIO2) falling edge
		GPIO2I/O=LO **AND** GPIO2INT=HI **AND** GPIO2LVL=HI **AND** GPIO2SM2=LO	$\overline{\text{INT}}$ pin HI→LO→HI at V(GPIO2) rising edge
GPIO2=INPUT, SM2 ENABLE	GPIO12 **AND** GPIO3	GPIO2I/O=LO **AND** GPIO2INT=LO **AND** GPIO2LVL=HI **AND** GPIO2SM2=HI	SM2 converter ON at V(GPIO2)=HI
		GPIO2I/O=LO **AND** GPIO2INT=LO **AND** GPIO2LVL=LO **AND** GPIO2SM2=HI	SM2 converter ON at V(GPIO2)=LO
GPIO1 = OUTPUT	GPIO12	GPIO1I/O=HI **AND** GPIO1OUT=HI	GPIO1 PIN SET TO HIGH IMPEDANCE MODE
		GPIO1I/O=HI **AND** GPIO1OUT=LO	V(GPIO1) = V_{OL}
GPIO1=INPUT, HOST INTERRUPT REQUEST	GPIO12 **AND** GPIO3	GPIO1I/O=LO AND GPIO1INT=HI **AND** GPIO1LVL=HI **AND** GPIO1SM1=LO **AND** GPIO1SMSBY=LO	$\overline{\text{INT}}$ pin HI→LO→HI at V(GPIO1) falling edge
		GPIO1I/O=LO **AND** GPIO1INT=HI **AND** GPIO1LVL=LO **AND** GPIO1SM1=LO **AND** GPIO1SMSBY=LO	$\overline{\text{INT}}$ pin HI→LO→HI at V(GPIO1) rising edge
GPIO1=INPUT, SM1 ENABLE	GPIO12 **AND** GPIO3	GPIO1I/O=LO **AND** GPIO1INT=LO **AND** GPIO1LVL=HI **AND** GPIO1SM1=HI **AND** GPIO1SMSBY=LO	SM1 converter ON at V(GPIO1)=HI
		GPIO1I/O=LO **AND** GPIO1INT=LO **AND** GPIO1LVL=LO **AND** GPIO1SM1=HI **AND** GPIO1SMSBY=LO	SM1 converter ON at V(GPIO1)=LO
GPIO1=INPUT, SM1/SM2 STANDBY CONTROL	GPIO12 **AND** GPIO3	GPIO1I/O=LO **AND** GPIO1INT=LO **AND** GPIO1LVL=HI **AND** GPIO1SM1=LO **AND** GPIO1SMSBY=HI	SM1/SM2 converter standby set at V(GPIO2)=HI
		GPIO1I/O=LO **AND** GPIO1INT=LO **AND** GPIO1LVL=LO **AND** GPIO1SM1=LO **AND** GPIO1SMSBY=HI	SM1/SM2 converter standby set at V(GPIO2)=LO

GPIOs — I^{2}C Registers

The I^{2}C registers that control GPIO-related functions are shown below. The HEX address for each register is shown by the register name, together with the R or W functionality for the register bits. Shaded values indicate default initial power-up values.

	B7	B6	B5	B4	B3	B2	B1	B0
GPIO12, ADDRESS=1B, ALL BITS R/W								
Bit Name	GPIO2I/O	GPIO1I/O	GPIO2OUT	GPIO1OUT	GPIO2LVL	GPIO1LVL	GPIO1SMSBY	GPIO1SM1
Function	GPIO2 MODE	GPIO1 MODE	SET GPIO2 LEVEL (OUTPUT ONLY)	SET GPIO1 LEVEL (OUTPUT ONLY)	GPIO2 EDGE AND LEVEL DETECTION	GPIO1 EDGE AND LEVEL DETECTION	GPIO 1 CONTROLS SM1 AND SM2 STANDBY ON/OFF	GPIO1 CONTROLS SM1 ON/OFF
When 0	INPUT	INPUT	LOW	LOW	RISING EDGE, LO LEVEL	RISING EDGE, LO LEVEL	DISABLED	DISABLED
When 1	OUTPUT	OUTPUT	HIGH	HIGH	FALLING EDGE, HI LEVEL	FALLING EDGE, HI LEVEL	ENABLED	ENABLED
GPIO3, ADDRESS=1C, ALL BITS R/W								
Bit Name	GPIO3I/O	GPIO3OUT	LDO0_EN	CHG_VOLT	NOT USED	GPIO2 INT	GPIO1 INT	GPIO2SM2
Function	GPIO3 MODE	SET GPIO3 LEVEL (OUTPUT ONLY)	LDO0 ON/OFF CONTROL	CHARGE VOLTAGE SAFETY BIT	NOT USED	GPIO2 TRIGGERS $\overline{\text{INT}}$:HI→LO	GPIO1 TRIGGERS $\overline{\text{INT}}$:HI→LO	SM2 ON/OFF CONTROL
When 0	INPUT	LOW	OFF	4.20 V	NOT USED	DISABLED	DISABLED	DISABLED
When 1	OUTPUT	HIGH	ON	4.36 V	NOT USED	ENABLED	ENABLED	ENABLED

APPLICATION INFORMATION

INDUCTOR AND CAPACITOR SELECTION — CONVERTERS SM1 AND SM2

SM1 and SM2 are designed with internal voltage mode compensation and the stabilization is based on choosing an LC filter that has a corner frequency around 27 kHz. It is not recommended to use LC values that would be outside the range of 13 kHz to 40 kHz.

Equation 9 calculates the corner frequency of the output LC filter. The standard recommended LC values are 3.3 µH and 10 µF.

$$F = \frac{1}{2\pi\sqrt{LC}} = 27.7\text{ kHz}\quad \text{(a) for } L = 3.3\ \mu\text{H and } C = 10\ \mu\text{F} \tag{9}$$

The inductor value, along with the input voltage VIN, output voltage V_{OUT} and switching frequency f define the ripple current. Typically the ripple current target is 30% of the full load current. At light loads it is desirable for ripple current to be less then 150% of the light load current.

The inductor should be chosen with a rating to handle the peak ripple current., if an inductor’s current gets higher than its rated saturation level (DCR) , the inductance starts to fall off, and the inductor’s ripple current increases exponentially . The DCR of the inductor plays an important role in efficiency and size of the inductor. Larger diameter wire has less DCR but may increase the size of the inductor

Equation 10 calculates the target inductor value. If an inductor value has already been chosen, Equation 11, calculates the inductor’s ripple current under static operating conditions. The ripple amplitude can be calculated during the on time (positive ramp) or during the off time (negative ramp). It is easiest to calculate the ripple using the off time since the inductor’s voltage is the output voltage.

$$I_{target} = \frac{V_{OUT}}{0.3 \times I_{OUT\_MAX}}\,\frac{\left(1 - \frac{V_{OUT}}{V_{IN\_MAX}}\right)}{f} \tag{10}$$

$$\Delta I_L = \frac{V_L}{L} \times \Delta t = \frac{V_{OUT}}{L}\,\frac{\left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{f} \tag{11}$$

Equation 12 calculates the peak current due to the output load and ripple current

$$I_{Lmax} = I_{OUTmax} + \frac{\Delta I_L}{2} \tag{12}$$

For a faster transient response, a lower inductor and higher capacitance allows the output current to ramp faster, while the addition capacitance holds up the output longer (a 2.2-µH inductor in combination with a 22-µF output capacitor are recommended).

The highest inductor current occurs at the maximum input voltage. The peak inductor current during a transient may be higher than the steady state peak current and should be considered when choosing an inductor. Monitoring the inductor current, for non-saturation operation, during a transient of 1.2 × I_loadmax at Vin_max, will insure adequate saturation margin.

Table 16. Inductors for Typical Operation Conditions

DEVICE	INDUCTOR VALUE	TYPE	COMPONENT SUPPLIER
DCDC3 converter	3.3 µH	CDRH2D14NP-3R3	Sumida
	3.3 µH	PDS3010-332	Coilcraft
	3.3 µH	VLF4012AT-3R3M1R3	TDK
	2.2 µH	VLF4012AT-2R2M1R5	TDK
	2.2 µH	NR3015T2R2	Taoup-Uidem

APPLICATION INFORMATION (continued)

Table 16. Inductors for Typical Operation Conditions (continued)

DEVICE	INDUCTOR VALUE	TYPE	COMPONENT SUPPLIER
DCDC2 converter	3.3 µH	CDRH2D18/HPNP-3R3	Sumida
	3.3 µH	VLF4012AT-3R3M1R3	TDK
	2.2 µH	VLCF4020-2R2	TDK
DCDC1 converter	3.3 µH	CDRH3D14/HPNP-3R2	Sumida
	3.3 µH	CDRH4D28C-3R2	Sumida
	3.3 µH	MSS5131-332	Coilcraft
	2.2 µH	VLCF4020-2R2	TDK

OUTPUT CAPACITOR SELECTION, SM1, SM2 CONVERTERS

The advanced Fast Response voltage mode control scheme of the SM1, SM2 converters implemented in the TPS65020 allow the use of small ceramic capacitors with a typical value of 10 µF for a 3.3-µH inductor , without having large output voltage under and overshoots during heavy load transients.

Ceramic capacitors having low ESR values have low output voltage ripple, and recommended values and manufacturers are listed in Table 1. Often, due to the low ESR, the ripple current rating of the ceramic capacitor is adequate to meet the inductor’s currents requirements.

The RMS ripple current is calculated as:

$$I_{RMSCout} = \frac{1 - \frac{V_{OUT}}{V_{IN}}}{2 \times L \times f} \times \frac{1}{\sqrt{3}} \tag{13}$$

At nominal load current, the inductive converters operate in PWM mode. The overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor: The output voltage ripple will be maximum at the highest input voltage Vin.

$$V_{RMSCout} = \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \left(\frac{1}{8 \times Cout \times f} + ESR\right) \tag{14}$$

At light load currents, the converters operate in PFM and the output voltage ripple is dependent on the output capacitor value. The output voltage ripple is set by the internal PFM output voltage comparator delay and the external capacitor. The typical output voltage ripple is less than 1% of the nominal output voltage.

Table 17. Input/Output Capacitors for Typical Operation Conditions

CAPACITOR VALUE	CASE SIZE	COMPONENT SUPPLIER	COMMENTS
22 µF	1260	TDK C3216X5R0J226M	Ceramic
22 µF	1260	Taiyo Yuden JMK316BJ226ML	Ceramic
10 µF	0805	Taiyo Yuden JMK212BJ106M	Ceramic
10 µF	0805	TDK C2012X5R0J106M	Ceramic
22 µF	0805	TDK C2012X5R0J226MT	Ceramic
22 µF	0805	Taiyo Yuden JMK212BJ226MG	Ceramic

INPUT CAPACITOR SELECTION, SM1, SM2 CONVERTERS

Buck converters have a pulsating input current that can generate high input voltage spikes at V_{IN}. A low ESR input capacitor is required to filter the input voltage, minimizing the interference with other circuits connected to the same power supply rail. Each dc-dc converter requires a 10-µF ceramic input capacitor on its input pin.

OUTPUT VOLTAGE SELECTION, SM1, SM2 CONVERTERS

Typically the output voltage is programmed by the I^2C. An external divider can be added to raise the output voltage, if the available I^2C values do not meet the application requirements. Care must be taken with this special option, since this external divider (gain factor) would apply to any selected I^2C output voltage value for this converter.

Equation 16 calculates R1, Let R2 = 20 kΩ:

$$R1 = \left[\frac{V_{SMxOUT}}{V_{FB}} - 1\right] R2 \tag{16}$$

Where V_{FB} is the I^2C selected voltage, is the desired output voltage and R1/R2 is the feedback divider.

DESIGN EXAMPLES

SM1, SME CONVERTER DESIGN EXAMPLE

Design Conditions and Parametrs for SM1 or SM2:

Vin_SM1/2: 4.6V typical (May be less if input source is limited).
Vout_SM1/2: 1.24 V
Iout_max: 0.6 A
fsw = 1500 kHz
fc = 25 kHz

$$L_{target} = \frac{V_{OUT}}{0.3 \times I_{OUT\_MAX}} \frac{\left[1 - \frac{V_{OUT}}{V_{IN\_MAX}}\right]}{fsw} = 3.35\ \mu H,\ 3.3\ \mu H \text{ is a good target.} \tag{17}$$

$$C = \frac{1}{L[2 \times \pi \times fc]^2} = 10.5\ \mu F\ \ 10\ \mu F \text{ is a good target.} \tag{18}$$

CHARGER DESIGN EXAMPLE

Design Conditions and Parameters for Charger:

Vout: 4.6 V; (OUT pin is input to Charger)
Fast Charge Current, I_{PGM}: 1 A
DPPM-OUT Threshold: 4.3 V; (Charging Current reduces when OUT falls to this level)
Safety Timer: 5 hr
Battery Short Circuit Delay, t_{DELAY}: 47 µs; (Delays BAT short circuit during hot plug of battery)
TS Temperature range: Disabled
K_{SET}=400; V_{SET}=2.5 V; K_{DPPM} = 1.15; I_{DPPM} = 100 µA; K_{TMR}=0.36 s/Ω

Program Fast Charge Current Level:

$$R_{ISET} = \frac{K_{SET} \times V_{SET}}{I_{PGM}} = 1\ k\Omega \tag{19}$$

Program DPPM_OUT Voltage Level (Level at which Charging Current Reduces)

$$R_{DPPM} = \frac{V_{DPPM\_OUT}}{K_{DPPM} \times I_{DPPM}} = 3.74\ k\Omega \tag{20}$$

Program BAT Short Circuit Delay (Used for inserting battery)

$$C_{DPPM} = t_{DELAY} \times I_{DPPM} = 4.7\ \text{Nf} \tag{21}$$

Program 5 Hour Safety timer

$$R_{TMR} = \frac{t_{SAFETY-HR} \times 3600\ \text{sec/hr}}{K_{TMR}} = 50\ \text{k}\Omega \tag{22}$$

Disable/Program TS

R_{TS} = 49.9k – fixed resistor to disable TS input.

$V_{TS} = I_{TS} \times R_{TS} = 20\ \mu A \times 49.9\ k = 0.998\ V$

The TS pin has a 20-µA current source output that biases the resistor or thermistor. If V_{TS} is within the 0.5- to 2.5-V window, normal operation is allowed. If a 503AT thermistor is used, the typical range is 4°C to 41°C.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS65820RSHR	ACTIVE	QFN	RSH	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TPS65820RSHRG4	ACTIVE	QFN	RSH	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TPS65820RSHT	ACTIVE	QFN	RSH	56	250	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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